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Analysis and Simulation of a D-STATCOM for Voltage Quality Improvement

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Abstract: Voltage flicker is a major power quality concern for both power companies and customers. This paper discusses the dynamic performance of a (D-STATCOM) with ESS for mitigation of voltage flicker. The (D-STATCOM) is intended to replace the widely used static var compensator (SVC). A Distribution Static Synchronous Compensator (D-STATCOM) is used to regulate voltage on a 25-kV distribution network. The (D-STATCOM) protects the utility transmission or distribution system from voltage sag and /or flicker caused by rapidly varying reactive current demand. The (D-STATCOM) regulates bus voltage by absorbing or generating reactive power. This voltage is provided by a voltage-sourced PWM inverter. The simulation is carried out using MATLAB/SIMULINK and the simulation results illustrate the performance of (D-STATCOM) in mitigation of voltage flicker.

Key words: Power Quality, Energy Storage System (ESS), D-STATCOM, Voltage Flicker, Synchronous Reference Frame (SRF).

INTRODUCTION

Utility and customer-side disturbances result in terminal voltage fluctuations, transients, and waveform distortions on the electric grid. Power electronic controllers for distribution systems, namely custom power devices, are able to enhance the reliability and quality of power that is delivered to customers (Hingorani, 1995).

A distribution static compensator or D-STATCOM is a fast response, solid-state power controller that provides flexible voltage control at the point of connection to the utility distribution feeder for power quality (PQ) improvements. It can exchange both active and reactive power with the distribution system by varying the amplitude and phase angle of the converter voltage with respect to the line terminal voltage, if an energy storage system (ESS) is included into the dc bus. The result is a controlled current flow through the tie reactance between the D-STATCOM and the distribution network. This enables the D-STATCOM to mitigate voltage fluctuations and to correct the power factor of weak distribution systems in instantaneous real-time (Song and Johns, 1999). In general, the D-STATCOM can be utilized for providing voltage regulation, power factor correction, harmonics compensation and load leveling (Hingorani and Gyugyi, 2000).

During the transient conditions the D-STATCOM provides leading or lagging reactive power to active system stability, power factor correction and load balancing and /or harmonic compensation of a particular load (IEEE PES working group, 1996),(Hingorani and Gyugyi, 2000)

The D-STATCOM has emerged as a promising device to provide not only for voltage sags mitigation but a host of other power quality solutions such as voltage stabilization, flicker suppression, power factor correction and harmonic control (Reed et al 1999). The D-STATCOM has additional capability to sustain reactive current at low voltage, reduce land use and can be developed as a voltage and frequency support by replacing capacitors with batteries as energy storage (Taylor, 1995). The proposed multi-level control scheme for the integrated D-STATCOM/BESS device is based on concepts of instantaneous power on the synchronous-rotating dq reference frame (Schauder and Mehta, 1993). This paper presents a model for (D-STATCOM) for voltage flicker mitigation. The most commonly used methods for compensation of voltage flicker is by regulating the Electric Arc Furnace (EAF) passive components (Esfandiari and Parniani, 2004),(Montanari et al 1993), (Marshall, 1997), static VAR compensator (SVC) and D-STATCOM.

Basic Configuration and Operation of D-STATCOM:

The D-STATCOM is a three phase and shunt connected power electronics based reactive power compensation equipment, which generates and /or absorbs the reactive power whose output can be varied so as to maintain control of specific parameters of the electric power system.

It is connected near the load at the distribution systems. The Detailed Versus Average Model of a D-STATCOM is shown in Fig. 1. It consists of a dc capacitor, three-phase inverter (IGBT, thyristor) module, ac filter, coupling transformer and a control strategy (Taylor, 1995). The AC voltage difference across the leakage reactance power exchange between the D-STATCOM and the Power system, such that the AC voltages at the bus bar can be regulated to improve the voltage profile of the power system, which is primary duty of the D-STATCOM. However a secondary damping function can be added in to the D-STATCOM for enhancing power

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system oscillation stability. The D-STATCOM provides operating characteristics similar to a rotating Synchronous compensator without the mechanical inertia. The D-STATCOM employs solid state power switching devices and provides rapid controllability of the three phase voltages, both in magnitude and phase angle.

The D-STATCOM employs an inverter to convert the DC link voltage V_{dc} on the capacitor to a voltage source of adjustable magnitude and phase. Therefore the D-STATCOM can be treated as a voltage controlled source. The D-STATCOM can also be seen as a current controlled source.

The basic objective of a VSI is to produce a sinusoidal AC voltage with minimal harmonic distortion from a DC voltage. The operation of the D-STATCOM is as follows: The voltage is compared with the AC bus voltage system (V_s), When the AC bus voltage magnitude is above that of the VSI magnitude (V_c); the AC system sees the D-STATCOM as inductance connected to its terminals. Otherwise if the VSI voltage magnitude is above that of the AC bus voltage magnitude, the AC system sees the D-STATCOM as capacitance to its terminals. If the voltage magnitudes are equal, the reactive power exchange is zero.

If the D-STATCOM has a DC source or energy storage device on its DC side, it can supply real power to the power system. This can be achieved by adjusting the phase angle of the D-STATCOM terminals and the phase angle of the AC power system. When phase angle of the AC power system leads the VSI phase angle, the D-STATCOM absorbs the real power from the AC system, if the phase angle of the AC power system lags the VSI phase angle, the D-STATCOM supplies real power to AC system.

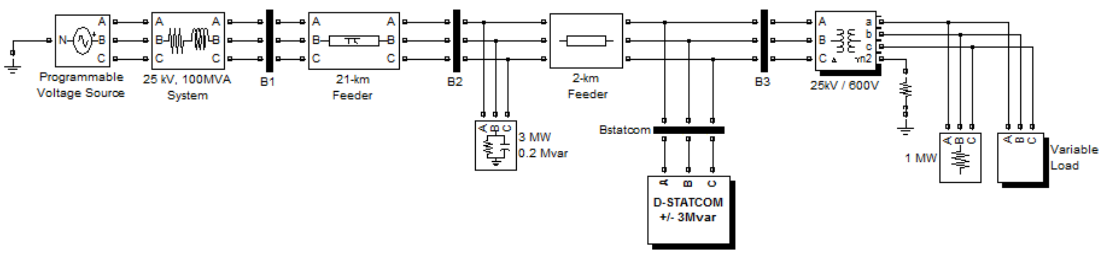

Fig. 1: Detailed Versus Average Model of D-STATCOM.

Synchronous Reference Frame Theory (d-q theory) For Flicker Mitigation:

The synchronous reference theory is based on the transformation of the stationary reference frame three phase variables (a,b,c) to synchronous reference frame variables (d,q,0) whose direct (d) and quadrature (q) axes rotate in space at the synchronous speed ω_e. ω_e is the angular electrical speed of the rotating magnetic field of the three phase supply, given by $\omega_e=2\pi f_s$, where f_s is the frequency of the supply.

If θ is the transformation angle, then the current transformation from abc to d-q-0 frame is defined as

$$\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} = \sqrt{\tfrac{2}{3}} \begin{bmatrix} \cos\theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ -\sin(\theta) & -\sin\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (1)$$

The block diagram of the DSTATCOM controller for flicker mitigation based on d-q theory is shown in Fig. 2.

The three- phase source voltages (V_{sa}, V_{sb} and V_{sc}) are applied to three-phase Phase Locked Loop (PLL) to synchronize the three-phase voltages at the converter output with the zero crossings of the fundamental component of the supply phase voltages. The PLL provides the synchronous reference angle θ required by the abc-dq0 (and dq0-abc) transformation.

The three phase source currents (i_{sa}, i_{sb}, i_{sc}) and bridge inverter currents (i_{ia}, i_{ib}, i_{ic})are converted into equivalent direct axis and quadrature axis component currents (i_d, i_q) by using (1).

In order to maintain the reactive power drawn from the source as zero, the output currents of the three phase bridge inverter are controlled in such a way that the inverter supplies the required reactive power. Thus for flicker mitigation, the source reactive power has to be zero. Therefore i_q reference (i_{qref}) is set at zero for inverter control. The reactive current supplied by the source (i_q) is subtracted from the reference value (i_{qref}=0) to obtain the error in reactive current for full compensation. This error signal is processed through a PI controller block to obtain the reference voltage signal (V_{qref}), which is fed to the dq0- abc transformation block. The reference for id (i_{dref}) comes from the DC link voltage PI controller, which maintains the DC link voltage (V_{dc}) at reference value.

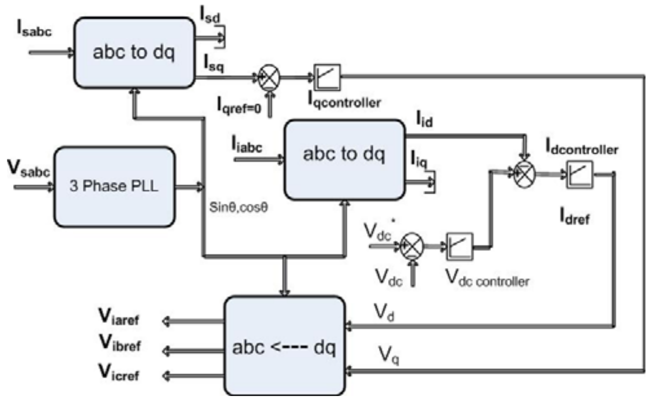

Fig. 2: D-STATCOM controller with d-q theory.

The active current supplied by the inverter (i_d) is subtracted from the reference value (i_{dref}) and this error signal is processed through a PI controller block to obtain the reference voltage signal (V_{dref}), which goes as another input for dq0-abc transformation. PI compensators for current and voltage loops are tuned to give the optimum performance.

The output voltage signals of transformation block (dq0-abc) act as reference voltages (V_{iaref}, V_{ibref} and V_{icref}) for PWM signal generators of bridge inverter. These signals are compared with a triangular carrier wave to obtain PWM signals for bridge inverter phases.

Model Description:

A Distribution Static Synchronous Compensator (D-STATCOM) is used to regulate voltage on a 25-kV distribution network. Two feeders (21 km and 2 km) transmit power to loads connected at buses B2 and B3. A shunt capacitor is used for power factor correction at bus B2. The 600-V load connected to bus B3 through a 25kV/600V transformer represents a plant absorbing continuously changing currents, similar to an arc furnace, thus producing voltage flicker. The variable load current magnitude is modulated at a frequency of 5 Hz so that its apparent power varies approximately between 1 MVA and 5.2 MVA, while keeping a 0.9 lagging power factor. This load variation will allow you to observe the ability of the D-STATCOM to mitigate voltage flicker.

The D-STATCOM regulates bus B3 voltage by absorbing or generating reactive power. This reactive power transfer is done through the leakage reactance of the coupling transformer by generating a secondary voltage in phase with the primary voltage (network side). This voltage is provided by a voltage-sourced PWM inverter. When the secondary voltage is lower than the bus voltage, the D-STATCOM acts like an inductance absorbing reactive power. When the secondary voltage is higher than the bus voltage, the D-STATCOM acts like a capacitor generating reactive power.

The D-STATCOM consists of the following components:

- a 25kV/1.25kV coupling transformer which ensures coupling between the PWM inverter and the network.
- a voltage-sourced PWM inverter consisting of two IGBT bridges. This twin inverter configuration produces less harmonics than a single bridge, resulting in smaller filters and improved dynamic response. In this case, the inverter modulation frequency is 28*60=1.68 kHz so that the first harmonics will be around 3.36 kHz.
- LC damped filters connected at the inverter output. Resistances connected in series with capacitors provide a quality factor of 40 at 60 Hz.
- a 10000-microfarad capacitor acting as a DC voltage source for the inverter
- a voltage regulator that controls voltage at bus B3
- a PWM pulse generator using a modulation frequency of 1.68 kHz
- anti-aliasing filters used for voltage and current acquisition.

The D-STATCOM controller consists of several functional blocks:

- a Phase Locked Loop (PLL). The PLL is synchronized to the fundamental of the transformer primary voltages.
- two measurement systems. Vmeas and Imeas blocks compute the d-axis and q-axis components of the voltages and currents by executing an abc-dq transformation in the synchronous reference determined by sin (wt) and cos(wt) provided by the PLL.

- An inner current regulation loop. This loop consists of two proportional-integral (PI) controllers that control the d-axis and q-axis currents. The controllers outputs are the V_d and V_q voltages that the PWM inverter has to generate. The V_d and V_q voltages are converted into phase voltages V_a, V_b, V_c which are used to synthesize the PWM voltages. The I_q reference comes from the outer voltage regulation loop (in automatic mode) or from a reference imposed by Q_{ref} (in manual mode). The I_d reference comes from the DC-link voltage regulator.
- an outer voltage regulation loop. In automatic mode (regulated voltage), a PI controller maintains the primary voltage equal to the reference value defined in the control system dialog box.
- a DC voltage controller which keeps the DC link voltage constant to its nominal value (V_{dc}=2.4kv)

Table 1: The parameter values of the system.

Parameters	Values
Source voltage	25kV/50Hz
Source Power	100MVA
Total Line Length	23Km
Coupling transformer	25kV/1.25kV
Modulation frequency	1.68 kHz
DC link voltage	2.4 kV

Simulation Results:

1. D-Statcom Dynamic Response:

During this test, the variable load will be kept constant and you will observe the dynamic response of a D-STATCOM to step changes in source voltage. Check that the modulation of the Variable Load is not in service (Modulation Timing [T_{on} T_{off}]=[0.15 1]*100 > Simulation Stop time). The Programmable Voltage Source block is used to modulate the internal voltage of the 25-kV equivalent. The voltage is first programmed at 1.077 pu in order to keep the D-STATCOM initially floating (B_3 voltage=1 pu and reference voltage V_{ref}=1 pu). Three steps are programmed at 0.2 s, 0.3 s, and 0.4 s to successively increase the source voltage by 6%, decrease it by 6% and bring it back to its initial value.

Start the simulation. Observe on Fig. 3 the phase voltage waveform of the D-STATCOM as well as Output voltage of voltage source inverter on Fig. 4. After a transient lasting approximately 0.15 sec., the steady state is reached. Initially, the source voltage is such that the D-STATCOM is inactive. It does not absorb nor provide reactive power to the network. At t = 0.2 s, the source voltage is increased by 6%. The D-STATCOM compensates for this voltage increase by absorbing reactive power from the network (Q = +2.7 Mvar on Fig. 5). At t = 0.3 s, the source voltage is decreased by 6% from the value corresponding to Q = 0. The D-STATCOM must generate reactive power to maintain a 1 pu voltage (Q changes from +2.7 MVAR to -2.8 MVAR). Note that when the D-STATCOM changes from inductive to capacitive operation, the modulation index of the PWM inverter is increased from 0.56 to 0.9 which corresponds to a proportional increase in inverter voltage. Reversing of reactive power is very fast, about one cycle, as observed on D-STATCOM current (magenta signal on Fig. 6).

2. Mitigation of Voltage Flicker:

During this test, voltage of the Programmable Voltage Source will be kept constant and you will enable modulation of the Variable Load so that you can observe how the D-STATCOM can mitigate voltage flicker. In the Programmable Voltage Source block menu, change the "Time Variation of" parameter to "None". In the Variable Load block menu, set the Modulation Timing parameter to [T_{on} T_{off}] = [0.15 1] (remove the 100 multiplication factor). Finally, in the D-STATCOM Controller, change the "Mode of operation" parameter to "Q regulation" and make sure that the reactive power reference value Q_{ref} (2nd line of parameters) is set to zero. In this mode, the D-STATCOM is floating and performs no voltage correction.

Run the simulation and observe on Fig. 8 variations of P and Q at bus B3 as well as voltages at buses B1 and B3 Fig 9. Without D-STATCOM, B3 voltage varies between 0.96 pu and 1.04 pu (+/- 4% variation). Now, in the D-STATCOM Controller, change the "Mode of operation" parameter back to "Voltage regulation" and restart simulation. Observe on Fig. 9 that voltage fluctuation at bus B3 is now reduced to +/- 0.7 %. The D-STATCOM compensates voltage by injecting a reactive current modulated at 5 Hz and varying between 0.6 pu capacitive when voltage is low and 0.6 pu inductive when voltage is high.

Conclusion

In this paper, D-STATCOM controller is derived by using synchronous reference theory. The model is simulated in MATLAB/SIMULINK platform and D-STATCOM controller's performance is evaluated using dq theory for voltage flicker mitigation. The controller is proven to be effective for flicker mitigation with improved dynamic response of the system and compensating reactive currents will help the mitigation of voltage flicker.

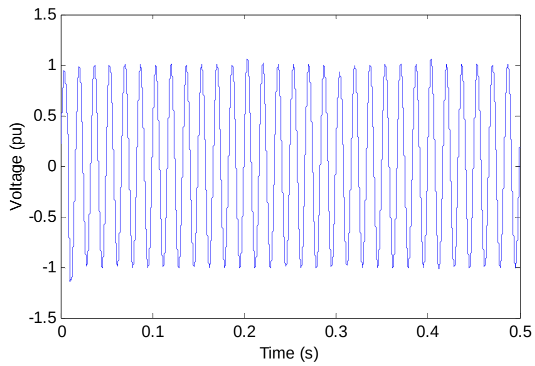

Fig. 3: Output voltage of D-STATCOM.

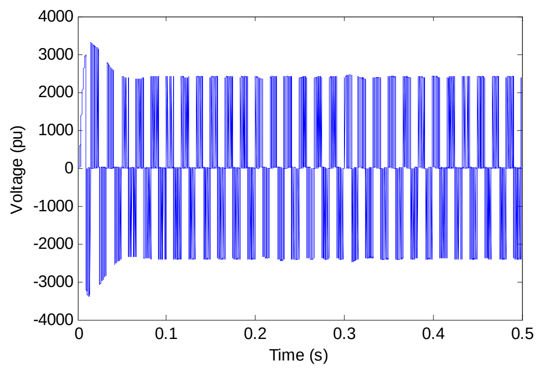

Fig. 4: Output voltage of voltage source inverter.

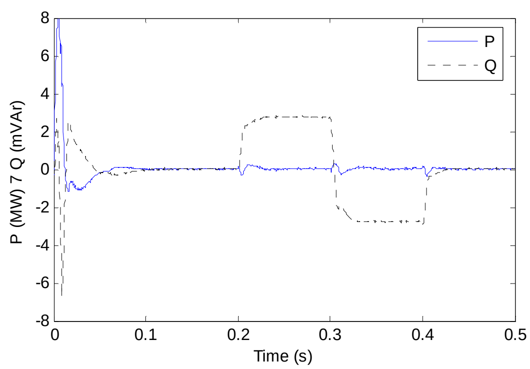

Fig. 5: Output P & Q of D-STATCOM.

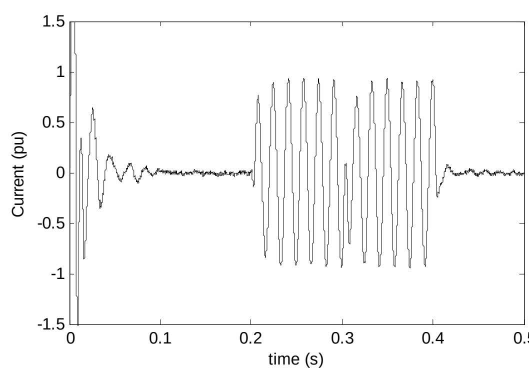

Fig. 6: Output current of D-STATCOM.

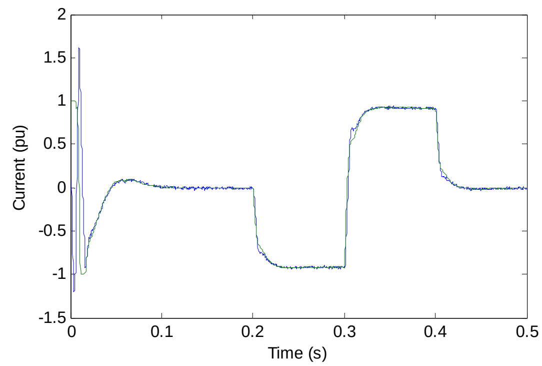

Fig. 7: I_q and I_{qref} of D-STATCOM.

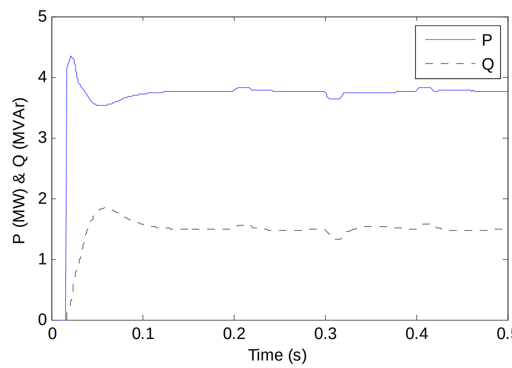

Fig. 8: P and Q of terminal B_3.

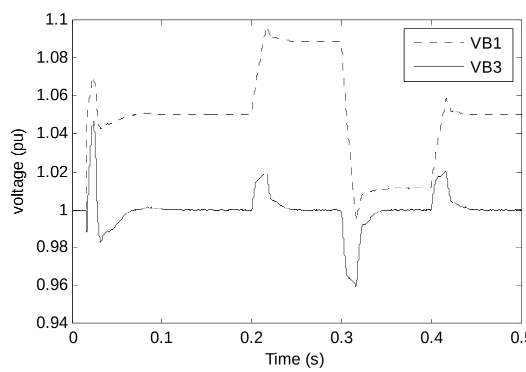

Fig. 9: Terminal voltages B_1 and B_3.

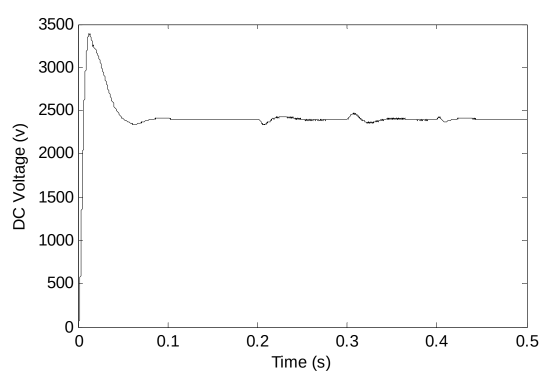

Fig. 10: Changes of DC voltage.

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