Cascade Cockcroft–Walton Voltage Multiplier Applied to Transformerless High Step-Up DC–DC Converter

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Abstract—**This paper proposes a high step-up dc-dc converter based on the Cockcroft-Walton (CW) voltage multiplier without a step-up transformer. Providing continuous input current with low ripple, high voltage ratio, and low voltage stress on the switches, diodes, and capacitors, the proposed converter is quite suitable for applying to low-input-level dc generation systems. Moreover, based on the n-stage CW voltage multiplier, the proposed converter can provide a suitable dc source for an $n+1$-level multilevel inverter. In this paper, the proposed control strategy employs two independent frequencies, one of which operates at high frequency to minimize the size of the inductor while the other one operates at relatively low frequency according to the desired output voltage ripple. A 200-W laboratory prototype is built for test, and both simulation and experimental results demonstrate the validity of the proposed converter.**

Index Terms—**Cockcroft–Walton (CW) voltage multiplier, high voltage ratio, multilevel inverter, step-up dc–dc converter.**

I. INTRODUCTION

IN RECENT YEARS, extensive use of electrical equipment has imposed severe demands for electrical energy, and this trend is constantly growing. Consequently, researchers and governments worldwide have made efforts on renewable energy applications for mitigating natural energy consumption and environmental concerns [1], [2]. Among various renewable energy sources, the photovoltaic (PV) cell and fuel cell have been considered attractive choices [3]–[5]. However, without extra arrangements, the output voltages generated from both of them are with rather low level [6], [7]. Thus, a high step-up dc-dc converter is desired in the power conversion systems corresponding to these two energy sources. In addition to the mentioned applications, a high step-up dc-dc converter is also required by many industrial applications, such as high-intensity discharge lamp ballasts for automobile headlamps and battery backup systems for uninterruptible power supplies [8].

Theoretically, the conventional boost dc-dc converter can provide a very high voltage gain by using an extremely high duty cycle. However, practically, parasitic elements associated with the inductor, capacitor, switch, and diode cannot be ignored, and their effects reduce the theoretical voltage gain [9]. Up to now, many step-up dc-dc converters have been proposed to obtain high voltage ratios without extremely high duty cycle by using isolated transformers or coupled inductors. Among these high step-up dc-dc converters, voltage-fed type sustains high input current ripple. Thus, providing low input current ripple and high voltage ratio, current-fed converters are generally superior to their counterparts. In [10], a traditional current-fed push–pull converter was presented to provide the aforementioned merit. However, in order to achieve high voltage gain, the leakage inductance of the transformer is relatively increased due to the high number of winding turns. Consequently, the switch is burdened with high voltage spikes across the switch at the turn-off instant. Thus, higher voltage-rating switches are required.

Some modified current-fed converters integrated step-up transformers [11]–[14] or coupled inductors [15]–[18], which focused on improving efficiency and reducing voltage stress, were presented to achieve high voltage gain without extremely high duty cycle. Most of them are associated with soft-switching or energy-regeneration techniques. However, the design of the high-frequency transformers, coupled inductors, or resonant components for these converters is relatively complex compared with the conventional boost dc-dc converter.

Some other alternative step-up dc-dc converters without step-up transformers and coupled inductors were presented in [19]–[24]. By cascading diode–capacitor or diode-inductor modules, these kinds of dc-dc converters provide not only high voltage gain but also simple and robust structures. Moreover, the control methods for conventional dc-dc converters can easily adapt to them. However, for most of these cascaded structures, the voltage stress on each individual switch and passive element depends on the number of stages. Fig. 1(a) shows an n-stage cascade boost converter proposed in [21] for obtaining a high voltage gain. However, the passive elements and switch sustained high voltage stress in this cascaded converter. Some other structures with switched-capacitor or switched-inductor circuits combined with basic transformerless topologies were proposed in [22]. Fig. 1(b) shows one of these topologies in
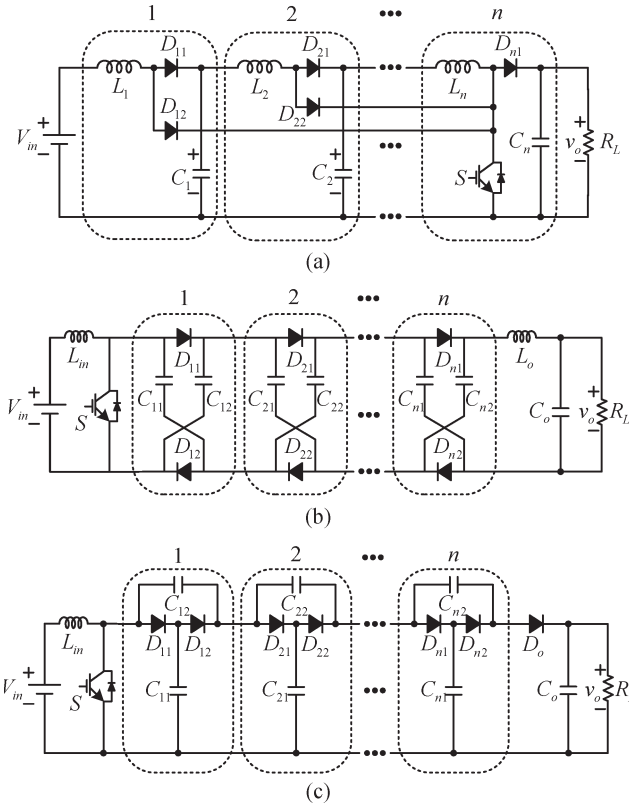
Fig. 1. Some cascaded dc-dc converters. (a) n cascade boost converter [21]. (b) Diode-capacitor n-stage step-up multiplier converter [23]. (c) Boost converter with cascade voltage multiplier cells [24].

Fig. 2. Proposed converter with n-stage CW voltage multiplier.

[22], which consists of a conventional boost converter and an n-stage diode–capacitor multiplier detailed in [23]. The main advantage of this topology is that higher voltage gain can easily be obtained by adding the stages of the diode-capacitor multipliers without modifying the main switch circuit. Nevertheless, the voltage across each capacitor in each switched-capacitor stage goes higher when a higher stage converter is used. Fig. 1(c) shows another similar topology proposed by Prudente *et al.* [24] which has advantages similar to that of the topology in [23]. However, the voltage stress on the capacitors of higher stage is still rather high. Moreover, in [24], a modified topology, with integrated interleaved multiphase boost converter and voltage multiplier, was proposed for high-power applications as well. In this topology, all capacitors in the voltage multiplier have identical voltage which is equal to $V_o/(n+1)$.

In the past few decades, high-voltage dc power supplies have been widely applied to industries, science, medicine, military, and, particularly, in test equipment, such as X-ray systems, dust filtering, insulating test, and electrostatic coating [25]–[27]. Providing the advantages of high voltage ratio, low voltage stress on the diodes and capacitors, compactness, and cost efficiency, the conventional Cockcroft-Walton (CW) voltage multiplier is very popular among high-voltage dc applications. However, the major drawback is that a high ripple voltage appears at the output when a low-frequency (50 or 60 Hz) utility source is used.

In this paper, a high step-up converter based on the CW voltage multiplier is proposed. Replacing the step-up transformer
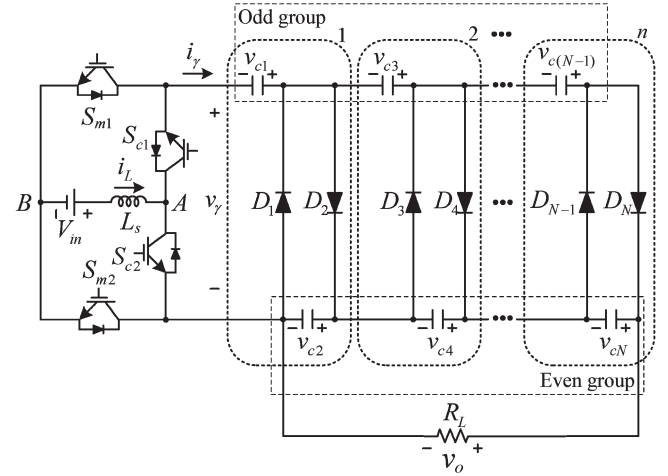
with the boost-type structure, the proposed converter provides higher voltage ratio than that of the conventional CW voltage multiplier. Thus, the proposed converter is suitable for power conversion applications where high voltage gains are desired. Moreover, the proposed converter operates in continuous conduction mode (CCM), so the switch stresses, the switching losses, and EMI noise can be reduced as well. The proposed converter deploys four switches, in which S_{c1} and S_{c2} are used to generate an alternating source to feed into the CW voltage multiplier and S_{m1} and S_{m2} are used to control the inductor energy to obtain a boost performance. This will increase the complexity and cost of the proposed converter because an isolated circuit is necessary to drive the power semiconductor switches. Nevertheless, the proposed converter still demonstrates some special features: 1) The four switches operate at two independent frequencies, which provide coordination between the output ripple and system efficiency; 2) with same voltage level, the number of semiconductors in the proposed converter is competing with some cascaded dc-dc converters [21], [23], [24]; 3) the dc output formed by series capacitors is suitable for powering multilevel inverters; and 4) the proposed converter can adapt to an ac–dc converter with the same topology, and that will be a future work of this paper.

In Section II, the mathematical model, circuit operation principle, and the ideal static gain will be derived and discussed. The design considerations will be introduced in Section III, and some comparisons between the proposed converter and the other topologies will be made in this section as well. In Section IV, the control strategy of the proposed converter will be described. In Section V, a prototype with 200-W rating is built, and both simulation and experimental results are displayed for verification. Finally, some conclusions are given in Section VI.

II. STEADY-STATE ANALYSIS OF PROPOSED CONVERTER

Fig. 2 shows the proposed converter, which is supplied by a low-level dc source, such as battery, PV module, or fuel cell sources. The proposed converter consists of one boost
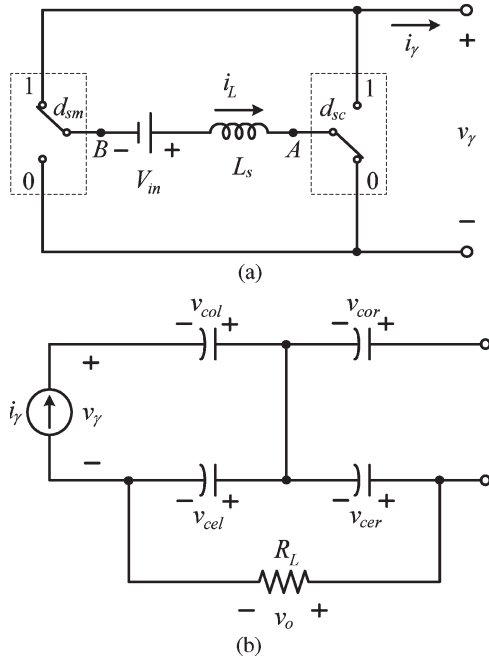
Fig. 3. Equivalent circuit of the proposed converter. (a) Source-side part. (b) Load-side part.

TABLE I
CONDUCTING STATES OF FOUR SWITCHES

Conducting states		Strategy I	Strategy II
d_{sc}	d_{sm}	$S_{c1}, S_{c2}, S_{m1}, S_{m2}$	
0	0	0101	0111
0	1	0110	0110
1	1	1010	1011
1	0	1001	1001
1 or 0	1 or 0	-	1111
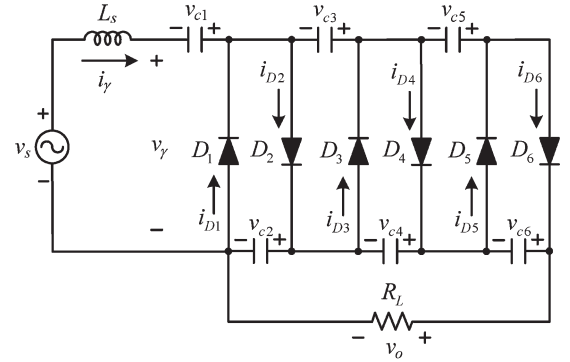
Fig. 4. Current-fed three-stage CW voltage multiplier circuit.

inductor L_s, four switches (S_{m1}, S_{m2}, S_{c1}, and S_{c2}), and one n-stage CW voltage multiplier. $S_{m1}(S_{c1})$ and $S_{m2}(S_{c2})$ operate in complementary mode, and the operating frequencies of S_{m1} and S_{c1} are defined as f_{sm} and f_{sc}, respectively. For convenience, f_{sm} is denoted as modulation frequency, and f_{sc} is denoted as alternating frequency. Theoretically, these two frequencies should be as high as possible so that smaller inductor and capacitors can be used in this circuit. In this paper, f_{sm} is set much higher than f_{sc}, and the output voltage is regulated by controlling the duty cycle of S_{m1} and S_{m2}, while the output voltage ripple can be adjusted by f_{sc}. As shown in Fig. 2, the well-known CW voltage multiplier is constructed by a cascade of stages with each stage containing two capacitors and two diodes. In an n-stage CW voltage multiplier, there are $N(=2n)$ capacitors and N diodes. For convenience, both capacitors and diodes are divided into odd group and even group according to their suffixes, as denoted in Fig. 2.

A. Mathematical Model

As shown in Fig. 2, the proposed converter is an integration of a boost converter with a CW voltage multiplier. For analysis, the equivalent circuit of the proposed converter can be divided into source-side and load-side parts as shown in Fig. 3(a) and (b), respectively. For the source-side part, the conducting states d_{sc} and d_{sm} are defined in Table I, where strategy I does not include safe commutation and strategy II includes safe commutation.

According to the conducting states d_{sc} and d_{sm}, the differential equation of the inductor current is given by

$$\frac{di_L}{dt} = \frac{1}{L_s}\left[V_{in} - (d_{sc} - d_{sm}) \cdot v_\gamma\right] \tag{1}$$

where V_{in} is the input voltage, i_L is the input current, and v_γ is the terminal voltage of the CW voltage multiplier. Assuming that the converter operates in CCM, the current i_γ flowing into the CW voltage multiplier depends on d_{sm} and d_{sc} and can be expressed as

$$i_\gamma = (d_{sc} - d_{sm}) \cdot i_L \tag{2}$$

where the current i_γ can be deemed a pulse-form current source.

In [28], the mathematical model of an n-stage CW voltage multiplier was discussed and simplified the equivalent circuit, which was convenient for simulation work. Thus, according to the analysis in [28], the circuit behavior of the load-side part (CW voltage multiplier) will be detailed in the following.

For convenience, a current-fed three-stage CW voltage multiplier energized by a sinusoidal ac source with line frequency, as shown in Fig. 4, is used to analyze the steady-state behavior of the CW circuit through simulation. Obviously, one inductor is connected between the ac source and the CW voltage multiplier for smoothing the current i_γ. Fig. 5 shows the waveforms of capacitor voltages $v_{c1}-v_{c6}$, line voltage v_s, terminal voltage v_γ and current i_γ, and diode currents $i_{D1}-i_{D6}$ over one line cycle, where time interval t_0-t_5 ($t_0'-t_5'$) is the positive (negative) half cycle. It can be seen from Fig. 5, during positive half cycle, that only one of the even diodes is conducted with the sequence D_6, D_4, and D_2 and that the even (odd) capacitors are charged (discharged) through the conducting diodes. Similar behavior occurs during the negative half cycle, while the odd diodes are conducted with the sequence D_5, D_3, and D_1, and the odd (even) capacitors are charged (discharged).
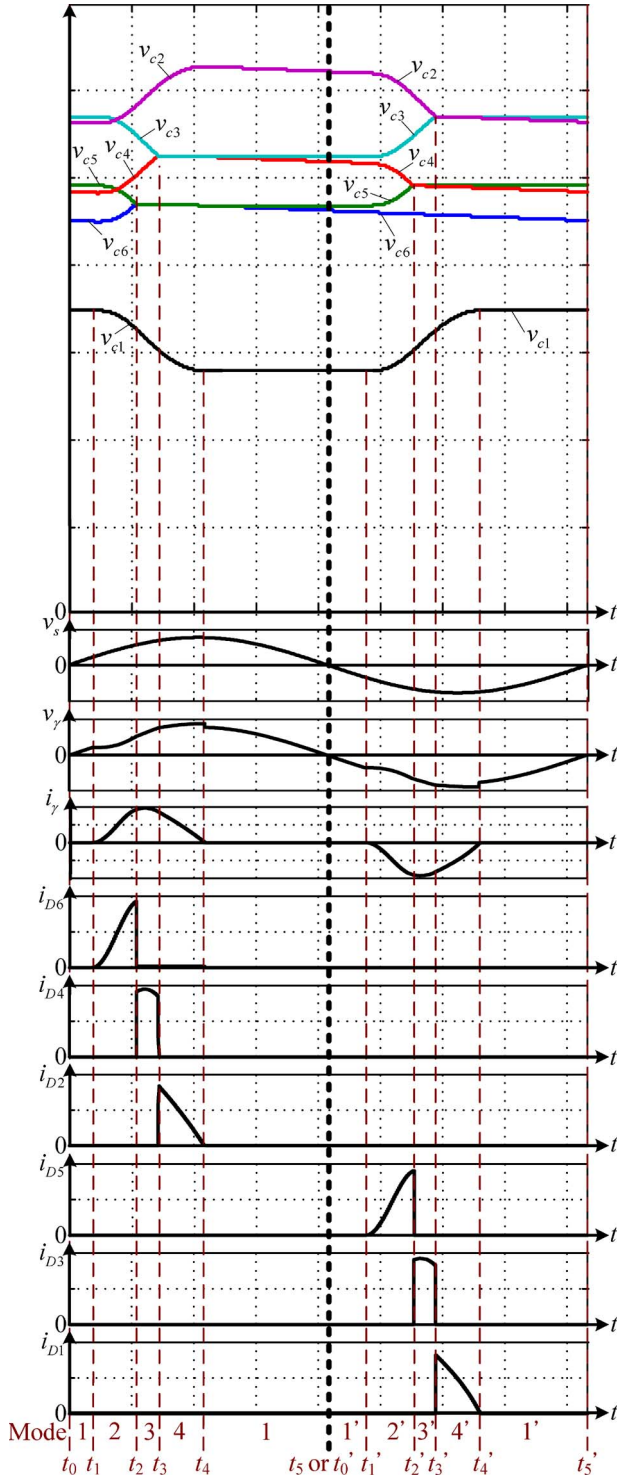
Fig. 5. Simulated waveforms of capacitor voltages $v_{C1} - v_{C6}$, input line voltage v_s, input terminal voltage v_γ and current i_γ, and diode currents $i_{D1} - i_{D6}$ for a current-fed three-stage CW circuit over one line cycle.

In the positive (negative) half cycle, there are four circuit modes, denoted as mode 1 (mode 1') to mode 4 (mode 4'), and Fig. 6(a)–(d) [Fig. 6(e)–(h)] shows the corresponding conducting paths, where an equivalent alternating current source i_γ is fed into the CW voltage multiplier. According to these modes, the capacitor voltages and conducting condition of diodes will

be discussed. The characteristic behavior of each mode in the positive half cycle is presented as follows.

Mode 1: During time intervals t_0-t_1 and t_4-t_5, i_γ is zero, and all diodes are not conducted. As shown in Fig. 6(a), even capacitors C_6, C_4, and C_2 supply the load, while odd capacitors C_5, C_3, and C_1 are floating.

Mode 2: During time interval t_1-t_2, i_γ is positive, and only D_6 is conducting. From Fig. 6(b), all even capacitors C_6, C_4, and C_2 are charged, while all odd capacitors C_5, C_3, and C_1 are discharged by i_γ. Moreover, from Fig. 5, it can be found that the conducting condition of D_6 is ($i_\gamma > 0$) and ($v_{c5} > v_{c6}$) and ($v_{c3} > v_{c4}$).

Mode 3: During time interval t_2-t_3, i_γ is positive, and only D_4 is conducting. From Fig. 6(c), C_4 and C_2 are charged, while C_3 and C_1 are discharged by i_γ. Simultaneously, C_6 supplies load current, and C_5 is floating. From Fig. 5, it can be found that the conducting condition of D_4 is ($i_\gamma > 0$) and ($v_{c5} \leqq v_{c6}$) and ($v_{c3} > v_{c4}$).

Mode 4: During time interval t_3-t_4, i_γ is positive, and only D_2 is conducting. From Fig. 6(d), C_2 is charged, while C_1 is discharged by i_γ. Simultaneously, C_6 and C_4 supply load current, while C_5 and C_3 are floating. From Fig. 5, it can be found that the conducting condition of D_2 is ($i_\gamma > 0$) and ($v_{c5} \leqq v_{c6}$) and ($v_{c3} \leqq v_{c4}$).

The behavior of the CW circuit during the negative half cycle can be obtained through a similar process.

From the circuit behavior, three diode conducting phenomena are found as follow: 1) Only one of the diodes in the CW circuit will conduct when $i_\gamma \neq 0$; 2) the sequence of conducting diode is from right side to left side with even diodes conducting in positive half cycle and odd diodes conducting in negative half cycle; and 3) the conduction condition of each diode is determined by the terminal current i_γ and capacitor voltages $v_{c1} - v_{c6}$. Consequently, a variable S_D for an n-stage CW voltage multiplier is used to indicate the diode conduction state and is given by

$$S_D = \max\{x_k\} \quad \text{for} \begin{cases} i_\gamma = 0, k = 0 \\ i_\gamma > 0, k = 2, 4, \ldots, 2n \\ i_\gamma < 0, k = 1, 3, \ldots, 2n-1 \end{cases} \quad (3)$$

where S_D is an integer with values from 0 to $2n$ and denoted as diode-conducting index, for example, when $S_D = 0$ represents that all diodes are not conducted and when $S_D = 6$ represents that the diode D_6 is conducted; $\{x_k\}$ is a set of diode-conducting indices used to determine S_D; and k is an integer determined by i_γ. When $i_\gamma = 0$, either in positive or negative half cycles, we have $k = 0$, $x_0 = 0$, and $\{x_k\} = \{0\}$. Thus, $S_D = 0$ represents that all diodes are not conducted. When $i_\gamma > 0$ in positive half cycle, we have $k = 2, 4, \ldots, 2n$, and x_k can be determined by

$$x_k = \begin{cases} k, & \text{for } k \leq 2 \\ k, & \text{for } k > 2 \text{ and } v_{c(k-1)} > v_{c(k)} \\ 0, & \text{for } k > 2 \text{ and } v_{c(k-1)} \leq v_{c(k)} \end{cases} \quad (4)$$

where $v_{c(k)}$ is the voltage of the kth capacitor and will be given later. Because only one of the even diodes is able to
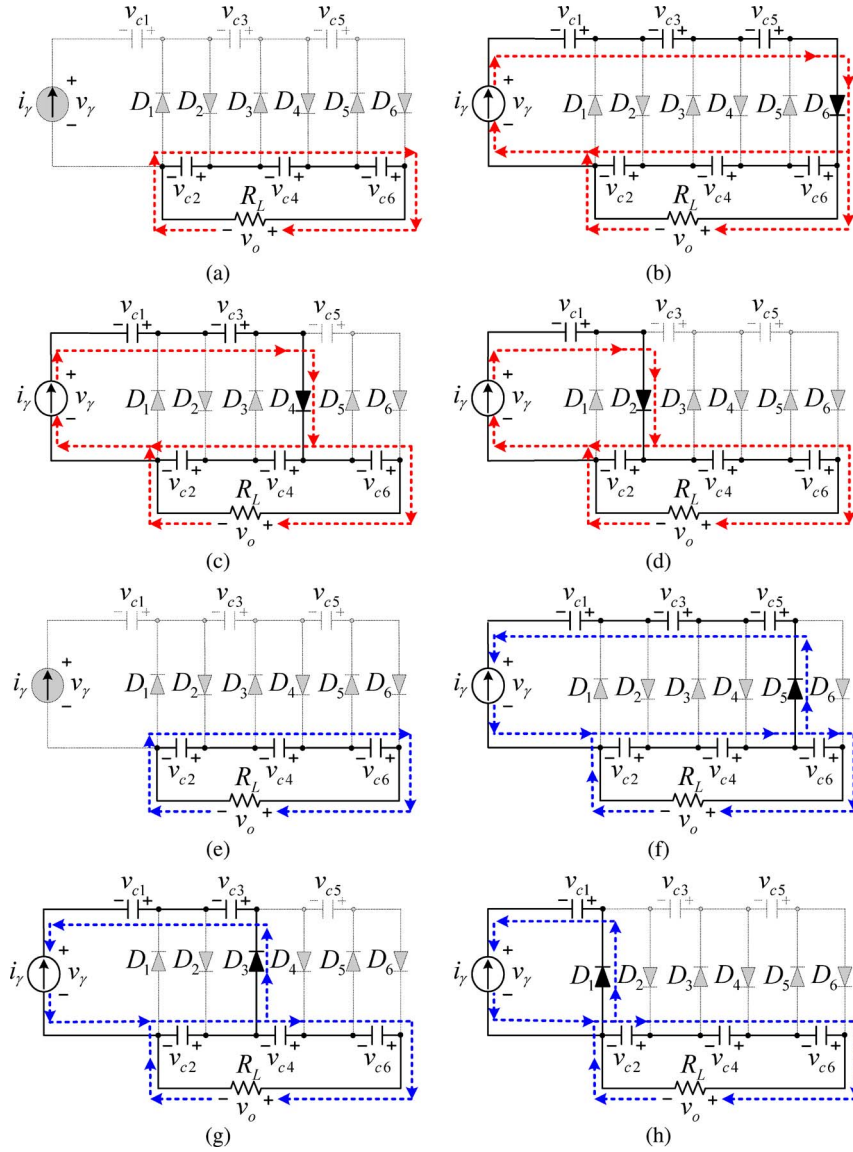
Fig. 6. Circuit conducting paths of three-stage CW voltage multiplier over one line cycle. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 1′. (f) Mode 2′. (g) Mode 3′. (h) Mode 4′.

conduct during the positive half cycle, there are n possibilities of conducting states. Consequently, the elements of $\{x_k\}$ can be determined by (4), and the element with maximum value will be chosen for S_D. This maximum value represents the number of the diode that is conducting. Similarly, the conducting states for $i_\gamma < 0$ during the negative half cycle can be obtained.

According to the operation modes shown in Fig. 6, the configurations of capacitors are dependent on diode-conducting states. Consequently, two variables corresponding to the charging behavior of even and odd capacitors are introduced and given by

$$EC_i = \begin{cases} 0, & S_D < i \\ 1, & S_D \geq i \end{cases} \quad \text{for } i = 2, 4, \ldots, 2n \quad (5)$$

$$OC_j = \begin{cases} 0, & S_D < j \\ 1, & S_D \geq j \end{cases} \quad \text{for } j = 1, 3, \ldots, 2n - 1 \quad (6)$$

where EC_i and OC_j are the charging indices for the ith even capacitor and jth odd capacitor, respectively. $EC_i = 1$ ($OC_j = 1$) represents that the ith even capacitor (the jth odd capacitor) is located in the left side of the conducting diode, while $EC_i = 0$ ($OC_j = 0$) represents that the ith even capacitor (the jth odd capacitor) is located in the right side of the conducting diode. For example, for a three-stage CW voltage multiplier, $S_D = 4$ represents that the diode D_4 is conducting and EC_6 and OC_5 are equal to zero while the others are equal to one. Therefore, the capacitors C_6 and C_5 are located in the right side of conducting diode D_4, and the others are located in the left side, as shown in Fig. 6(c). However, when $S_D = 0$ ($i_\gamma = 0$), all EC_i and OC_j are equal to zero, the even-group capacitors supply the load, and the odd-group capacitors are floating, as shown in Fig. 6(a) and (e).

With the help of these two variables, for an n-stage CW voltage multiplier, the capacitors can be divided into four parts,

and the equivalent series voltages of them are given by

$$v_{\text{cel}} = \sum_{i=2,4,\ldots}^{2n} EC_i \cdot v_{ci} \tag{7}$$

$$v_{\text{col}} = \sum_{j=1,3,\ldots}^{2n-1} OC_j \cdot v_{cj} \tag{8}$$

$$v_{\text{cer}} = \sum_{i=2,4,\ldots}^{2n} (1 - EC_i) \cdot v_{ci} \tag{9}$$

$$v_{\text{cor}} = \sum_{j=1,3,\ldots}^{2n-1} (1 - OC_j) \cdot v_{cj} \tag{10}$$

where v_{cel} (v_{col}) represents the series voltage of even (odd) capacitors that are on the left side of the conducting diode, v_{cer} (v_{cor}) represents the series voltage of even (odd) capacitors that are on the right side of the conducting diode, and $v_{ci}(v_{cj})$ is the voltage of the ith even capacitor (the jth odd capacitor). Fig. 3(b) shows the capacitor configuration corresponding to the conducting diode (S_D). From Fig. 3(b), v_γ and v_o can be expressed, respectively as

$$v_\gamma = v_{\text{cel}} - v_{\text{col}} \tag{11}$$

$$v_o = v_{\text{cel}} + v_{\text{cer}}. \tag{12}$$

Finally, according to (2), (5), (6), and (12), the current equations of each even and each odd capacitor are given by

$$\frac{dv_{ci}}{dt} = \frac{1}{C_i} \left(EC_i \cdot i_\gamma - \frac{v_o}{R_L} \right) \qquad \text{for } i = 2, 4, \ldots, 2n \tag{13}$$

$$\frac{dv_{cj}}{dt} = \frac{-1}{C_j} (OC_j \cdot i_\gamma) \qquad \text{for } j = 1, 3, \ldots, 2n-1 \tag{14}$$

where C_i is the capacitance of the ith even capacitor and C_j is the capacitance of the jth odd capacitor. As shown in (13) and (14), the states of EC_i (OC_j) determine the charge–discharge behavior of the ith even capacitor (the jth odd capacitor).

From above, one conclusion can be made that, during one line cycle, each diode conducts equal average current due to equality of energy transferring with the sequence $D_6 - D_4 - D_2 - D_5 - D_3 - D_1$, as shown in Fig. 5. Although the proposed converter and the conventional CW voltage multiplier have different equivalent current i_γ, this conclusion is still available. Finally, the mathematical model of the proposed converter described in this section can be used for simulation.

B. Circuit Operation Principle

In order to simplify the analysis of circuit operation, the proposed converter with a three-stage CW voltage multiplier, as shown in Fig. 7, is used. Before analyzing, some assumptions are made as follows.

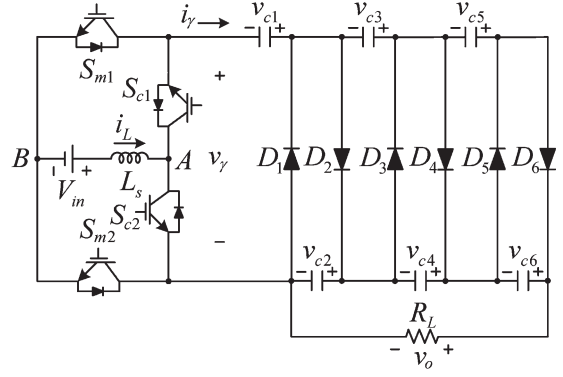1) All of the circuit elements are ideal, and there is no power loss in the system.

Fig. 7. Proposed converter with three-stage CW voltage multiplier.

2) When a high-frequency periodic alternating current is fed into the CW circuit and all of the capacitors in the CW voltage multiplier are sufficiently large, the voltage drop and ripple of each capacitor voltage can be ignored under a reasonable load condition. Thus, the voltages across all capacitors are equal, except the first capacitor whose voltage is one half of the others.

3) The proposed converter is operating in CCM and in the steady-state condition.

4) When the inductor transfers the storage energy to the CW circuit, only one of the diodes in the CW circuit will be conducted.

5) Some safe commutation states are ignored.

According to the second assumption, each capacitor voltage in the CW voltage multiplier can be defined as

$$v_{ck} = \begin{cases} V_c/2 & \text{for } k = 1 \\ V_c & \text{for } k = 2, 3, \ldots, N \end{cases} \tag{15}$$

where v_{ck} is the voltage of the kth capacitor and V_c is the steady-state voltage of $v_{c2} - v_{cN}$.

For an n-stage CW voltage multiplier, the output voltage is equal to the total voltage of all even capacitors, which can be expressed as

$$V_o = nV_c. \tag{16}$$

Substituting (16) into (15), each capacitor voltage in an n-stage CW voltage multiplier can also be expressed as

$$v_{ck} = \begin{cases} V_o/2n & \text{for } k = 1 \\ V_o/n & \text{for } k = 2, 3, \ldots, N \end{cases} \tag{17}$$

where V_o is the steady-state voltage of the output load side.

Fig. 8 shows the theoretical waveforms of the proposed converter, including switching signals, inductor current, v_γ, i_γ, and diode currents. According to the polarity of i_γ, the operation of the proposed converter can be divided into two parts: positive conducting interval $[t_0, t_1]$ for $i_\gamma \geqq 0$ and negative conducting interval $[t_1, t_2]$ for $i_\gamma \leqq 0$. During positive conducting
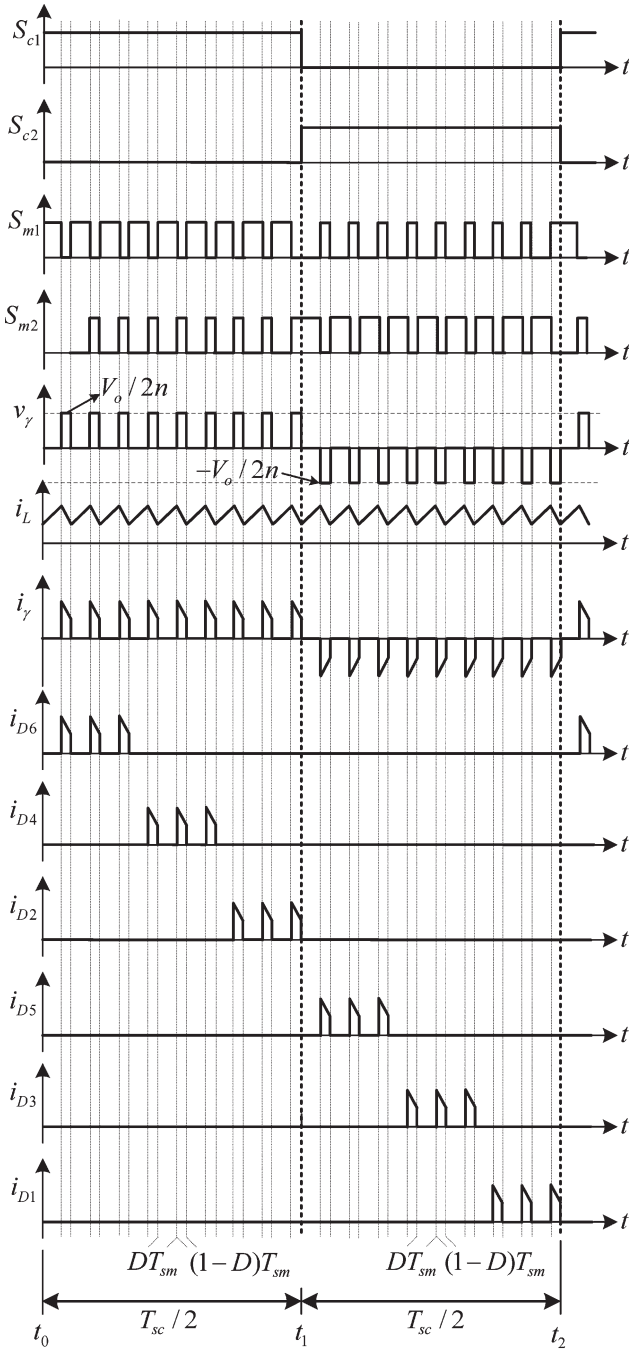
Fig. 8. Ideal waveforms of the proposed converter in CCM.

interval, only one of the even diodes can conduct with the sequence $D_6-D_4-D_2$, while during negative conducting interval, only one of the odd diodes can conduct with the sequence $D_5-D_3-D_1$. Moreover, during positive conducting interval, there are four circuit states, as shown in Fig. 9(a)–(d), denoted as states I, II-A, II-B, and II-C. In state I, S_{m1} turns on; thus, the energy stored in the inductor increases. In states II-A, II-B, and II-C, S_{m2} turns on, and the inductor transfers energy to the CW circuit through D_6, D_4, and D_2, respectively. Similarly, there are four circuit states in the negative conducting interval, as shown in Fig. 9(e)–(h), denoted as states III, IV-A, IV-B, and IV-C. According to Fig. 9, the circuit operation

principle of the proposed converter is illustrated in detail as follows.

1) State I: S_{m1} and S_{c1} are turned on, and S_{m2}, S_{c2}, and all CW diodes are turned off, as shown in Fig. 9(a). The boost inductor is charged by the input dc source, the even-group capacitors C_6, C_4, and C_2 supply the load, and the odd-group capacitors C_5, C_3, and C_1 are floating.

2) State II: S_{m2} and S_{c1} are turned on, S_{m1} and S_{c2} are turned off, and the current i_γ is positive. The boost inductor and input dc source transfer energy to the CW voltage multiplier through different even diodes, as shown in Fig. 9(b)–(d). In Fig. 9(b), state II-A, D_6 is conducting; thus, the even-group capacitors C_6, C_4, and C_2 are charged, and the odd-group capacitors C_5, C_3, and C_1 are discharged by i_γ. In Fig. 9(c), state II-B, D_4 is conducting. Thus, C_4 and C_2 are charged, C_3 and C_1 are discharged by i_γ, C_6 supplies load current, and C_5 is floating. In Fig. 9(d), state II-C, D_2 is conducting. Thus, C_2 is charged, C_1 is discharged by i_γ, C_6 and C_4 supply load current, and C_5 and C_3 are floating.

3) State III: S_{m2} and S_{c2} are turned on, and S_{m1}, S_{c1}, and all CW diodes are turned off, as shown in Fig. 9(e). The boost inductor is charged by the input dc source, the even-group capacitors C_6, C_4, and C_2 supply the load, and the odd-group capacitors C_5, C_3, and C_1 are floating.

4) State IV: S_{m1} and S_{c2} are turned on, S_{m2} and S_{c1} are turned off, and the current i_γ is negative. The boost inductor and input dc source transfer energy to the CW voltage multiplier through different odd diodes, as shown in Fig. 9(f)–(h). In Fig. 9(f), state IV-A, D_5 is conducting. Thus, the even-group capacitors, except C_6 which supplies load current, are discharged, and the odd-group capacitors C_5, C_3, and C_1 are charged by i_γ. In Fig. 9(g), state IV-B, D_3 is conducting. Thus, C_2 is discharged, C_3 and C_1 are charged by i_γ, C_6 and C_4 supply load current, and C_5 is floating. In Fig. 9(h), state IV-C, D_1 is conducting. Thus, C_1 is charged by i_γ, all even capacitors supply load current, and C_5 and C_3 are floating.

C. Derivation of the Ideal Static Gain

From Fig. 9 and (17), it can be seen that the terminal voltage of the CW circuit $V_{AB} = 0$ in states I and III, while in states II and IV, $V_{AB} = V_o/2n$. The inductor current variation, during interval $0 < t < DT_{sm}$, can be represented as

$$\Delta i_L = \frac{V_{in}}{L_s} DT_{sm} \tag{18}$$

where V_{in} is the input voltage, L_s is the boost inductor, and D is the duty cycle of the switch $S_{m1}(S_{m2})$ in the positive (negative) conducting interval over one modulation switching period $T_{sm} = 1/f_{sm}$. Then, during interval $DT_{sm} < t < (1-D)T_{sm}$, the inductor current variation can be represented as

$$\Delta i_L = \frac{V_{in} - V_o/2n}{L_s}(1-D)T_{sm}. \tag{19}$$

Under the steady-state condition, by the volt–second balance principle, the voltage gain of the proposed converter can be
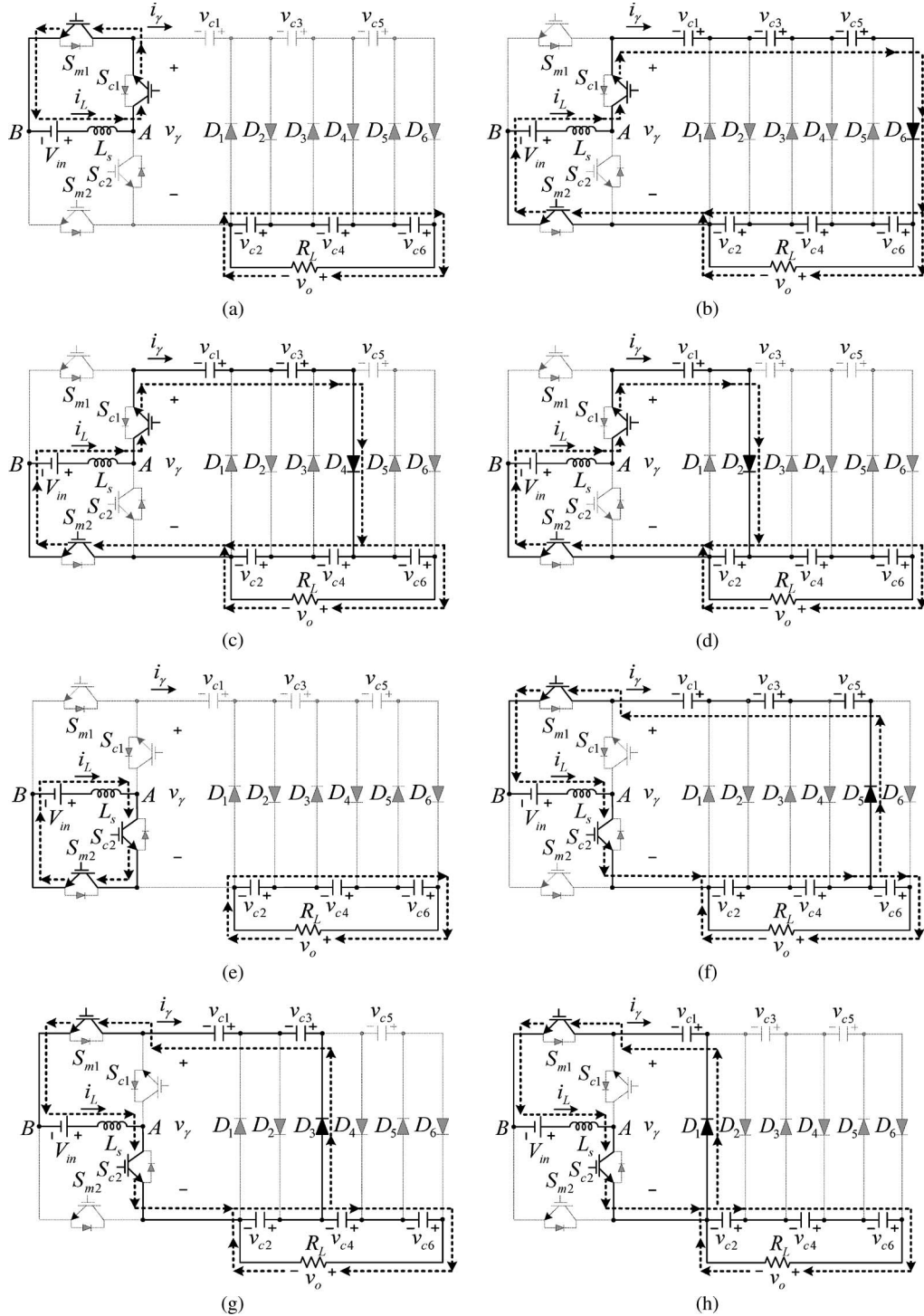
Fig. 9. Conducting paths of proposed converter. (a) State I. (b) State II-A. (c) State II-B. (d) State II-C. (e) State III. (f) State IV-A. (g) State IV-B. (h) State IV-C.

derived from (18) and (19) as

$$M_V = \frac{V_o}{V_{\text{in}}} = \frac{2n}{1-D} \qquad (20)$$

where M_V represents the static voltage gain of the proposed converter. Moreover, the relationship between i_γ and i_L can be obtained by $|i_\gamma|/i_L = 1 - D$.

The relationship between voltage gain and duty cycle for the proposed converter under $n = 1-8$ and the classic boost

dc-dc converter is shown in Fig. 10. Obviously, the proposed converter provides high voltage gain without extremely high duty cycle, while the classic boost dc-dc converter is operating at extremely high duty cycle.

III. DESIGN CONSIDERATIONS OF PROPOSED CONVERTER

In this section, the voltage and current stresses on each capacitor, switch, and diode will be considered. Moreover, the values of inductor and capacitors will be discussed as well.
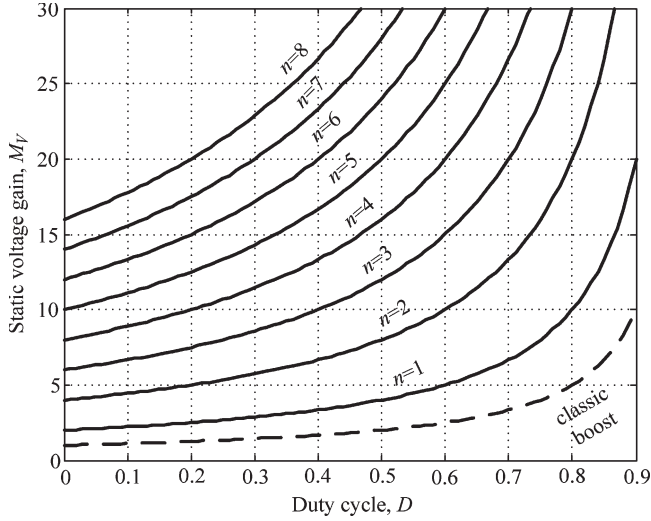
Fig. 10.   Voltage gain versus duty cycle for the proposed converter under $n = 1-8$ and the classic boost dc-dc converter.

A. Capacitor Voltage Stress

In the steady-state condition, assuming that all capacitors are large enough, then, each capacitor in an n-stage CW voltage multiplier, theoretically, has the same voltage except the first one, which has one half of the others. As a result, the maximum voltage stress on each capacitor, as shown in (17), is $V_{o,\mathrm{pk}}/n$, except that the first one is $V_{o,\mathrm{pk}}/2n$, where $V_{o,\mathrm{pk}}$ is the maximum peak value of the output voltage. For comparison, the voltage stress on each capacitor corresponding to the high step-up converters shown in Fig. 1 is summarized in the secondary row of Table II. It can be seen that the capacitor voltage of the proposed converter only depends on the input voltage and duty cycle while the capacitor voltages of the others are dependent on the number of the cascade stages. Thus, the determination of the capacitor rating is easier for the proposed converter.

B. Switch Voltage and Current Stresses

From Fig. 9, the maximum current and voltage stresses on the switches are I_{pk} and $V_{o,\mathrm{pk}}/2n$, respectively, where I_{pk} is the maximum peak value of input current. For comparison, the voltage stress of the switches in the proposed converter and other topologies is listed in the fourth row of Table II. Except the switch in the converter shown in Fig. 1(a), which burdens the overall output voltage, the voltage stress of the switches in the rest of the converters is similar to that of the conventional boost converters.

C. Diode Voltage and Current Stresses

Similarly, the maximum current and voltage stresses on the diodes in the proposed converter are I_{pk} and $V_{o,\mathrm{pk}}/n$, respectively. The voltage stress of the diodes is twice as large as that of the switches. The fifth row in Table II demonstrates the voltage stress on the diodes in the proposed converter and other topologies.

D. Input Inductance

The value of the boost inductor can be calculated by

$$L_s = V_{\mathrm{in}} \frac{D T_{\mathrm{sm}}}{K_I I_{\mathrm{pk}}} \qquad (21)$$

where K_I is the expecting percentage of the maximum peak-to-peak current ripple in the inductor.

E. Capacitance of CW Voltage Multiplier

A major advantage of the conventional CW voltage multiplier is that the voltage gain is theoretically proportional to the number of cascaded stages. In the previous section, the ideal voltage gain (unloaded) is assumed to simplify the circuit analysis. Unfortunately, when a load is connected to the load side of the system, the voltage drop and ripple across each capacitor cannot be ignored. Voltage-fed mode, in which the input terminal of the CW voltage multiplier was fed by a sinusoidal voltage source, was used for analyzing voltage drop and ripple for CW multipliers in most literatures [25]–[27], [29]–[31], while only few literatures discussed current-fed mode [32], [33]. In this paper, for analyzing the voltage drop and ripple, an equivalent discontinuous-pulse-type current source is fed into the CW voltage multiplier. According to the current-fed mode analytical principle presented in [32], the voltage drop and ripple associated with each capacitor can be found by the charge–discharge behavior of capacitors under the steady-state condition, as shown in Fig. 5.

Based on the current-fed analysis method, the voltage ripple of each capacitor of the proposed converter can be derived as

$$\delta V_{ci} = \frac{I_o}{f_{\mathrm{sc}} \cdot C} \times \left(\frac{2n-i+1}{2} \right) \qquad \text{for } i = 1, 2, \ldots, 2n \qquad (22)$$

where I_o is the average load current, f_{sc} is the alternating frequency, C is the capacitance values of all capacitors (all capacitors are identical), and n is the number of stages.

As shown in Fig. 2, it can be known that the output voltage ripple of the proposed converter is equal to the sum of all even capacitor voltage ripples; thus, by (22), the output voltage ripple can be expressed as

$$\delta V_o = \sum_{i=2,4,\ldots}^{2n} \delta V_{ci} = \frac{1}{2} \cdot \frac{I_o \cdot n^2}{f_{\mathrm{sc}} \cdot C}. \qquad (23)$$

Furthermore, the maximum voltage of each capacitor, except the first and second capacitors, can also be derived as

$$V_{ci(\mathrm{max})}$$

$$= V_{c(i-1)(\mathrm{max})}$$

$$- \frac{I_o}{f_{\mathrm{sc}} \cdot C} \times \begin{cases} \left(\frac{2n^2 - (i-2) \cdot n - 1}{2n} \right) & \text{for } i = 3, 5, \ldots, 2n-1 \\ \left(\frac{2n^2 - (i-2) \cdot n}{2n} \right) & \text{for } i = 4, 6, \ldots, 2n. \end{cases} \qquad (24)$$

TABLE II
COMPARISON OF TOPOLOGIES

	Proposed converter	Converter shown in Fig. 1(a)	Converter shown in Fig. 1(b)	Converter shown in Fig. 1(c)
Voltage gain	$M_V = \dfrac{2n}{1-D}$	$M_V = \left(\dfrac{1}{1-D}\right)^n$	$M_V = \begin{cases} \dfrac{n+D}{1-D} & ,n = \text{odd} \\ \dfrac{n+1-D}{1-D} & ,n = \text{even} \end{cases}$	$M_V = \dfrac{n+1}{1-D}$
Capacitor voltage	$V_{Ck} = \begin{cases} \dfrac{V_{in}}{1-D} & \text{for } k=1 \\ \dfrac{2V_{in}}{1-D} & \text{for } k=2,...,2n \end{cases}$	$V_{Ck} = V_{in}\left(\dfrac{1}{1-D}\right)^k$ for $k=1,...,n$	$V_{Ck1} = V_{Ck2} = \dfrac{kV_{in}}{1-D}$ for $k=1,...,n$	$\begin{cases} V_{Ck1} = \dfrac{kV_{in}}{1-D} \\ V_{Ck2} = \dfrac{V_{in}}{1-D} \end{cases}$ for $k=1,...,n$
Elements number	$N_{\text{total}} = 5+4n$	$N_{\text{total}} = 4n$	$N_{\text{total}} = 4+4n$	$N_{\text{total}} = 4+4n$
Switch voltage	$\dfrac{V_{in}}{1-D}$	$V_{in}\left(\dfrac{1}{1-D}\right)^n$	$\dfrac{V_{in}}{1-D}$	$\dfrac{V_{in}}{1-D}$
Diode voltage	$\dfrac{2V_{in}}{1-D}$	$\begin{cases} V_{Dk1} = V_{Ck} & \text{for } k=1,...,n \\ V_{Dk2} = V_{Cn} - V_{Ck} & \text{for } k=1,...,n-1 \end{cases}$	$\dfrac{V_{in}}{1-D}$	$\dfrac{V_{in}}{1-D}$

From (24), it can be found that the maximum voltage of the ith capacitor $(i = 3, \ldots, 2n)$ is dependent on the maximum voltage of the second capacitor with a voltage drop; thus, (24) can be represented as

$$
\begin{aligned}
&V_{ci(\max)} \\
&= V_{c2(\max)} \\
&\quad - \frac{I_o}{f_{\text{sc}} \cdot C} \times \left\{ \sum_{k=1}^{\lfloor (i-1)/2 \rfloor} \frac{2n^2 - (2k-1)\cdot n - 1}{2n} \right. \\
&\qquad\qquad\qquad \left. + \sum_{h=1}^{\lfloor (i-2)/2 \rfloor} \frac{2n^2 - (2h)\cdot n}{2n} \right\} \\
&\qquad\qquad\qquad\qquad\qquad \text{for } i = 3, 4, \ldots, 2n \quad (25)
\end{aligned}
$$

where $\lfloor X \rfloor$ is the largest integer and not greater than X.

Before applying (25), the maximum voltage of the second capacitor has to be obtained first. For a CW voltage multiplier, the average output voltage is equal to the sum of average voltages of all even capacitors and can be expressed as

$$
V_o = \sum_{i=2,4,...}^{2n} V_{ci} = \sum_{i=2,4,...}^{2n} \left(V_{ci(\max)} - \delta V_{ci}/2 \right). \quad (26)
$$

Assuming that the average output voltage V_o is regulated through a closed-loop controller and substituting (22) and (25) into (26), the maximum voltage of the second capacitor can be estimated as

$$
\begin{aligned}
&V_{c2(\max)} \\
&= \frac{1}{n} \left\{ V_o + \frac{I_o}{f_{\text{sc}} \cdot C} \right. \\
&\quad \left. \times \left[\sum_{i=2,4,...}^{2n} \frac{2n-i+1}{4} \right.\right. \\
&\qquad \left.\left. + \sum_{i=4,6,...}^{2n} \sum_{k=1}^{(i-2)/2} \frac{4n^2 - (4k-1)\cdot n - 1}{2n} \right] \right\}. \quad (27)
\end{aligned}
$$

To simplify the calculation of $V_{c2(\max)}$, (27) can be expressed as

$$
V_{c2(\max)} = \frac{V_o}{n} + \frac{I_o}{f_{\text{sc}} \cdot C} \times \left(\frac{2}{3}n^2 - \frac{1}{2}n - \frac{1}{6} + \frac{1}{4}n \right). \quad (28)
$$

From (22) and (25), it can be seen that the higher number capacitor has smaller voltage ripple and larger voltage drop. Consequently, the second capacitor has both the highest voltage and ripple, which are dependent on I_o, f_{sc}, C, and n. Among them, the number of stages is most influential. For the proposed converter, the voltage drop affected by the number of stages is more obvious than the voltage ripple; the result is similar to that of the conventional CW voltage multiplier investigated in [25]–[27] and [29]–[31].

Theoretically, each capacitor voltage has identical voltage except the first one. However, the voltages of capacitors are not equal to the theoretical value (V_o/n) in practical applications. For design consideration, the voltage difference among all capacitors should be as small as possible. Thus, higher f_{sc} and C are selected to achieve this, unless they are beyond practical limitations or other considerations. With a specified $V_{c2(\max)}$, (28) can be used to determine the capacitance value of capacitors in the CW voltage multiplier.

F. Number of Major Components

Referring back to Figs. 1 and 2, it can be seen that the numbers of diodes and capacitors increase when the number of the stages goes higher. These two devices, the input inductor and the controllable switch, are the major components of these kinds of cascaded converters. From this point of view, the number of major components is another merit of the proposed converter. For convenience, the duty cycle is all set to 0.8 for all competitors. Fig. 11 shows the number of major components versus voltage gain for the proposed converter and the topologies of Fig. 1(b) and (c). Obviously, the number of major components of converters shown in Fig. 1(b) and (c) is lesser
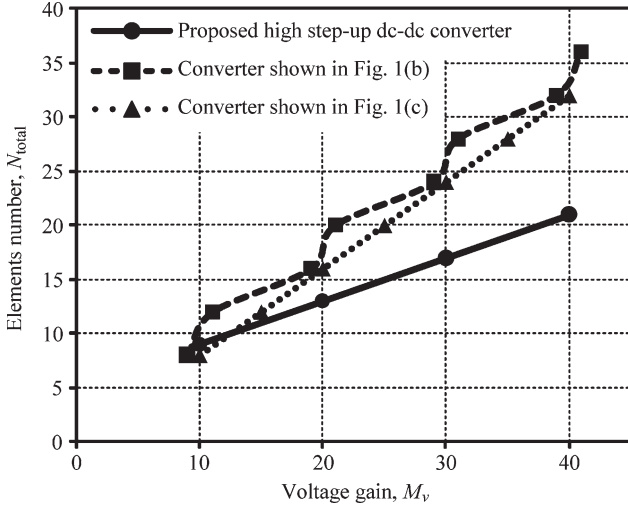
Fig. 11. Element number versus voltage gain at duty cycle $D = 0.8$ for the proposed converter and other converters.

Fig. 12. Timing diagram of switching patterns for the proposed converter including safe commutation states.

than that of the proposed converter when the voltage gain is equal to ten. However, when a higher voltage gain is desired, e.g., $M_v = 20$, the proposed converter only needs $n = 2$, and the total number of major components is 13. With the same voltage gain, the converter in Fig. 1(c) needs 16 components. Then, for a 19 voltage gain, the converter in Fig. 1(b) needs 16 components as well. Moreover, from Fig. 11, it can be seen that the difference of the number of major components between the proposed converter and the other converters increases when a higher voltage gain is desired.

IV. CONTROL STRATEGY OF PROPOSED CONVERTER

Due to the circuit operation, the proposed converter is similar to the conventional boost dc-dc converter, except that the proposed converter provides alternating current i_γ to the CW voltage multiplier. Thus, some commercial control ICs for conventional boost converters can adopt to the proposed converter with an extra auxiliary circuit which modifies the original PWM signal to signals with suitable timing and frequency for the four switches.

Taking a close look at the circuit states in Fig. 9, it can be found that S_{c1} and S_{c2} (S_{m1} and S_{m2}) swap the conduction states at the changing instant between each state. If the commutation fails, the discontinuous inductor current will cause voltage spike and damage the switching elements. However, the switching strategy, as shown in Fig. 8, for the four switches of the proposed converter is not including safe commutation technique. Therefore, another switching strategy including safe commutation technique under the same output function, as shown in Fig. 12, is used in the control strategy of the proposed converter to avoid open circuit of the inductor. The switching patterns of S_{c1} and S_{c2} place a short overlap time, while $S_{m2}(S_{m1})$ maintains a trigger high level when $S_{c1}(S_{c2})$ is turned on; in this way, it provides a safe commutation to the operation of the proposed converter.

In this paper, an average-current mode control will be used to design the PWM modulator in order to achieve the proposed converter in CCM. For facilitating design, this paper deploys
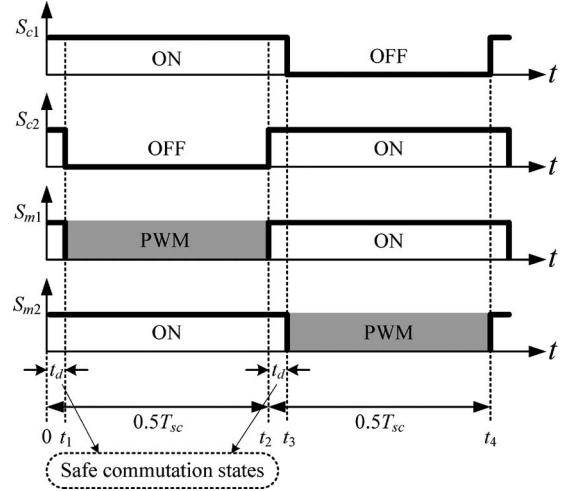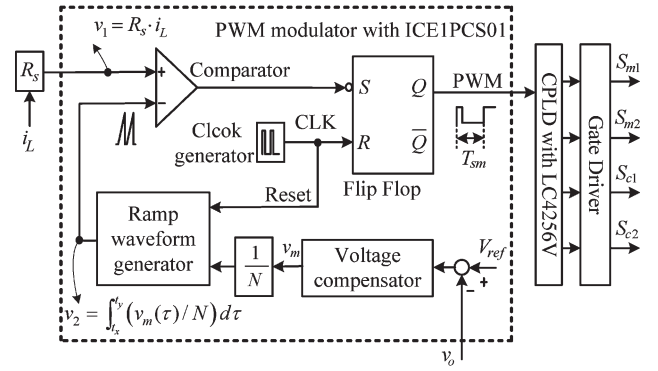

Fig. 13. Control strategy of proposed converter including safe commutation technique.

ICE1PCS01 as the main controller for the PWM modulator, which adopts the quasi-steady-state approach by using one-cycle control technique on leading-edge modulation, as shown in Fig. 13, in which the protective control devices are left out [34]. For the quasi-steady-state approach [35], the control aim is to provide a resistor emulator, making the input current i_L to be proportional to the input voltage V_{in}. Define the emulated resistance R_e as

$$R_e = \frac{V_{\text{in}}}{\langle i_L \rangle} \tag{29}$$

where $\langle i_L \rangle$ is the average of the input current over one modulation period T_{sm}.

Substituting (20) into (29), the emulated resistance can be rewritten as

$$R_e = \frac{V_o \cdot (1 - D)}{N \cdot \langle i_L \rangle} \tag{30}$$

where $N = 2n$.

In general, R_e can be regulated by the following control law [35]:

$$R_s \cdot \langle i_L \rangle = \frac{v_m}{M_V} \tag{31}$$

TABLE III
SYSTEM SPECIFICATIONS OF THE PROTOTYPE

Output power, P_o	200W
Output voltage, V_o	450V
Input dc voltage, V_{in}	42-54V
Modulation frequency, f_{sm}	60kHz
Alternating frequency, f_{sc}	1kHz
Resistive load, R_L	1kΩ
Stage number, n	3

TABLE IV
COMPONENT LIST FOR THE PROTOTYPE

Components Description	Symbol	Value/Part no.
Control IC	-	ICE1PCS01
CPLD	-	LC4256V
Boost inductor	L_s	1.5mH
Power switches	$S_{m1}, S_{m2}, S_{c1}, S_{c2}$	IRF640
Capacitors	$C_1 \sim C_6$	470μF/400V
Diodes	$D_1 \sim D_6$	SF20L60U
Gate driver	-	HCPL-3120

where R_s is the equivalent current-sensing resistance and v_m is the modulation voltage, which is determined by the error command between the reference value V_{ref} and actual value v_o, as shown in Fig. 13. As shown in Fig. 13, the voltage compensator is used to regulate the output voltage v_o through v_m to deliver suitable power to the load. Substituting (20) into (31)

$$R_s \cdot \langle i_L \rangle = \frac{v_m \cdot (1-D)}{N}. \tag{32}$$

Then, according to (30) and (32), R_e can be represented as

$$R_e = \frac{R_s \cdot V_o}{v_m}. \tag{33}$$

It can be seen from (33) that if the modulation voltage v_m is controlled to be a constant, the emulated resistance R_e will be a constant. Consequently, the input current will be proportional to the input voltage as shown in (29). In other words, the proposed converter operating in CCM can be achieved. The implementation of this performance has to regulate the duty cycle D of the PWM modulator to satisfy the control law as shown in (32). Using one-cycle control technology on leading-edge modulation, the PWM modulator, as shown in Fig. 13, is constructed by a constant time clock generator, a voltage comparator, an SR flip-flop, and a ramp waveform generator with reset. For practical applications, the average inductor current can be approximately equal to the instant inductor when the current ripple in the inductor is negligible during one modulation period [35]. Therefore, in this paper, the functions v_1 and v_2, as shown in Fig. 13, are set to implement the control law (32).

The PWM signal including boost function in CCM is obtained from the operation of PWM modulator. The PWM signal is fed into a preprogrammed complex programmable logic device, CPLD LC4256V, as shown in Fig. 13. A timer established in the CPLD is used to set the alternating period T_{sc} or alternating frequency f_{sc}. In addition, a logical circuit programmed in the same CPLD modifies the PWM signal from ICE1PCS01 and then sends the modified signals to trig the four switches. An overlap with interval t_d for safe commutation is implemented in the CPLD as well.

V. SIMULATION AND EXPERIMENTAL RESULTS

A prototype with 200-W rating was built to verify the validity of the proposed converter. The system specifications and components of the prototype are summarized in Tables III and IV, respectively. Moreover, Matlab/Simulink is applied to simulate
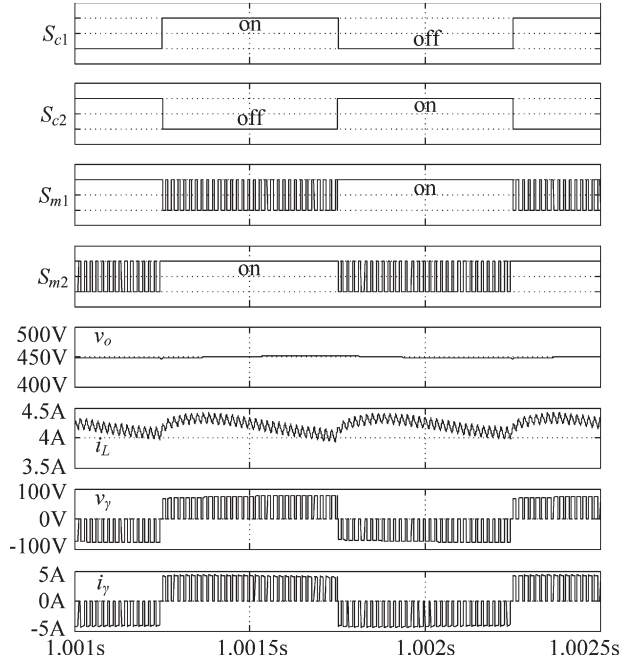

Fig. 14. Some selected waveforms for simulation using the proposed mathematical model at full-load $P_o = 200$ W and $V_{in} = 48$ V.

the mathematic model and control strategy of the proposed converter.

Some selected waveforms of the proposed converter at $P_o = 200$ W, $V_{in} = 48$ V, and $V_o = 450$ V for both simulation and experiment are shown in Figs. 14 and 15, respectively. The upper part of Fig. 14 shows the switching signals of simulation for the four switches, in which S_{c1} and S_{c2} are operated at f_{sc} and S_{m1} and S_{m2} are operated at f_{sm}. Moreover, the simulation results of the output voltage v_o, the input current i_L, the terminal voltage v_γ, and current i_γ of the CW voltage multiplier are shown in the lower part of Fig. 14. Fig. 15 shows the experimental waveforms of the switching signals, v_o, i_L, v_γ, and i_γ. Obviously, the simulation results well agree with the experimental results. In theoretical analysis, the input current ripple frequency (f_{sc}) is ignored due to the fact that the capacitors are assumed large enough to obtain stable capacitor voltages with no voltage ripple in the CW voltage multiplier. However, the voltage ripple exists practically in all capacitors. In other words, the input current and the output voltage have the same ripple frequency (f_{sc}). The results also influence the terminal voltage v_γ and current i_γ of the CW voltage multiplier.
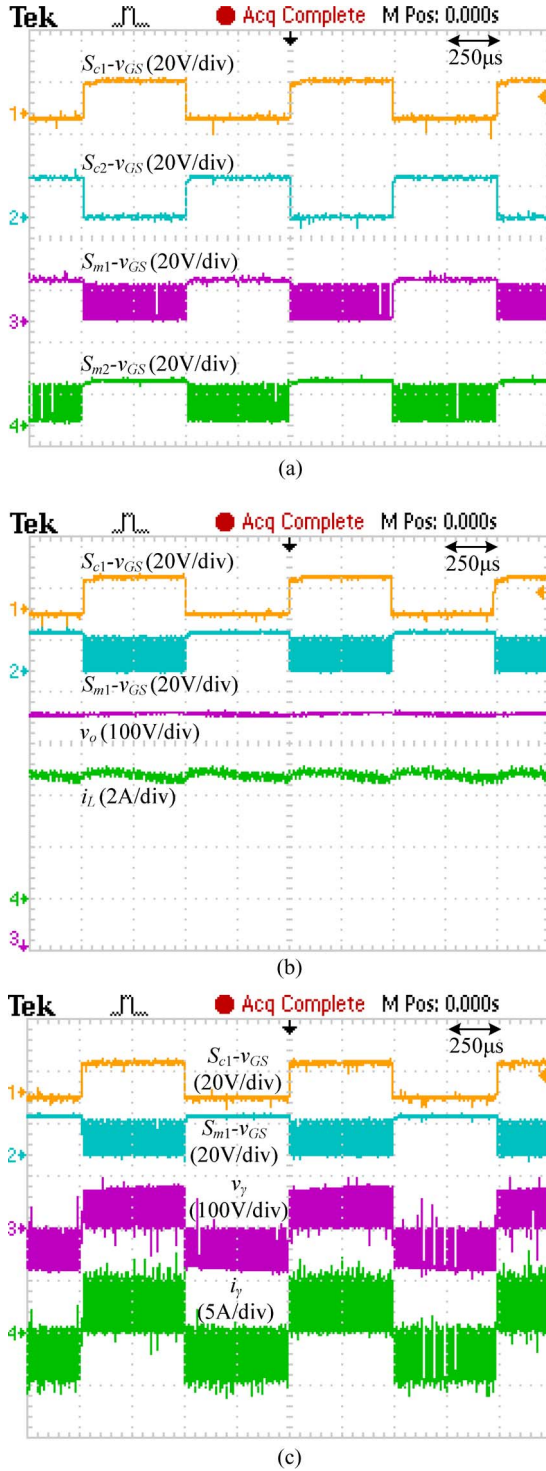
Fig. 15. Experimental waveforms of (a) $S_{c1}-v_{GS}$, $S_{c2}-v_{GS}$, $S_{m1}-v_{GS}$, and $S_{m2}-v_{GS}$; (b) $S_{c1}-v_{GS}$, $S_{m1}-v_{GS}$, v_o, and i_L; and (c) $S_{c1}-v_{GS}$, $S_{m1}-v_{GS}$, v_{AB}, and i_γ at full-load $P_o = 200$ W and $V_{in} = 48$ V.
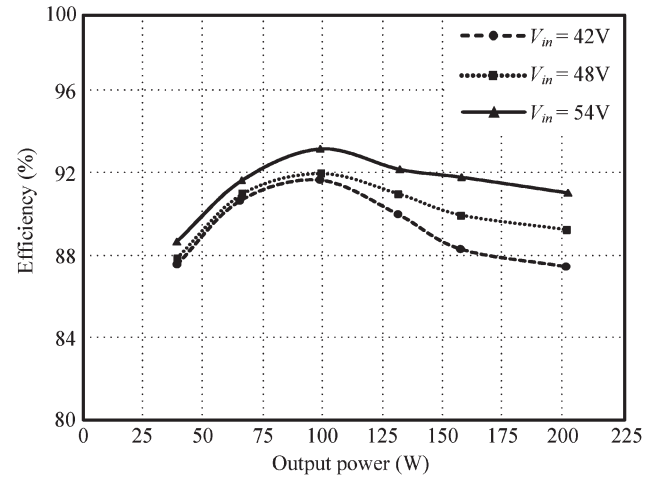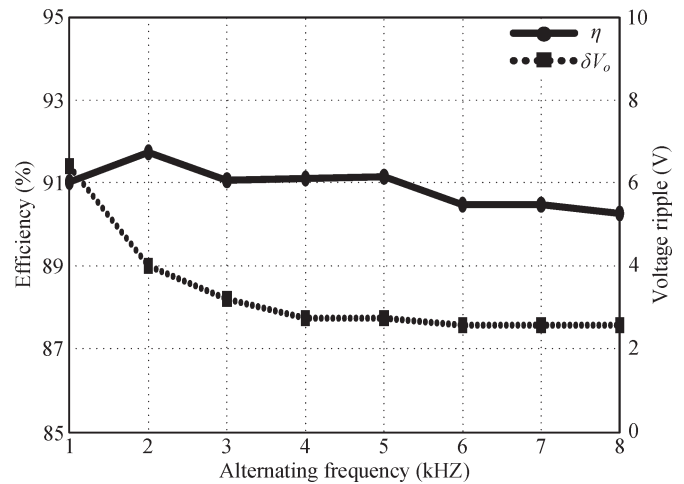

Fig. 16. Measured efficiency of proposed converter.

Fig. 17. Measured efficiency and voltage ripple of proposed converter at full-load $P_o = 200$ W and $V_{in} = 54$ V.

The efficiency of the proposed converter with different input voltages (42, 48, and 54 V) is shown in Fig. 16. The output voltage of the proposed converter is regulated at 450 V; thus, the voltage gains corresponding to these three input voltages are 10.7, 9.4, and 8.3, respectively. The results represent that the proposed converter has lower efficiency at lower input because of higher conducting loss accompanied by higher input current. On the other hand, for higher load condition, the efficiency

decreases due to the conducting loss of the diodes and the resistance loss of the capacitors. The highest system efficiency for these three input voltages appears at $P_o = 100$ W load. A maximum 93.15% efficiency is achieved at 54-V input voltage. Fig. 17 shows the efficiency and voltage ripple of the proposed converter at $V_{in} = 54$ V and $P_o = 200$ W when f_{sc} varies from 1 to 8 kHz. It can be seen that, when f_{sc} increases, the voltage ripple reduces to a minimum value when $f_{sc} > 4$ kHz, while the efficiency decreases only a slight value over the whole frequency range. Finally, Fig. 18 shows the theoretical, simulated, and experimental voltage gains under $V_{in} = 24$ V, $R_L = 2$ kΩ, $f_{sc} = 1$ kHz, and $f_{sm} = 60$ kHz. Three different stages ($n = 2$, 3, and 4) of CW circuit were used, while the experimental results demonstrate only for $n = 2$ and $n = 3$ with $D = 0-0.7$. As shown in Fig. 18, when $M_v < 15$, both simulation and experimental results well agree with the theoretical analysis. However, the difference increases when $M_v > 15$. The reason is that the effect of the parasitic elements increases when the proposed converter operates under high duty cycle, and the voltage gain will be deteriorated. Nevertheless, the proposed converter still can provide high voltage gain without extremely high duty cycle.
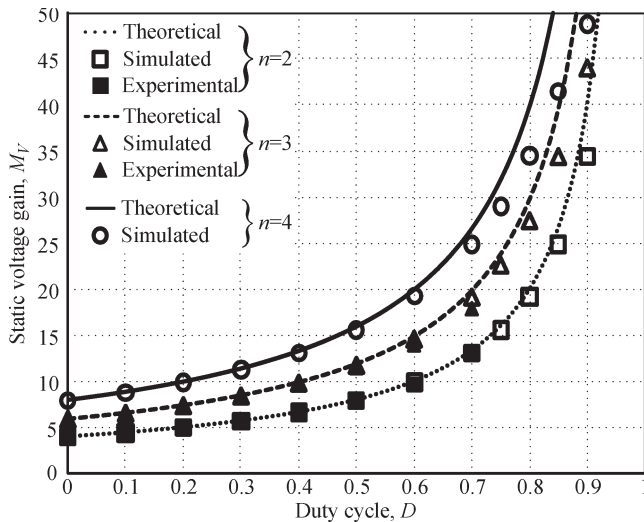
Fig. 18. Theoretical, simulated, and experimental voltage gains of the proposed converter under $V_{\text{in}} = 24$ V and $R_L = 2$ kΩ.

VI. CONCLUSION

In this paper, a high step-up dc-dc converter based on the CW voltage multiplier without a line- or high-frequency step-up transformer has been presented to obtain a high voltage gain. Since the voltage stress on the active switches, diodes, and capacitors is not affected by the number of cascaded stages, power components with the same voltage ratings can be selected. The mathematical modeling, circuit operation, design considerations, and control strategy were discussed. The control strategy of the proposed converter can be easily implemented with a commercial average-current-control CCM IC with adding a programmed CPLD. The proposed control strategy employs two independent frequencies, one of which operates at high frequency to minimize the size of the inductor while the other one operates at relatively low frequency according to the desired output voltage ripple. Finally, the simulation and experimental results proved the validity of theoretical analysis and the feasibility of the proposed converter. In future work, the influence of loading on the output voltage of the proposed converter will be derived for completing the steady-state analysis.

REFERENCES

[1] B. K. Bose, "Energy, environment, and advances in power electronics," *IEEE Trans. Power Electron.*, vol. 15, no. 4, pp. 688–701, Jul. 2000.
[2] F. Blaabjerg, Z. Chen, and S. B. Kjaer, "Power electronics as efficient interface in dispersed power generation systems," *IEEE Trans. Power Electron.*, vol. 19, no. 5, pp. 1184–1194, Sep. 2004.
[3] Q. Li and P. Wolfs, "A review of the single phase photovoltaic module integrated converter topologies with three different dc link configurations," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1320–1333, May 2008.
[4] W. Li and X. He, "Review of nonisolated high-step-up dc/dc converters in photovoltaic grid-connected applications," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1239–1250, Apr. 2011.
[5] M. W. Ellis, M. R. Von Spakovsky, and D. J. Nelson, "Fuel cell systems: Efficient, flexible energy conversion for the 21st century," *Proc. IEEE*, vol. 89, no. 12, pp. 1808–1817, Dec. 2001.
[6] G. R. Walker and P. C. Sernia, "Cascaded dc-dc converter connection of photovoltaic modules," *IEEE Trans. Power Electron.*, vol. 19, no. 4, pp. 1130–1139, Jul. 2004.
[7] J. Wang, F. Z. Peng, J. Anderson, A. Joseph, and R. Buffenbarger, "Low cost fuel cell converter system for residential power generation," *IEEE Trans. Power Electron.*, vol. 19, no. 5, pp. 1315–1322, Sep. 2004.

[8] L. S. Yang, T. J. Liang, and J. F. Chen, "Transformerless dc-dc converters with high step-up voltage gain," *IEEE Trans. Ind. Electron.*, vol. 56, no. 8, pp. 3144–3152, Aug. 2009.
[9] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics*, 2nd ed. New York: Wiley, 1995, pp. 172–178.
[10] A. L. Rabello, M. A. Co, D. S. L. Simonetti, and J. L. F. Vieira, "An isolated dc-dc boost converter using two cascade control loops," in *Proc. IEEE ISIE*, Jul. 1997, vol. 2, pp. 452–456.
[11] R. J. Wai, C. Y. Lin, C. Y. Lin, R. Y. Duan, and Y. R. Chang, "High-efficiency power conversion system for kilowatt-level stand-alone generation unit with low input voltage," *IEEE Trans. Ind. Electron.*, vol. 55, no. 10, pp. 3702–3714, Oct. 2008.
[12] J. M. Kwon, E. H. Kim, B. H. Kwon, and K. H. Nam, "High-efficiency fuel cell power conditioning system with input current ripple reduction," *IEEE Trans. Ind. Electron.*, vol. 56, no. 3, pp. 826–834, Mar. 2009.
[13] A. K. Rathore, A. K. S. Bhat, and R. Oruganti, "Analysis, design and experimental results of wide range ZVS active-clamped L-L type current-fed dc/dc converter for fuel cells to utility interface," *IEEE Trans. Ind. Electron.*, vol. 59, no. 1, pp. 473–485, Jan. 2012.
[14] B. Yuan, X. Yang, X. Zeng, J. Duan, J. Zhai, and D. Li, "Analysis and design of a high step-up current-fed multiresonant dc/dc converter with low circulating energy and zero-current switching for all active switches," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 964–978, Feb. 2012.
[15] R. J. Wai, C. Y. Lin, R. Y. Duan, and Y. R. Chang, "High-efficiency dc-dc converter with high voltage gain and reduced switch stress," *IEEE Trans. Ind. Electron.*, vol. 54, no. 1, pp. 354–364, Feb. 2007.
[16] T. F. Wu, Y. S. Lai, J. C. Hung, and Y. M. Chen, "Boost converter with coupled inductors and buck-boost type of active clamp," *IEEE Trans. Ind. Electron.*, vol. 55, no. 1, pp. 154–162, Jan. 2008.
[17] S. S. Lee, S. W. Rhee, and G. W. Moon, "Coupled inductor incorporated boost half-bridge converter with wide ZVS operation range," *IEEE Trans. Ind. Electron.*, vol. 56, no. 7, pp. 2505–2512, Jul. 2009.
[18] C. S. Leu, P. Y. Huang, and M. H. Li, "A novel dual-inductor boost converter with ripple cancellation for high-voltage-gain applications," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1268–1273, Apr. 2011.
[19] O. Abutbul, A. Gherlitz, Y. Berkovich, and A. Ioinovici, "Step-up switching-mode converter with high voltage gain using a switched-capacitor circuit," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 50, no. 8, pp. 1098–1102, Aug. 2003.
[20] F. L. Luo and H. Ye, "Positive output multiple-lift push-pull switched-capacitor Luo-converters," *IEEE Trans. Ind. Electron.*, vol. 51, no. 3, pp. 594–602, Jun. 2004.
[21] F. L. Luo and H. Ye, "Positive output cascade boost converters," *Proc. Inst. Elect. Eng.—Elect. Power Appl.*, vol. 151, no. 5, pp. 590–606, Sep. 2004.
[22] B. Axelrod, Y. Berkovich, and A. Ioinovici, "Switched-capacitor/switched-inductor structures for getting transformerless hybrid dc-dc PWM converters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 2, pp. 687–696, Mar. 2008.
[23] Y. Berkovich, B. Axelrod, and A. Shenkman, "A novel diode-capacitor voltage multiplier for increasing the voltage of photovoltaic cells," in *Proc. IEEE COMPEL*, Zurich, Switzerland, Aug. 2008, pp. 1–5.
[24] M. Prudente, L. L. Pfitscher, G. Emmendoerfer, E. F. Romaneli, and R. Gules, "Voltage multiplier cells applied to non-isolated dc-dc converters," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 871–887, Mar. 2008.
[25] M. D. Bellar, E. H. Watanabe, and A. C. Mesquita, "Analysis of the dynamic and steady-state performance of Cockcroft–Walton cascade rectifiers," *IEEE Trans. Power Electron.*, vol. 7, no. 3, pp. 526–534, Jul. 1992.
[26] F. Hwang, Y. Shen, and S. H. Jayaram, "Low-ripple compact high-voltage dc power supply," *IEEE Trans. Ind. Appl.*, vol. 42, no. 5, pp. 1139–1145, Sep./Oct. 2006.
[27] I. C. Kobougias and E. C. Tatakis, "Optimal design of a half-wave Cockcroft–Walton voltage multiplier with minimum total capacitance," *IEEE Trans. Power Electron.*, vol. 25, no. 9, pp. 2460–2468, Sep. 2010.
[28] C. M. Young and M. H. Chen, "A novel single-phase ac to high voltage dc converter based on Cockcroft–Walton cascade rectifier," in *Proc. IEEE PEDS*, 2009, pp. 822–826.
[29] M. M. Weiner, "Analysis of Cockcroft–Walton voltage multipliers with an arbitrary number of stages," *Rev. Sci. Instrum.*, vol. 40, no. 2, pp. 300–333, Feb. 1969.
[30] E. Kuffel and W. S. Zaengl, *High Voltage Engineering Fundamentals*. New York: Pergamon, 1984, ch. 2.
[31] M. Khalifa, "High-voltage engineering, theory and practice," in *Electrical Engineering and Electronics, a Series of Reference Books and Textbooks*, vol. 63. New York: Marcel Decker, Mar. 1990, ch. 6.

[32] L. Malesani and R. Piovan, "Theoretical performance of the capacitor-diode voltage multiplier fed by a current source," *IEEE Trans. Power Electron.*, vol. 8, no. 2, pp. 147–155, Apr. 1993.

[33] H. van der Broeck, "Analysis of a current fed voltage multiplier bridge for high voltage applications," in *Proc. IEEE PESC*, 2002, pp. 1919–1924.

[34] Infineon Technol., Preliminary datasheet, V1.1 ICE1PCS01-Standalone Power Factor Correction Controller in Continuous Conduction Mode, May 2003.

[35] Z. Lai and K. M. Smedley, "A family of continuous-conduction-mode power-factor-correction controllers based on the general pulse-width modulator," *IEEE Trans. Power Electron.*, vol. 13, no. 3, pp. 501–510, May 1998.
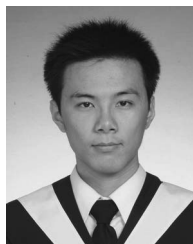
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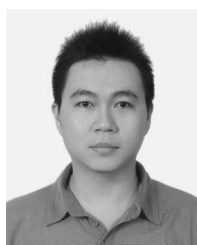
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