Load Compensation for Diesel Generator-Based Isolated Generation System Employing DSTATCOM

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***Abstract*—This paper presents the control of distribution static synchronous compensator (DSTATCOM) for reactive power, harmonics and unbalanced load current compensation of a diesel generator set for an isolated system. The control of DSTATCOM is achieved using least mean square-based adaptive linear element (Adaline). An Adaline is used to extract balanced positive-sequence real fundamental frequency component of the load current and a proportional–integral (PI) controller is used to maintain a constant voltage at the dc-bus of a voltage-source converter (VSC) working as a DSTATCOM. Switching of VSC is achieved by controlling source currents to follow reference currents using hysteresis-based PWM control. This scheme is simulated under MATLAB environment using Simulink and PSB block-set toolboxes for feeding linear and nonlinear loads. The modeling is performed for a three-phase, three-wire star-connected synchronous generator coupled to a diesel engine, along with the three-leg VSC working as a DSTATCOM. Results are presented to verify the effectiveness of the control of DSTATCOM for the load compensation and an optimal operation of the DG set.**

***Index Terms*—Adaline, diesel generator set, distribution static synchronous compensator (DSTATCOM), harmonic elimination, load compensation.**

I. Introduction

INSTALLATION OF the diesel engine-based electricity generation unit (DG set) is a widely used practice to feed the power to some crucial equipment in remote areas [1], [2]. DG sets used for these purposes are loaded with unbalanced, reactive and nonlinear loads such as power supplies in some telecommunication equipment and medical equipment. The source impedance of the DG set is quite high, and the unbalanced and distorted currents lead to the unbalanced and distorted three-phase voltages at point of common coupling (PCC). Harmonics and unbalanced currents flowing through the generator result into torque ripples at the generator shaft. All of these factors lead to the increased fuel consumption and reduced life of the DG sets. These forces the DG sets to be operated with derating, which results into an increased cost of the system. Nowadays, small generator units are available with full conversion (inverter-converter) units to meet stringent power quality norms [3]. Instead of using these, a DSTATCOM [2] can be used with a three-phase DG set to feed unbalanced loads without derating the DG set and to have the same cost involved. For example, a 24-kW lagging power factor load of 0.8 pf will consume 18 kVAR which is 60% of total kVA rating of a 30 kVA generator. The market price of an inverter is \$50–70 per kVA which can be easily be configured to work as a DSTATCOM. However, the capital cost of the diesel generator is approximately §500 per kVA rating. Moreover, the DSATCOM can provide compensation for harmonics which facilitates to load the DG set up to its full kVA rating.

The performance of DSTATCOM is very much dependent on the method of deriving reference compensating signals. Instantaneous reactive power theory, modified p-q theory, synchronous reference frame theory, instantaneous $i_{\mathrm{d}} - i_{\mathrm{q}}$ theory, and method for estimation of reference currents by maintaining the voltage of dc link are generally reported in the literature for an estimation of reference currents for the DSTATCOM through the extraction of positive-sequence real fundamental current component from the load current [4]–[7]. These techniques are based on complex calculations and generally incorporate a set of low-pass filter which results in a delay in the computation of reference currents and therefore leads to slow dynamic response of the DSTATCOM. In this paper, a fast and simple neural network-based control scheme is used to estimate reference source currents for the control of the DSTATCOM.

This paper presents a DSTATCOM for the load compensation of a diesel generator set to enhance its performance. The control of DSTATCOM with capabilities of reactive power, harmonics and unbalanced load compensation is achieved by Least Mean Square (LMS) algorithm [8], [9] based adaptive linear element (Adaline). The Adaline is used to extract positive-sequence fundamental frequency real component of the load current. The dc-bus voltage of voltage source converter (VSC) is supported by a proportional–integral (PI) controller which computes current component to compensate losses in DSTATCOM. The extraction of reference currents using Adaline involves an estimation of weights. These weights are measure of peak of fundamental frequency real current component of the load current. The life of a DG set is enhanced in the absence of unbalanced and harmonic currents. The modeling of the DG set is performed using a synchronous generator, a speed governor, and the excitation control system. This proposed system is simulated under MATLAB environment using Simulink and PSB Block-set toolboxes. The results for a 30-kVA DG set with the linear load at 0.8 lagging pf and a nonlinear load with different load dynamics and unbalance load conditions are

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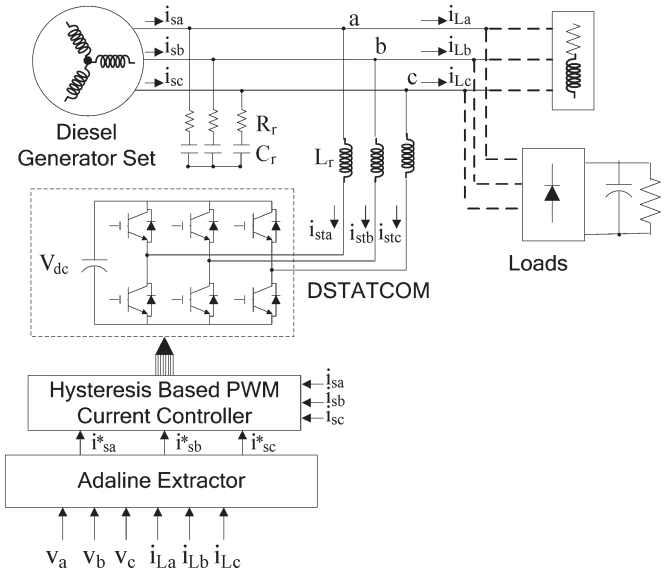

Fig. 1. Basic configuration of the DG set with DSTATCOM.

TABLE I
SYSTEM SPECIFICATIONS

Load	Linear	Delta Connected R-L load of 37.5 kVA at 0.8pf
	Non-linear	30 kW Diode bridge converter with LC filter at output with L=2 mH and C=500 μF
Voltage Source Converter		DC link capacitor C_{dc}=10000 μF, AC inductor=3 mH, Ripple Filter: C_r=10 μF and R_r=8 Ω, f_s=20 kHz.

presented to demonstrate the effectiveness of DSTATCOM-DG set system.

II. SYSTEM CONFIGURATION

Fig. 1 shows the configuration of the system for a three-phase three-wire DG set feeding to variety of loads. A 30 kVA system is chosen to demonstrate the work of the system with the DSTATCOM. The DSTATCOM consists of an insulated gate bipolar transistors-based three-phase three-leg VSC system. The load current is tracked using Adaline-based reference current generator, which in conjunction with the hysteresis-based PWM current controller that provides switching signals for VSC-based DSTATCOM. It controls source currents to follow a set of three-phase reference currents. The parameters of a salient pole synchronous generator are 415 V, 30 kVA, 4 pole, 1500 rpm, 50 Hz, $X_{\rm d} = 1.56$ pu, $X'_{\rm d} = 0.15$ pu $X''_{\rm d} = 0.11$ pu, $X_{\rm q} = 0.78$, $X'_{\rm q} = 0.17$, $X''_{\rm q} = 0.6$, $H_{\rm s} = 0.08$. The other critical parameters are given in Table I.

III. CONTROL ALGORITHM

The operation of this system requires a DG set to supply real power needed to the load and some losses (switching losses of devices used in VSC, losses in the reactor, and dielectric losses

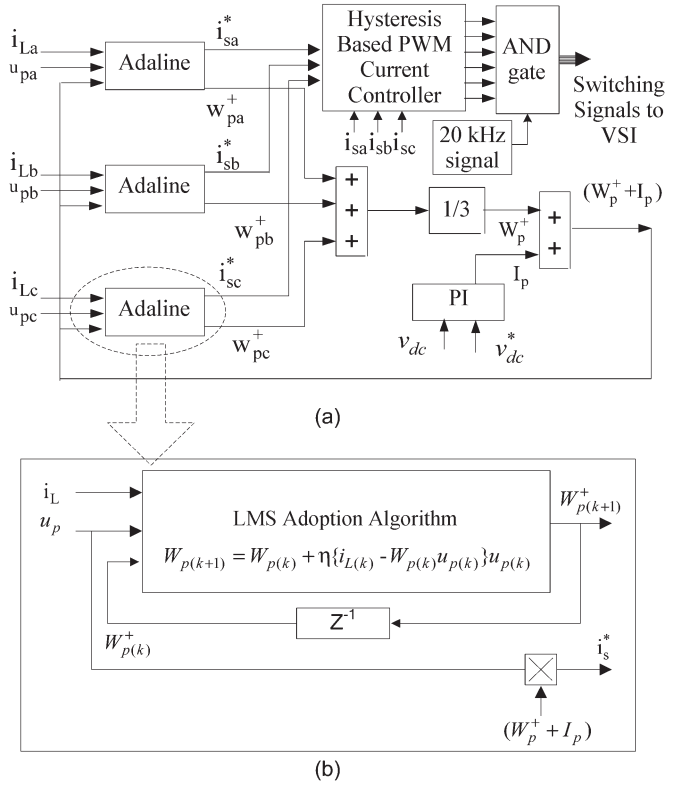

Fig. 2. (a), (b). Control block diagram of the reference current extraction scheme.

of the dc capacitor) in DSTATCOM. Therefore, the reference source current used to decide the switching of the DSTATCOM has two parts. One is real fundamental frequency component of the load current, which is being extracted using Adaline and another component, which corresponds to the losses in the DSTATCOM, are estimated using a PI controller over dc voltage of DSTATCOM. Fig. 2(a) shows the control scheme for the implementation of reactive, unbalanced and harmonic currents compensation. The output of the PI controller is added to the weight calculated by the Adaline to maintain the dc-bus voltage of the DSTATCOM.

A. Extraction of Real Positive-Sequence Fundamental Frequency Current from Load Current

The basic theory of the proposed decomposer is based on LMS algorithm [9] and its training through Adaline, which tracks a unit voltage vector templates to maintain minimum error. The basic concept of theory used here can be understood by considering the analysis in single-phase system which is given. For an ac system, the supply voltage may be expressed as

$$v_s = V \sin \omega t \tag{1}$$

where v_s is the instantaneous ac terminal voltage, V is an amplitude and ω is the angular frequency of the voltage.

The load current (i_L) consists of active current (i_p^+), reactive current (i_q^+) for the positive sequence, negative-sequence

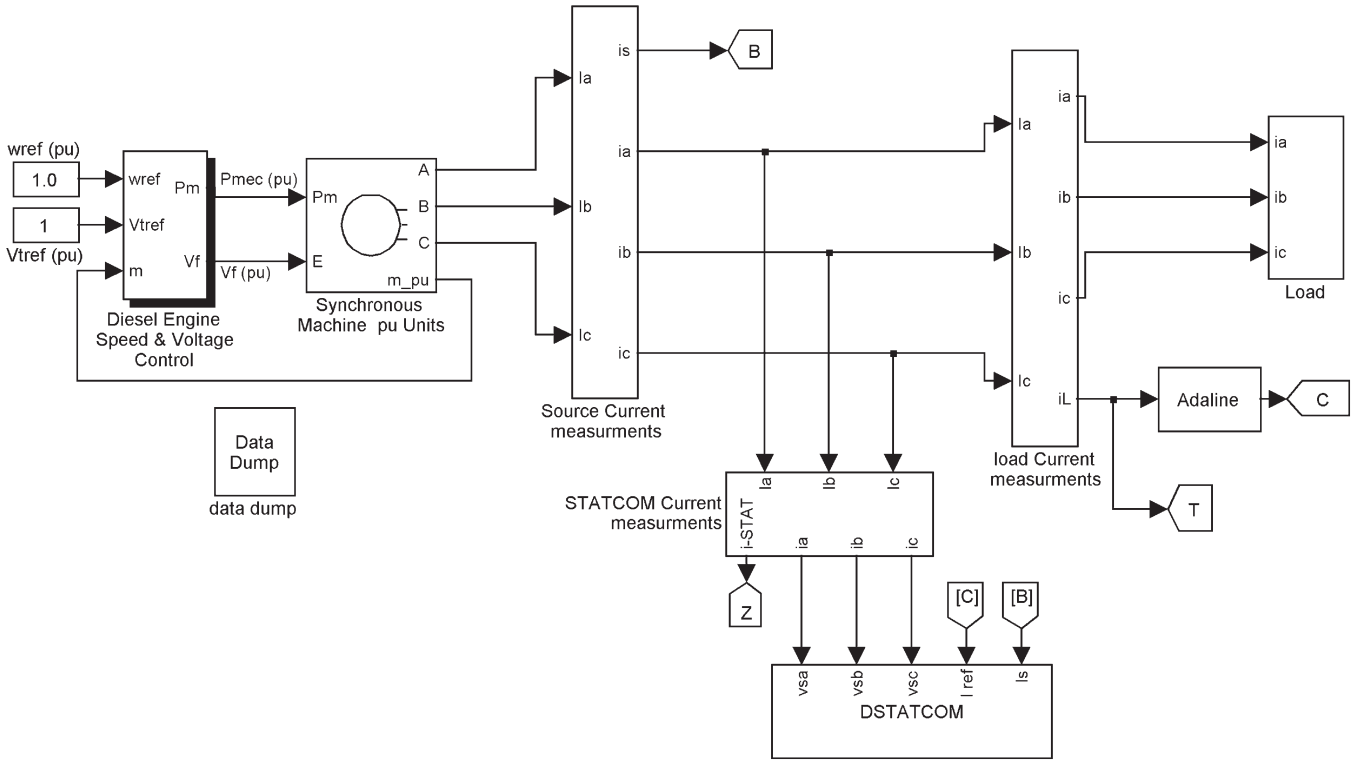

Fig. 3. MATLAB based simulation Model.

current (i^-), and harmonic frequency current (i_h) can be written as summation of different parts as

$$i_L = i_p^+ + i_q^+ + i^- + i_h. \tag{2}$$

The control algorithm is based on the extraction of the current component in phase with unit voltage template. To estimate the fundamental frequency positive-sequence real component of load current, the unit voltage template should be in phase with the system voltage and should have unit amplitude. The unit voltage template (u_p) derived from the system phase voltage can be represented as:

$$u_p = v_s/V. \tag{3}$$

For proper estimation of the current components of the load current, the unit voltage templates must be undistorted. In case of the voltage being distorted, the zero crossing of phase voltage is detected to generate sinusoid $(\sin \omega t)$ vector template, synchronized with system terminal voltage. This signal is generated from the look-up table by adjustment of the delay to track the change in the frequency of the system.

An initial estimate of the active part of load current for single-phase can be chosen as

$$i_p^+ = W_p u_p \tag{4}$$

where weight (W_p) is estimated using an Adaline. This weight is variable and changes as per the load current. The scheme for estimating weights corresponding to fundamental frequency real component of load current (for three-phase system), based on LMS algorithm-tuned Adaline tracks the unit vector templates to maintain minimum error. The estimation of the weight is given as per the following iterations:

$$W_{p(k+1)} = W_{p(k)} + \eta \left\{ i_{L(k)} - W_{p(k)} u_{p(k)} \right\} u_{p(k)} \tag{5}$$

where subscript k and $\mathrm{k}+1$ represent sample instant and η is the convergence coefficient. The value of convergence coefficient decides the rate of convergence and the accuracy of the estimation. The practical range of convergence coefficient lies in between 0.1 to 1.0. Three-phase reference currents corresponding to positive-sequence real component of the load current may be computed as

$$i_{pa}^+ = W_p^+ u_{pa}; i_{pb}^+ = W_p^+ u_{pb}; i_{pc}^+ = W_p^+ u_{pc} \tag{6}$$

$$W_p^+ = \left(W_{pa}^+ + W_{pa}^+ + W_{pc}^+\right)/3 \tag{7}$$

where W_p^+ is averaged weight. Weights of phase a, b and c are averaged to compute the equivalent weight for positive-sequence current component in the decomposed form. The averaging of weights helps in removing the unbalance in load current components.

B. PI Controller for Maintaining Constant DC-Bus Voltage of DSTATCOM

To compute the second component of reference active power current, a reference dc-bus voltage is compared with sensed dc-bus voltage of DSTATCOM. This comparison of sensed dc-bus voltage (v_{dc}) to the reference dc-bus voltage (v_{dc}^*) of VSC,

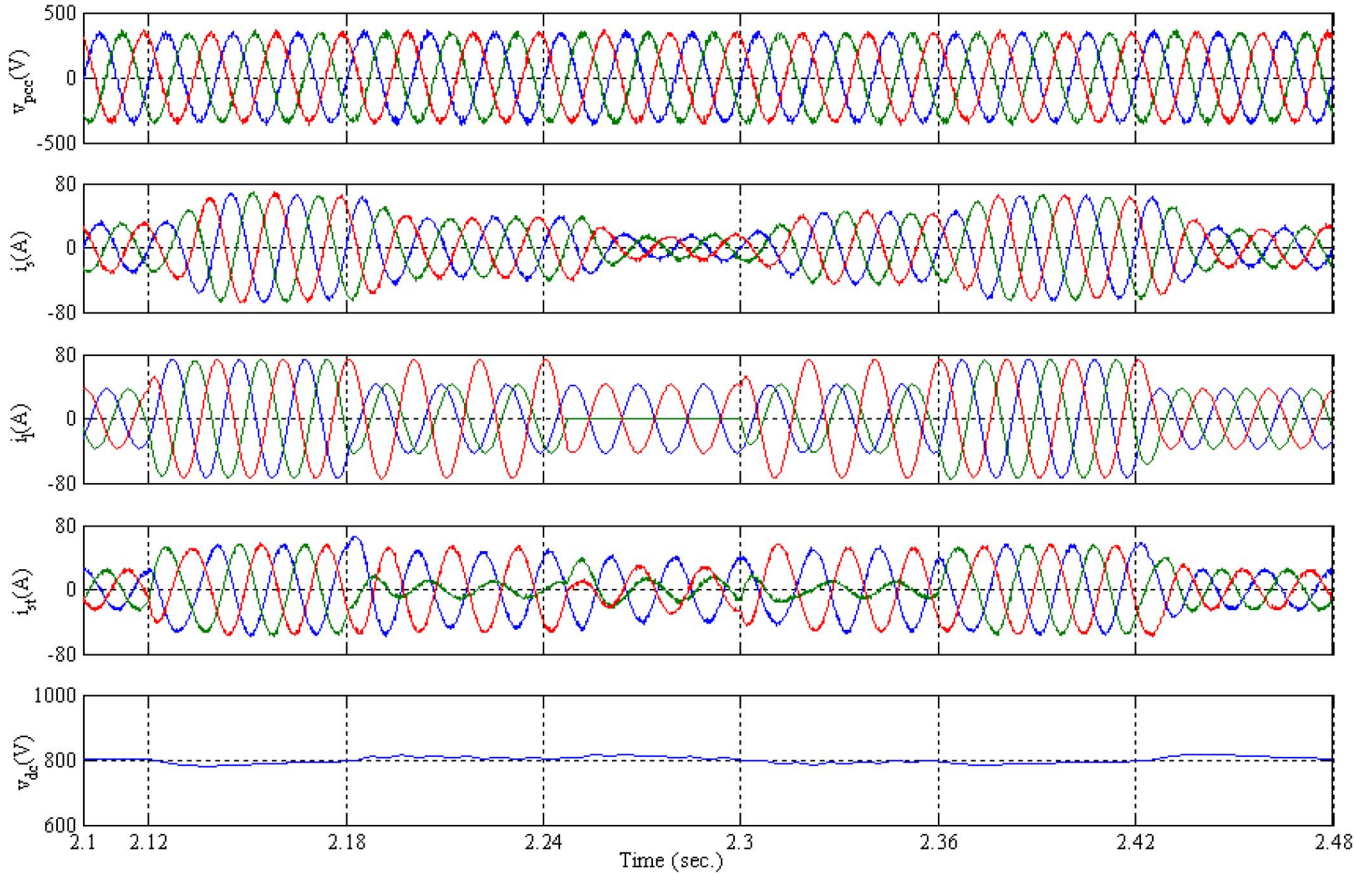

Fig. 4. Dynamic performance of the DSTATCOM-DG isolated system with linear load.

results in a voltage error (v_{dcl}), which in the nth sampling instant is expressed as

$$v_{dcl(n)} = v^*_{dc(n)} - v_{dc(n)}. \tag{8}$$

This error signal is processed in a PI controller and output $\{I_{\mathrm{p(n)}}\}$ at the nth sampling instant is expressed as:

$$I_{p(n)} = I_{p(n-1)} + K_{pdc}\left\{v_{dcl(n)} - v_{dcl(n-1)}\right\} + K_{idc}v_{dcl(n)} \tag{9}$$

where K_{pdc} and K_{idc} are proportional and integral gains of the PI controller.

The output of the PI controller accounts for the losses in DSTATCOM and it is considered as the loss component of the current, which is added with the weight estimated by the Adaline corresponding to fundamental frequency positive-sequence reference active current component. Therefore, the total real reference current has component corresponding to the load and component corresponding to feed the losses of DSTATCOM, is expressed as

$$\begin{aligned} i^*_{sa} &= \left(W^+_p + I_p\right) u_{pa}; i^*_{sb} = \left(W^+_p + I_p\right) u_{pb}; \\ i^*_{sc} &= \left(W^+_p + I_p\right) u_{pc}. \end{aligned} \tag{10}$$

These three-phase currents are considered reference source currents i_{ref} (i^*_{sa}, i^*_{sb} and i^*_{sc}) and along with sensed source currents i_{act} (i_{sa}, i_{sb} and i_{sc}), these are fed to the hysteresis-based PWM current controller to control the source currents to follow these reference currents. The switching signals generated by the PWM current controller force actual source currents to acquire shape close to the reference source currents. This indirect current control results in the control of the slow varying source current (as compared to DSTATCOM currents) and therefore requires less computational efforts. Switching signals are generated on the following logic:

if $(i_{act}) < (i_{ref} - hb/2)$ upper switch of the leg is ON and lower switch is OFF

if $(i_{act}) > (i_{ref} + hb/2)$ upper switch of the leg is OFF and lower switch is ON

where hb is hysteresis band around the reference current i_{ref}.

The weights are computed online by LMS algorithm. The update equation of weights based on LMS algorithm is described in (5) for each phase. The structure of such Adaline is depicted in Fig. 2(b). Weights are averaged not only for averaging at fundamental frequency but to cancel out sinusoidal oscillating components in weights present due to harmonics in the source current. The averaging of weights in different phases is shown in Fig. 2(a). Thus Adaline is trained at fundamental frequency of a particular sequence in-phase with voltage. Fig. 2(a) and (b) show the detailed scheme implemented for control of DSTATCOM.

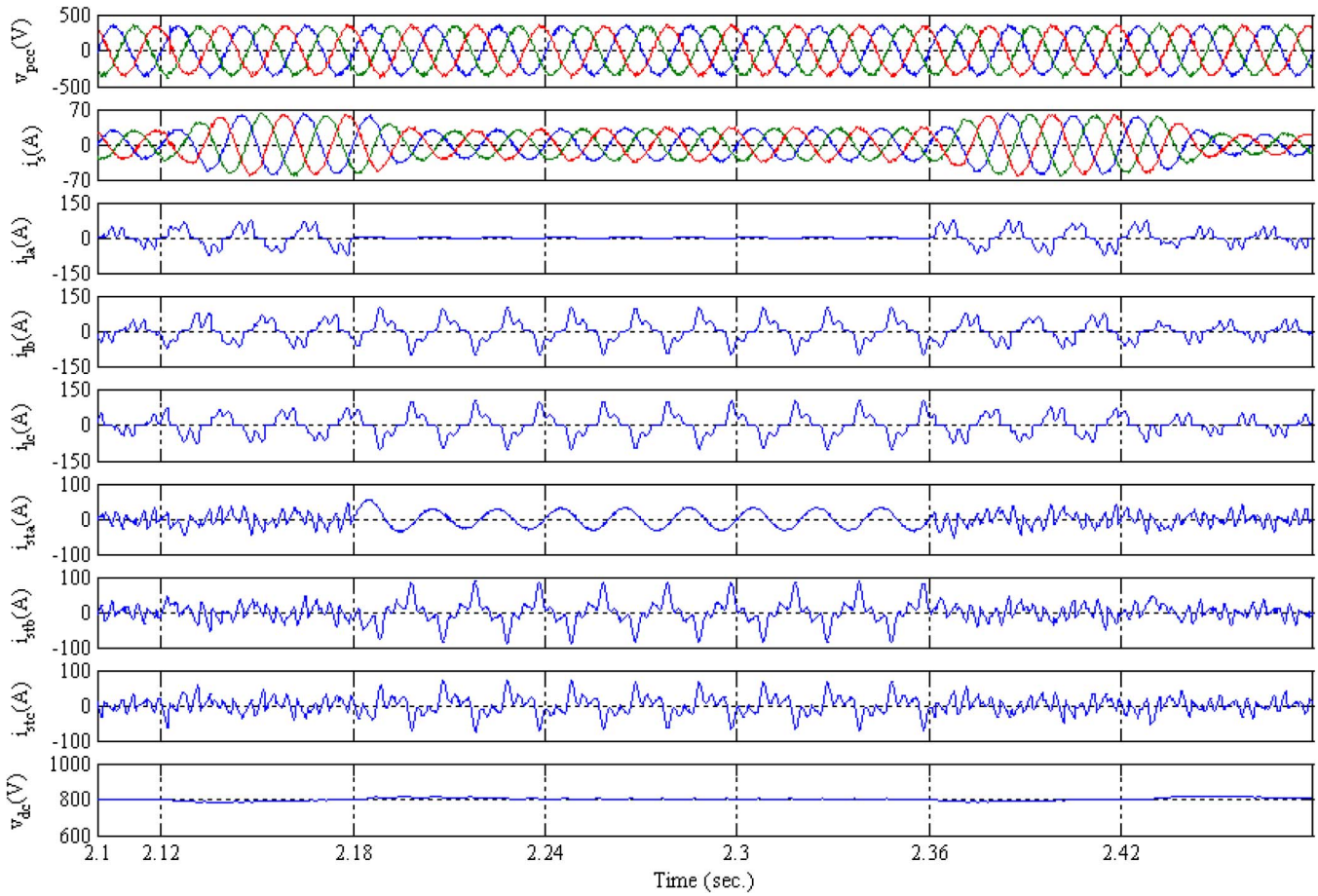

Fig. 5. Dynamic performance of the DSTATCOM-DG isolated system with nonlinear load.

Due to the unbalance in the load currents, a second harmonic ripple is produced in the dc-bus voltage. Similarly, harmonics in the load currents also produce ripple at dc-bus voltage. However, this ripple is at higher frequency as compared to the second harmonic ripple. These ripples have to be filtered out before feeding the signal of the PI controller; otherwise this may introduce the harmonics component in source currents (predominantly because of harmonic ripple at dc bus). For this purpose the dc-bus voltage is filtered using a low-pass filter (LPF). Since major amount of reference current (load real current component) is computed using Adaline-based extractor, effect of the delay caused by the LPF is negligible in practical cases.

IV. MATLAB Simulation

Fig. 3 shows the MATLAB model of the DSTATCOM-DG set isolated system. The modeling of the DG set is carried out using a star connected synchronous generator of 30 kVA, controlled by a speed governor and an excitation system. The linear load applied to the generator is at 0.8 lagging pf which is modeled as a delta connection of the series combination of resistance and inductance (R-L) models. The nonlinear load is modeled using discrete diodes connected in a bridge with a capacitor filter and a resistive load on the dc bus. The unbalanced was realized by disconnecting phase-a from the diode bridge. The simulation is carried out in continuous mode at $1 * 10$-6 step size with ode15s (stiff/NDF) solver.

V. Results and Discussion

The simulation of the DSTATCOM-DG isolated system is carried out with different types of loads i.e., a linear R-L load, a nonlinear load i.e., a diode bridge converter load. The load compensation is demonstrated for these types of loads using DSTATCOM system for an isolated DG set. The following observations are made on the basis of obtained simulation results under different system conditions.

A. DG Set System Operation Under Linear Load

Fig. 4 shows the dynamic performance of the DG set with DSTATCOM system. From $t = 2.10$ s to 2.12 s, a three-phase 18.75-kVA load at 0.8 pf is being connected. At $t = 2.12$ s, the load is increased upt o 37.5 kVA at 0.8 pf. The real power supplied by the DG set is 30 kW and reactive power is supplied by the DSTATCOM. At $t = 2.18$ s, an unbalanced is introduced in the load by taking off load from phase a. It can be easily observed that even if load currents (i_{L}) are unbalanced, the source currents (i_{s}) are still balanced. At $t = 2.24$ s, the load is taken out from phase b also, even in this condition the

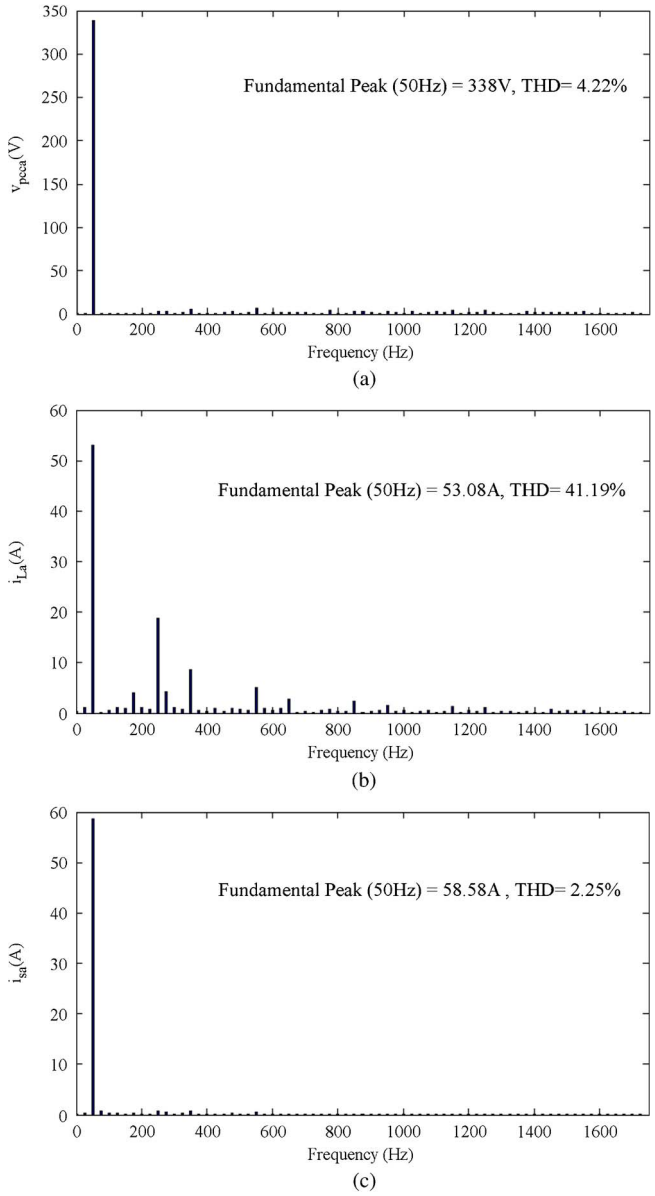

Fig. 6. Harmonic spectra of phase-a (a) voltage at PCC (b) load current and (c) source current at peak nonlinear load condition.

DSTATCOM system is able to balance DG set currents. For time $t = 2.3$ s to $t = 2.48$ s these dynamics are shown in the reverse sequence of events. The dc-bus voltage of VSC is well maintained at 800 V during the complete range of operation and the small sag and swell in the voltage at the load change are compensated by the PI controller action.

B. DG Set System Operation under Non-Linear Load

Fig. 5 shows the performance of the DG set with DSTATCOM under nonlinear loading conditions. The load on the system is kept 15.0 kW initially for time $t = 2.1$ s to 2.12 s. The load compensation in terms of harmonic mitigation is also being provided by the DSTATCOM during this condition. The load is increased to 30 kW at $t = 2.12$ s. At $t = 2.18$ s, an unbalanced is introduced in load and therefore the load is reduced to 16.4 kW. At $t = 2.36$ s, phase-a load is reconnected again to the diode bridge and the load is reduced to its initial value

TABLE II
%THD OF THREE-PHASE VOLTAGES AT PCC, LOAD CURRENTS AND SOURCE CURRENTS WITH NON-LINEAR LOADS

Condition		% THD			RMS Voltage (V) and Currents (A)		
		Ph. a	Ph. b	Ph. c	Ph. a	Ph. b	Ph. c
Light Load Condition	V_{pcc}	3.49	3.72	3.43	239.5	239.5	239.6
	i_L	69.99	68.85	70.76	23.2	23.2	23.3
	i_S	3.73	3.72	4.10	20.3	20.3	20.4
Peak Load Condition	V_{pcc}	4.22	4.19	4.35	239.4	239.5	239.5
	i_L	41.19	38.81	38.89	42.5	42.4	42.6
	i_S	2.25	2.00	2.14	41.4	41.3	41.4

(15.6 kW) and at $t = 2.42$ s, to demonstrate the dynamics in reverse sequence of events. The harmonic spectra of the phase-a voltage, load and source currents are shown in Fig. 6(a)–(c) for peak load condition. The high value of the % total harmonic distortion (THD) of voltage at PCC, load currents and source currents are given in Table II for light load and peak load conditions. A high value of the %THD of the voltage at PCC is due to the high source impedance of the generator. The improvement in the voltage waveform is achieved using of a ripple filter employed at the DG set terminals comprising of a capacitance and resistive constituting a high-pass filter. The DG set currents and voltages are observed to be almost sinusoidal and balanced and operating at unity power factor.

VI. CONCLUSION

The proposed control algorithm of the DSTATCOM has been found to improve the performance of the isolated DG system. The DSTATOM has compensated the variety of loads on the DG set and it has sinusoidal voltages at PCC and currents with compensated and equivalent linear balanced unity power factor loads. The cost of the installation of DSTATCOM system with the DG set can be compensated as it leads to less initial and running cost of DG set as its ideal operation while feeding variety of loads.

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