Buck–Boost-Type Unity Power Factor Rectifier With Extended Voltage Conversion Ratio

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***Abstract*—A buck–boost-type unity power factor rectifier is proposed in this paper. The main advantage of the proposed rectifier over the conventional buck–boost type is that it can perform input power factor correction (PFC) over a wider voltage conversion range. With a single switch, a fast well-regulated output voltage is achieved with a zero-current switch at turn-on. Moreover, the switch voltage stress is independent of converter load variation. The proposed converter is well suited for universal offline PFC applications for a low power range (< 150 W). The feasibility of the converter is confirmed with results obtained from a computer simulation and from an experimental prototype.**

***Index Terms*—Low harmonic rectifier, power factor correction (PFC), single-stage single-switch rectifier, unity power factor (UPF).**

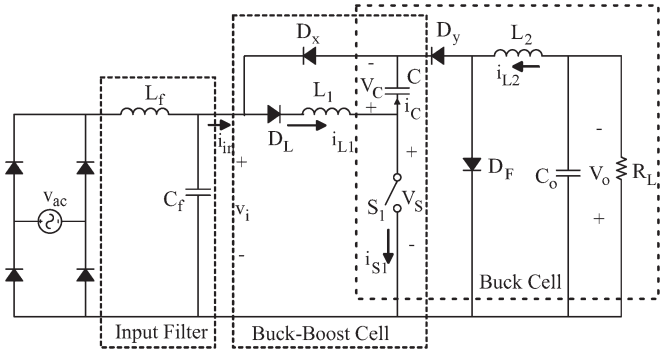

Fig. 1. Proposed single-stage PFC converter.

I. Introduction

MANY single-stage power factor correction (PFC) topologies have been recently proposed as a cost-effective approach for achieving both the function of high PFC and fast output voltage regulation by using one (or one set of synchronized) active switch(es) under a single control loop. Unfortunately, unlike the two-stage approach, single-stage converters have relatively high-voltage stress suffered by their switching components due to unregulated dc voltage on the intermediate energy storage capacitor, which generally depends on both the line and load characteristics [1]–[3]. This condition will limit the single-stage approach, particularly when it requires an operation with a universal input voltage since the storage capacitor voltage would easily rise beyond 450 V. Therefore, a bulky capacitor and high-voltage-rating semiconductors have to be used; this increases both the size and cost, and will result in lower efficiency as well as reduced holdup time.

In an effort to reduce the dc voltage on the energy storage capacitor, a number of techniques have been introduced [4]–[29]. However, most of the proposed techniques usually comprise a boost converter for PFC, followed by a dc–dc converter for output voltage regulation. Hence, for low-output-voltage applications, a high step-down transformer topology would be needed for the output dc–dc stage even when galvanic isolation is not required.

On the other hand, conventional single-switch buck–boost topologies, including the plain buck–boost, flyback, SEPIC, and Cuk converters [30], [31], have the potential of both PFC and step-down conversion capability. However, they incur penalties of reduced efficiencies and increase component stresses, compared to the boost converter. Moreover, the buck–boost topologies suffer from providing low output voltage over a large range of input voltages since it requires an extremely low duty ratio (short switch-on time) operation. A high-switching-frequency operation reduces the switch-on time even shorter and gives rise to an objectionable increase in switching losses. Thus, not only does it degrade the efficiency of the converter but it also limits the ability to increase the switching frequency. Moreover, considering, for example, a buck–boost converter with $V_{\rm IN} = 370$ V and $V_{\rm OUT} = 5$ V operating at 100 kHz would require a switch-on time of 133 ns, which is close to the physical limitation of some of the low-cost pulsewidth modulation controller's minimum on-time. Last but not the least, conventional buck–boost topologies operating with extremely low or high duty ratio utilize the active switch very poorly [32].

The motivation and main objective of this paper have been established from the result of previous literature research on single-stage single-switch PFC transformerless topologies suitable for universal input voltage operation and low output dc voltage applications. We approach this task by cascading a front-end buck–boost converter with an output buck converter, as shown in Fig. 1. The buck–boost converter is selected due to its capability of providing a step-down voltage conversion and a high power factor when it is operating in the discontinuous conduction mode (DCM). On the other hand, the buck converter is selected due to its step-down capability. Hence, a high step-down ratio is achieved. In addition, the related characteristics of the proposed converter in Fig. 1 also include the absence of inrush current problem and the ability to protect against over load current.

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It should be mentioned here that the proposed converter in Fig. 1 is a modified version of its dc–dc version presented in [33], by adding an additional diode D_L in series with L_1. Moreover, the operation of the buck output cell in Fig. 1, in either the continuous conduction mode (CCM) or DCM, has no effect on the quality of the input current. However, it is found that operating the buck cell in the DCM gives several desirable advantages. These advantages include the following:

1) zero-current switch turn-on;
2) reduction of the reverse recovery problem of the fast diodes in the circuit;
3) low-voltage stress on both the energy stored capacitor C and the active switch S_1, and independent of the output load current;
4) well and fast regulation of the output voltage.

The aforementioned advantages are obtained at the expense of drawing higher peak currents by the converter. By using a high speed and a higher current density switch, the peak currents and their impact become less significant when compared to the gained advantages. Furthermore, the converter efficiency can be improved if buck cell inductor L_2 is operated in the boundary conduction mode (BCM) since the peak currents in the converter will be relatively reduced. This will also reduce the ac core losses as well as the current ripple in output capacitor C_o.

Section II presents the principle of operation of the proposed converter along with the important circuit equations. A low-frequency averaged model of the proposed converter and the steady-state characteristics is presented in Section III. In Section IV, the design considerations of the proposed converter will be given. Simulation and experimental results are presented in Section V to verify the validity of the proposed concept. Finally, a conclusion will be given in Section VI.

II. Converter Operation Principle

The proposed converter shown in Fig. 1 is analyzed with six assumptions in this section.

1) Input voltage $v_{\rm ac}$ is considered to be an ideal rectified sine wave, i.e., $v_i = V_m|\sin(\omega_L t)|$, where V_m is the peak amplitude and ω_L is the line angular frequency.
2) All components are ideal; thus, the efficiency is 100%.
3) Switching frequency f_s is much higher than ac line frequency f_L, so that the input voltage can be considered constant during one switching period T_s.
4) Capacitor C is big enough such that voltage V_C can be considered constant during T_s. Furthermore, output voltage V_o is pure dc without twice the line frequency ripple.
5) Both inductors L_1 and L_2 operate in the DCM. Furthermore, the current in inductor $L_1(i_{L1})$ reaches zero level prior to the current in $L_2(i_{L2})$.
6) The phase shift of the input line current introduced by the input filter is minimal and can be neglected.

With these assumptions, the circuit operation over one switching period T_s can be described in three operating stages, as shown in Fig. 2.

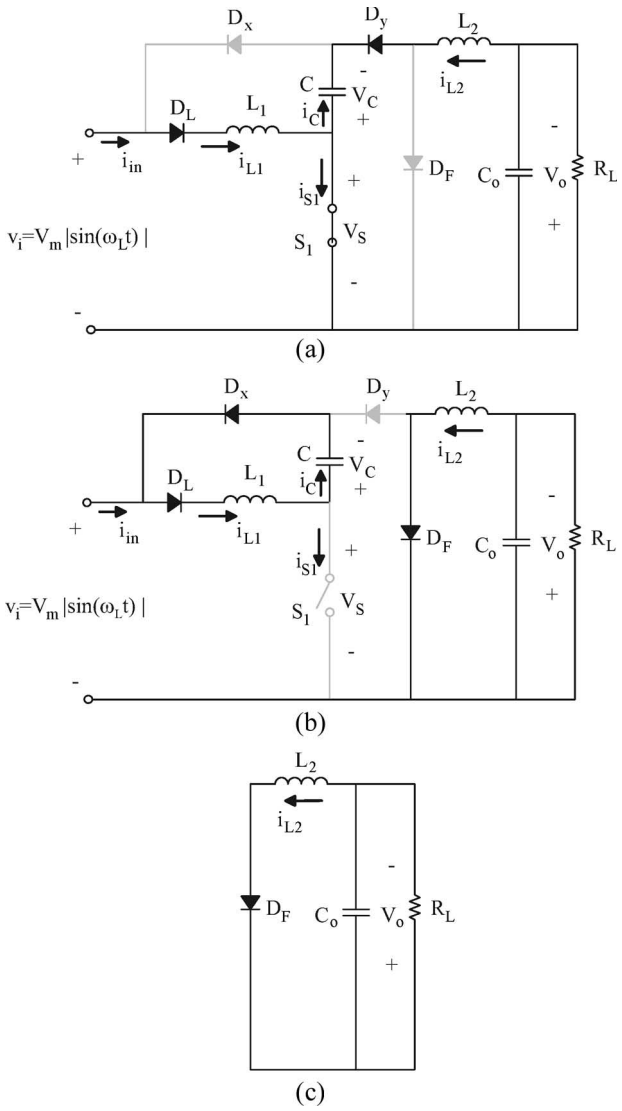

Fig. 2. Operating stages of the proposed converter. (a) Stage 1. (b) Stage 2. (c) Stage 3.

Stage 1 $[t_0, t_1]$*:* Prior to this interval, the currents through L_1 and L_2 are at ground level. When switch S_1 is turned on at $t = 0$, diode D_y becomes forward biased, and currents i_{L1} and i_{L2} begin to linearly increase. This interval ends when switch S_1 is turned off, initiating the next stage.

Stage 2 $[t_1, t_2]$*:* When the switch is turned off, diode D_y becomes reverse biased. Thus, current i_{L1} linearly decreases through diode D_x, whereas current i_{L2} linearly decreases at a rate proportional to output voltage V_o through the freewheeling diode D_F. This stage ends when current i_{L1} reaches the ground level. Diode D_L prevents current i_{L1} from becoming negative.

Stage 3 $[t_2, t_3]$*:* In this stage, current i_{L2} continues to decrease through the freewheeling diode D_F until it becomes zero. The converter stays in this stage until the switch is turned on again. To improve the overall efficiency, it is preferred to turn on the switch at $t = t_3$, which will reduce the current stresses through the semiconductor devices.

The characteristic ideal circuit waveforms during one switching period are shown in Fig. 3.

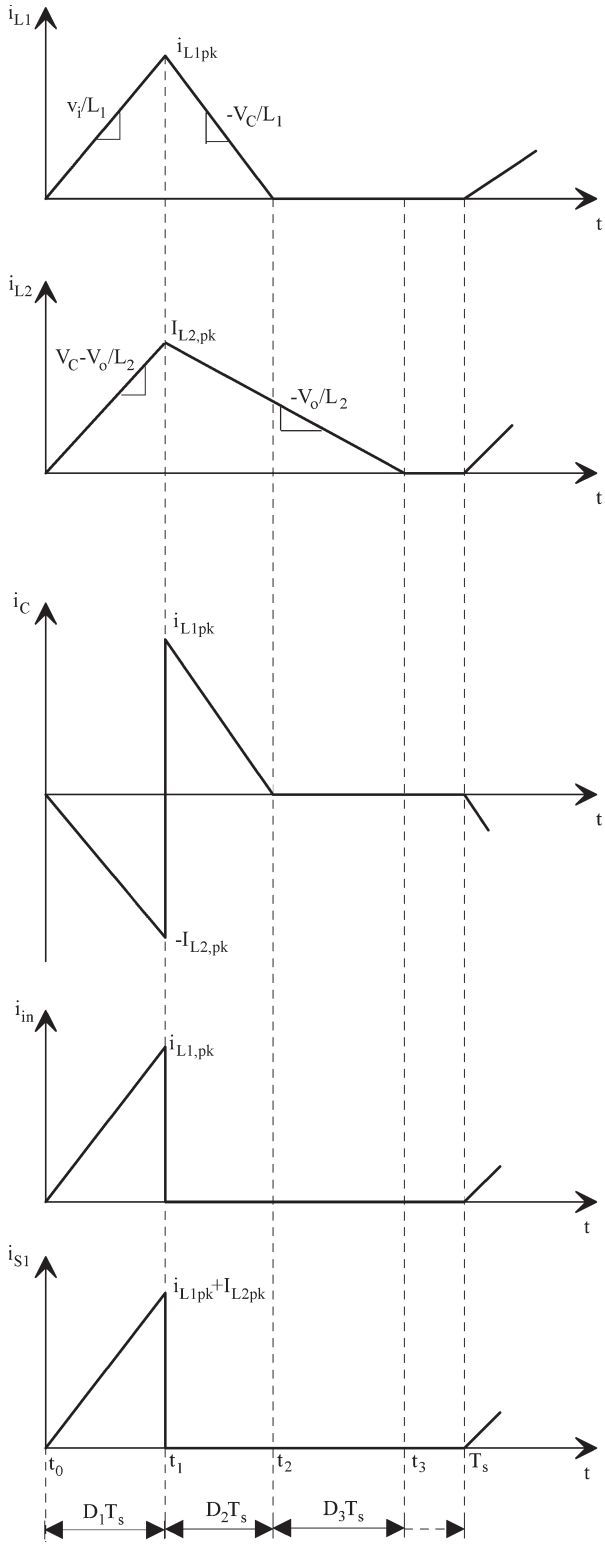

Fig. 3. Idealized waveforms.

III. Theoretical Analysis

A. Conditions for DCM

The normalized switch-off time defined by D_2 and D_3 can be found in terms of switch duty cycle D_1 by applying voltage-second to both L_1 and L_2, respectively, which gives

$$D_2 = D_1 \frac{v_i}{V_C} \tag{1}$$

$$D_2 + D_3 = \left(\frac{V_C - V_o}{V_o}\right) D_1. \tag{2}$$

To maintain a sinusoidal input current, L_1 must operate in DCM over the entire ac line cycle. For inductor L_1 to operate in DCM, the following condition must be held:

$$D_2 \leq 1 - D_1. \tag{3}$$

The condition for inductor L_2 to be in DCM is satisfied if

$$D_2 + D_3 \leq 1 - D_1. \tag{4}$$

Simplifying (3) and (4) by using (1) and (2) gives the following results:

$$\frac{v_i}{V_o} \leq \frac{1 - D_1}{D_1^2} \tag{5}$$

$$D_1 \leq \frac{V_o}{V_C}. \tag{6}$$

Note that, from (5), the condition for L_1 to be in DCM can be always satisfied over the entire ac line period, while the worst case must be satisfied when $v_i = V_m$. Moreover, the assumption is that the current in L_2 reaches zero level after the current in L_1 is also satisfied since $D_1 + D_2 \leq D_1 + D_2 + D_3$.

Operating L_2 in BCM requires the sum of the normalized subintervals length to be unity, i.e., $D_1 + D_2 + D_3 = 1$; hence, the inequality in (6) will be modified to $V_o = D_1\ V_C$. It is important for L_2 to be in BCM in order to reduce the current stress on the semiconductor devices, leading to better overall efficiency improvement.

B. DC Capacitor Voltage V_C

The dc capacitor voltage V_C determines the voltage stress across switch S_1 and diodes D_x and D_y. Therefore, it is an important design factor. Voltage V_C can be found by applying charge balance on C in a half-line cycle $T_L/2$. The average capacitor current over $T_L/2$ is

$$\langle i_C(t)\rangle_{T_L/2} = \frac{2}{T_L} \int_0^{T_L/2} \langle i_C(t)\rangle_{T_s}\, dt. \tag{7}$$

The averaged value of the capacitor current over one switching period T_s, i.e., $\langle i_C(t)\rangle_{T_s}$, can be found from Fig. 3 as

$$\langle i_C(t)\rangle_{T_s} = \frac{1}{2}\left[D_2 i_{L1\mathrm{pk}}(t) - D_1 I_{L2\mathrm{pk}}\right]. \tag{8}$$

Equation (7) must be equal to zero at steady state. Substituting (8) into (7) and solving for V_C give

$$V_C = \frac{V_o}{2}\left[\sqrt{1 + \frac{2L_2}{L_1 M^2}} + 1\right] \tag{9}$$

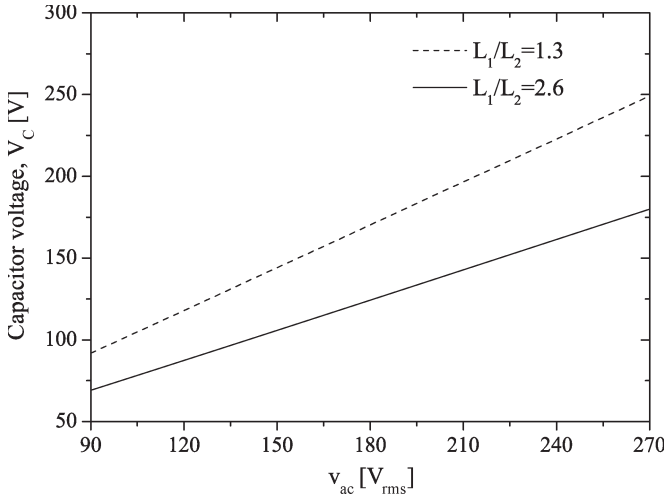

Fig. 4. Capacitor voltage V_C as a function of ac line voltage $v_{\rm ac}$ ($V_o = 24$ V, and L_1 and L_2 are in DCM).

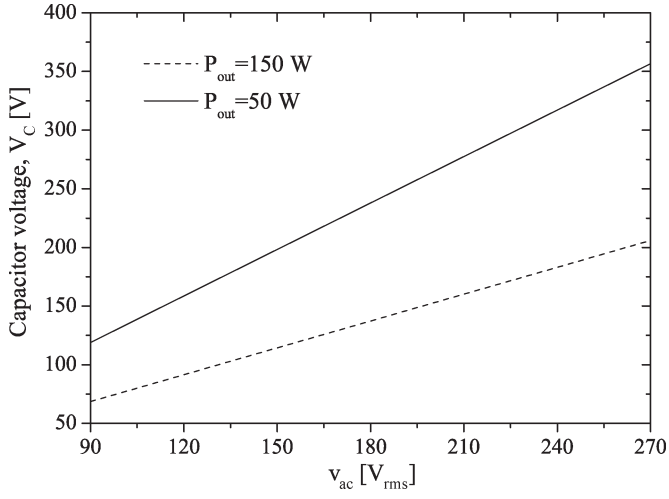

Fig. 5. Capacitor voltage V_C as a function of ac line voltage $v_{\rm ac}$ ($V_o = 24$ V, $f_s = 50$ kHz, $L_1 = 66$ μH, and L_1 in DCM and L_2 in CCM).

where $M = V_o/V_m$ is the voltage conversion ratio. Thus, for a given value of M, capacitor voltage V_C is independent of load current variation, and it is a function of inductance ratio L_1/L_2. This effect was first reported in [4]. Since then, several studies about this effect have been reported in the literature [6], [7], [19], and [24].

Fig. 4 shows the variation in capacitor voltage V_C as a function of line voltage $v_{\rm ac}$, with the ratio L_1/L_2 as a parameter. It is clear from Fig. 4 that higher values of inductance ratio L_1/L_2 tend to reduce the voltage stress on capacitor C and, hence, on power switch S_1. This is true since the capacitor charging and discharging currents are inversely proportional to L_1 and L_2, respectively. Moreover, from Fig. 4, when $L_1/L_2 = 2.6$, voltage V_C is about 69 V at low-line input voltage and about 177 V at high-line input voltage. Therefore, a 600-V power metal–oxide–semiconductor field-effect transistor switch suffices.

However, increasing the value of L_1/L_2 beyond a certain value will force L_1 to leave the DCM region, which will degrade the quality of the input line current. Thus, there is an upper bound limit for ratio L_1/L_2, which can be found from (5), (6), and (9) as

$$\frac{L_1}{L_2} \leq \frac{1}{2M}. \tag{10}$$

From (10), the upper bound limit of L_1/L_2 is determined by the output voltage and low-line ac voltage.

For the sake of comparison, when L_2 operates in CCM, then V_C depends on both line voltage $v_{\rm ac}$ and load power $P_{\rm out}$, and is given by

$$V_C = \frac{V_m}{2}\sqrt{\frac{R_L}{f_s L_1}}. \tag{11}$$

A plot of (11) for two different output power levels is shown in Fig. 5. Nevertheless, the voltage stress on capacitor C is still below 450 V for load variation from full load to one third of full load.

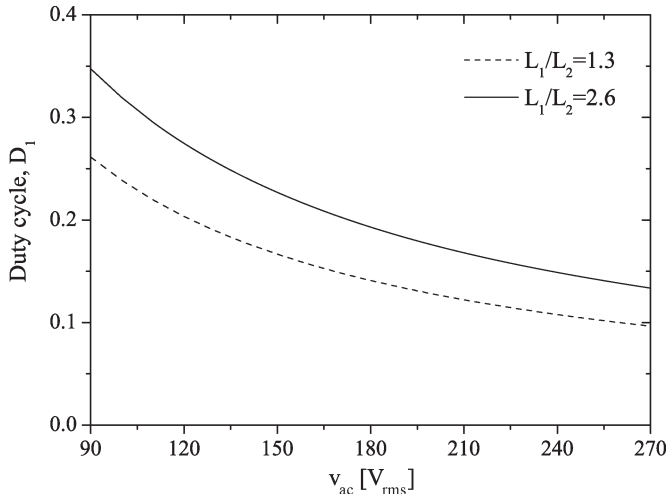

Fig. 6. Variation of duty cycle D_1 as a function of ac line voltage $v_{\rm ac}$ ($V_o = 24$ V, L_1 in DCM, and L_2 in BCM).

Furthermore, when L_2 is in BCM, then duty cycle D_1 can be obtained from (6) and (9) as

$$D_1 = \frac{V_o}{V_C} = \frac{L_1 M^2}{L_2}\left[\sqrt{1 + \frac{2L_2}{L_1 M^2}} - 1\right]. \tag{12}$$

Equation (12) shows that D_1 is independent of load current variation, yet it must be kept constant for a given value of M. This implies that the switching frequency must vary in order to compensate for load current variation. Fig. 6 shows the variation of duty cycle D_1 as a function of ac line voltage for different values of inductance ratio L_1/L_2.

C. Voltage Conversion Ratio M

The voltage conversion ratio $M = V_o/V_m$ in terms of circuit parameters can be found by applying the input–output power

balance principle to the circuit in Fig. 1. The average input power during one half-cycle of the line voltage is

$$\langle p_{\rm in}(t)\rangle_{T_L/2} = \frac{2}{T_L}\int_0^{T_L/2} v_i \langle i_{\rm in}(t)\rangle_{T_s}\, dt. \tag{13}$$

From Fig. 3, the average input line current over one switching period $\langle i_{\rm in}(t)\rangle_{T_s}$ is

$$\langle i_{\rm in}\rangle_{T_s} = \frac{1}{2}D_1 i_{L1{\rm pk}}(t) = \frac{v_i}{R_e} \tag{14}$$

where R_e is the emulated input resistance of the converter, and it is equal to

$$R_e = \frac{2L_1}{D_1^2 T_s}. \tag{15}$$

For a given operating point (M, R_L), the emulated input resistance in (15) is constant if both D_1 and T_s are kept constant. Thus, the converter presents a linear resistive load to the ac power main, which is the perfect condition for unity power factor (UPF) operation. Evaluating (13) and applying the power balance between the input–output ports, the desired voltage conversion ratio M is

$$M = \sqrt{\frac{\eta}{2K}}D_1 \tag{16}$$

where η is the converter efficiency, and the dimensionless parameter K is defined by

$$K = \frac{2L_1}{R_L T_s}. \tag{17}$$

D. Inductances L_1 and L_2

The critical value of $K(K_{\rm crit})$ required for L_1 to be in DCM is found by rearranging (5) and (16), which gives

$$K_{\rm crit} = \frac{1}{2}\left(\frac{1-D_1}{D_1}\right)^2. \tag{18}$$

For values of $K \le K_{\rm crit}$, then L_1 is operating in DCM; otherwise, L_1 will enter the CCM region. Note that the proposed converter has a wider range of voltage conversion ratio when it is compared to the conventional buck–boost converter, which has $K_{\rm crit} = (1-D_1)^2/2$.

The critical value of $L_1(L_{1,\rm crit})$ required for DCM operation occurs at maximum output power $R_{L,\min}$ and at the peak of the low-line voltage $V_{m,\min}$. Using (16)–(18) gives $L_{1,\rm crit}$ as

$$L_{1,\rm crit} = \frac{R_{L,\min}T_{s,\max}}{16}\left[-1+\sqrt{1+\frac{4V_{m,\min}}{V_o}}\right]^2. \tag{19}$$

For values of $L_1 > L_{1,\rm crit}$, the converter enters the CCM region, where (16) is no longer valid. In CCM, there are only two operating stages per switching cycle, i.e., Fig. 2(a) and (b). The voltage conversion ratio in CCM can be expressed by $M = 2D_1^2/[\pi(1-D_1)]$, which can be derived by equating the average capacitor current during a half-cycle to zero and applying the power balance between the input–output ports. However, operating L_1 in the CCM region results in a more distorted input line current and a lower input power factor than in the DCM region. The best choice for the value of L_1 is to be close to $L_{1,\rm crit}$ since this will reduce the ripple value of input current $i_{\rm in}$. The DCM characteristic is plotted in Fig. 7 for several values of K. Note that the CCM/DCM boundary line in Fig. 7 is valid for $\omega t = \pi/2$, i.e., when $v_i = V_m$, which gives the minimum required value of $K_{\rm crit}$.

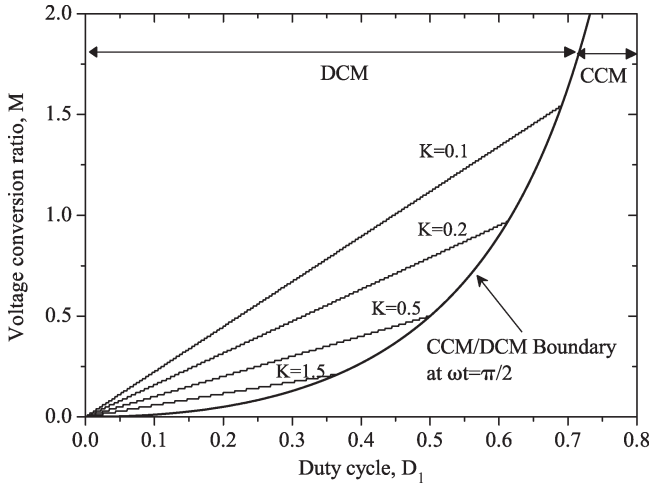

Fig. 7. Voltage conversion ratio M as a function of duty cycle D_1 for several values of K.

Similarly, the condition for inductor L_2 to operate in DCM occurs when the average output current $\langle i_{L2}\rangle_{T_s} \le I_{L2,\rm pk}/2$, Fig. 1. Thus, the minimum value of $L_2(L_{2,\rm crit})$ can be found as

$$L_{2,\rm crit} = \frac{R_{L,\min}T_{s,\max}}{2} \times\left[1-\frac{V_o}{2V_{m,\min}}\left(-1+\sqrt{1+\frac{4V_{m,\min}}{V_o}}\right)\right]. \tag{20}$$

For L_2 to operate in BCM, then the value of L_2 must be equal to $L_{2,\rm crit}$.

E. Averaged Circuit Model

The averaged model for the converter of Fig. 1 when both inductors L_1 and L_2 are in DCM is derived here based on averaging various waveforms over one switching cycle T_s. The averaged diode D_x and D_y currents are given by

$$\langle i_{\rm Dx}\rangle_{T_s} = \frac{v_i^2}{v_C R_e} = \frac{\langle p_{\rm ac}(t)\rangle_{T_s}}{v_C} \tag{21}$$

$$\langle i_{\rm Dy}\rangle_{T_s} = \frac{V_o^2}{\eta R_L v_C} = \frac{\langle p_{\rm dc}(t)\rangle_{T_s}}{\eta v_C} \tag{22}$$

and the average voltage across output diode D_F is equal to

$$\langle v_{\rm DF}\rangle_{T_s} = G_0 v_C \tag{23}$$

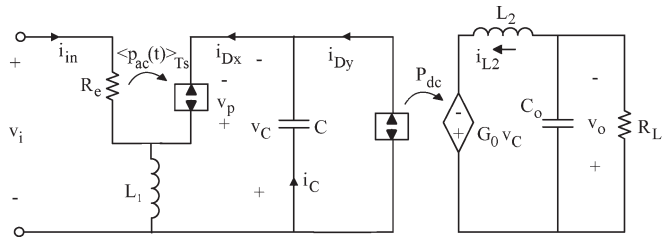

Fig. 8. Averaged circuit model in DCM (Both L_1 and L_2 are in DCM.).

where G_0 is given by

$$G_0 = \frac{\eta L_1 R_L}{2L_2 R_e}\left[\sqrt{1+\frac{4L_2R_e}{\eta L_1 R_L}}-1\right]. \tag{24}$$

By using (14) and (21)–(23), a complete averaged model for the proposed PFC can be obtained, as shown in Fig. 8, which is based on the "Loss-Free-Resistor" concept presented in [30] and [32]. Note that if this model is implemented by PSPICE, then a large resistor must be inserted across capacitor C to avoid floating problems. Moreover, the power sources elements in Fig. 8 can be modeled in PSPICE as a "voltage-controlled current source." Moreover, the model is also valid when L_2 operates in CCM, provided that coefficient G_0 is replaced by duty cycle D_1.

The averaged model is helpful in finding the exact steady-state low-frequency ripple waveforms as well as the open-loop system transient response. From Fig. 8, capacitor current i_C can be written as

$$C\frac{dv_C(t)}{dt} = \frac{v_i^2(t)}{R_e v_C(t)} - G_0^2\frac{v_C(t)}{\eta R_L}. \tag{25}$$

Eliminating the intermediate steps, the exact expression for the capacitor voltage is obtained as

$$v_C(t) = \left[-(B_0+B_1)e^{-yt} + B_0 + B_1\cos(2\omega_L t) + B_2\sin(2\omega_L t)\right]^{1/2} \tag{26}$$

where

$$y = \frac{2G_0^2}{\eta R_L C} \qquad B_0 = \frac{P_{\rm dc}R_L}{\eta G_0^2}$$

$$B_1 = \frac{-B_0}{1+\left(\frac{\omega_L R_L C}{G_0^2}\right)^2} \qquad B_2 = \frac{\omega_L R_L C}{G_0^2}B_1.$$

The peak–peak low-frequency voltage ripple on capacitor C can be evaluated from (26) as

$$\Delta v_{C,\rm p-p} = \sqrt{B_0 - B_2} - \sqrt{B_0 + B_2}. \tag{27}$$

The time-variant expression for output voltage $v_o(t)$ and the peak–peak low-frequency output voltage ripple can be simply obtained by multiplying both (26) and (27) by coefficient G_0. The maximum peak voltage ripple of v_C occurs at low-line voltage and at maximum power throughput. Theoretical transient waveforms are plotted in Fig. 9 for the following values: $v_i = 90\ V_{\rm rms}$ at 50 Hz, $P_o = 150$ W, $V_o = 24$ V, $L_1/L_2 = 2.6$, and $C = 1.5$ mF.

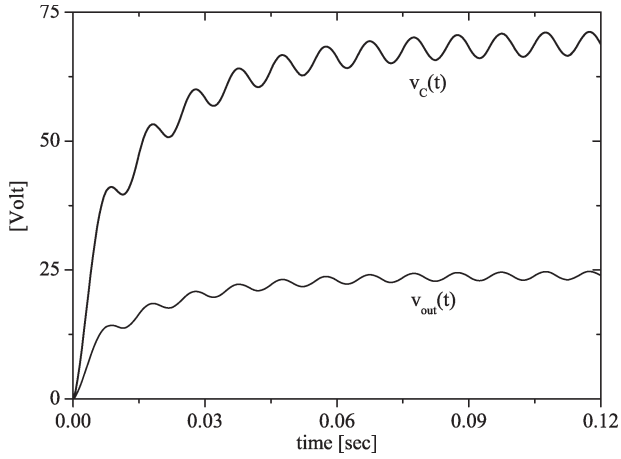

Fig. 9. Turn-on transient waveforms.

TABLE I
SEMICONDUCTOR VOLTAGE STRESS

S_1	D_x	D_y	D_F
V_m+V_C	V_m+V_C	V_m	V_C

IV. DESIGN CONSIDERATION

In general, when operating a converter in the DCM region, the current stress on the converter components becomes relatively large when compared to the CCM operation, and this is one disadvantage of the DCM operation, which limits this operating mode to low-power applications (< 150 W). Considerations for the rating and selection of the various components for the proposed converter are presented next for the DCM/BCM operating mode.

A. Semiconductors Stresses

The voltage stresses across the semiconductors in terms of peak line voltage V_M and capacitor voltage V_C are shown in Table I, whereas the closed-form expressions for the rms currents (over half-line cycle $T_L/2$) for the switch and the diodes of Fig. 1 are given as

$$I_{S,\rm rms} = \frac{P_{\rm out}}{\sqrt{3}\eta V_{\rm ac,rms}}\sqrt{\frac{4}{D_1}+\frac{16}{\pi M}+\frac{2D_1}{M^2}} \tag{28}$$

$$I_{\rm Dx,rms} = \frac{P_{\rm out}}{3\eta V_{\rm ac,rms}}\sqrt{\frac{32}{\pi M}} \tag{29}$$

$$I_{\rm Dy,rms} = \frac{P_{\rm out}}{\eta M V_{\rm ac,rms}}\sqrt{\frac{2D_1}{3}} \tag{30}$$

$$I_{\rm DF,rms} = \frac{P_{\rm out}}{\eta {\rm M} V_{\rm ac,rms}}\sqrt{\frac{2\left(1-D_1\right)}{3}}. \tag{31}$$

Fig. 10 shows the effect of the input voltage variations on the semiconductors rms currents for $P_{\rm out} = 150$ W, $\eta = 100\%$,

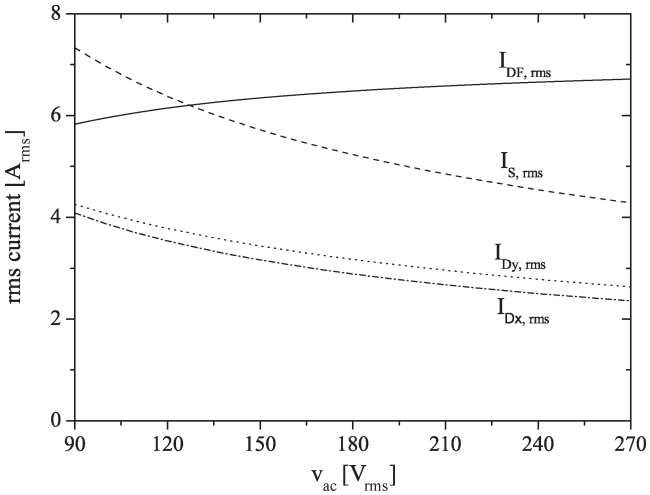

Fig. 10. Semiconductors full-load rms current stress as a function of ac line voltage $v_{\rm ac}$.

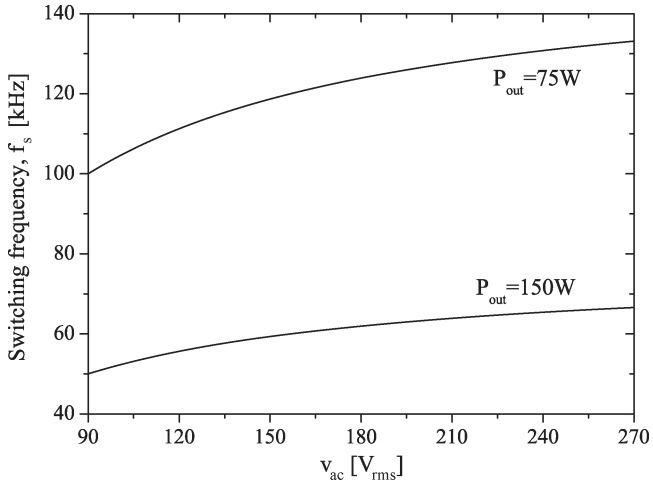

Fig. 11. Switching frequency as a function of ac line voltage $v_{\rm ac}$ ($V_o = 24$ V, and $L_1/L_2 = 2.6$).

$V_o = 24$ V, and $L_1/L_2 = 2.6$. The worst case rms current stress for switch S_1 and diodes D_x and D_y happens at low-line input and maximum output power, whereas the current stress in diode D_F slightly varies as the ac line voltage varies.

B. Passive Elements Stresses and Selection

Similarly, the closed-form expressions for the rms currents in the passive elements L_1, L_2, C, and C_o are given by

$$I_{L1,\rm rms} = \frac{P_{\rm out}}{\eta V_{\rm ac,rms}}\sqrt{\frac{4}{3D_1}+\frac{32}{9\pi M}} \tag{32}$$

$$I_{L2,\rm rms} = \frac{P_{\rm out}}{\eta {\rm M} V_{\rm ac,rms}}\sqrt{\frac{2}{3}} \tag{33}$$

$$I_{C,\rm rms} = \frac{P_{\rm out}}{\eta V_{\rm ac,rms}}\sqrt{\frac{32}{9\pi M}+\frac{2D_1}{3M^2}} \tag{34}$$

$$I_{\rm co,rms} = \frac{P_{\rm out}}{\sqrt{6}\eta M V_{\rm ac,rms}}. \tag{35}$$

The energy storage capacitor C must be large enough to ensure that it does not ring with L_1 or with L_2 during switching period T_s. Moreover, from (27), the required value of C can be obtained in terms of twice the line-frequency peak voltage ripple ($\Delta v_{C,\rm p-p}$) as

$$C = \frac{G_0^2}{\omega_L R_L\sqrt{1-\left(1-\frac{\Delta v_{C,\rm p-p}^2 G_0^2}{2V_o^2}\right)^2}}. \tag{36}$$

On the other hand, a relatively small bulk capacitor C_o is required at the output port to filter the high-frequency switching current ripples presented in L_2. The amount of capacitance necessary to meet the output high-frequency peak–peak ripple voltage ($\Delta v_{\rm o-hf}$) requirements when L_2 in BCM is given by

$$C_o = \frac{V_o}{4R_L f_s \Delta v_{\rm o-hf}}. \tag{37}$$

C. Control Consideration

The control of the proposed converter can be either a simple variable duty-cycle fixed-frequency control or a fixed duty-cycle variable-frequency control. Both control methods have almost no effect on either the line current quality or the voltage variation across energy storage capacitor C.

When the BCM operation is desired for inductor L_2, then it is necessary to sense for the zero-current point in L_2 prior to switch turn-on, hence disallowing fixed-frequency operation in this mode. The variation in the switching frequency depends on the output load and/or the input line voltage. Thus, for a normal operating mode, i.e., when M and R_L are fixed, then the time variation of the input ac voltage has no effect on the switching frequency. This is true, as shown in Fig. 3; the current waveform of L_2 does not depend on the input voltage, but rather it relatively depends on constant voltages, capacitor voltage V_C, and output voltage V_o.

The minimum switching frequency $f_{s,\rm min}$ required for the DCM/BCM operation is a design parameter, and it happens at low-line voltage and at maximum load power; the maximum switching frequency is given by

$$f_{s,\rm max} = \frac{R_L(1-D_1)f_{s,\rm min}}{R_{L,\rm min}\left(1-\frac{V_o}{v_{\rm ac,min}}\sqrt{K_{\rm crit}}\right)} \tag{38}$$

where $K_{\rm crit} = (2L_{1\rm crit}f_{\rm design}/R_{L,\rm min})$, and D_1 is given by (12). The effect of line voltage variation on the switching frequency is shown in Fig. 11 for the full-load and half-load cases. The variable-frequency control becomes unsuitable when the load varies by more than one fifth of the full load due to a large variation in the switching frequency.

When the converter is designed to operate at a constant duty cycle D_1, then an undesirable steady-state low-frequency (double the line frequency) ripple is produced in output voltage V_o (Fig. 9). This is not a desirable characteristic in a single-stage PFC since the objective of providing a tight and fast output voltage regulation is lost. However, the low-frequency-related ripple can be simply eliminated from the output voltage without degrading the line current waveform by implementing

a high-bandwidth (well above twice the line frequency) control loop. This can be accomplished by controlling switch duty cycle D_1 such that the average output inductor current during each switching period $\langle i_{L2}\rangle_{T_s}$ is constant, i.e., equal to the average load current $I_{\rm RL}$ [9]. From Fig. 3, the average output inductor current during each switching period can be expressed as

$$\langle i_{L2}\rangle_{T_s} = \frac{D_1^2 T_s V_C\,(V_C - V_o)}{2L_2 V_o}. \tag{39}$$

Hence, from (39), the required duty cycle D_1 to keep $\langle i_{L2}\rangle_{T_s}$ equal to I_o is

$$D_1(t) = \sqrt{\frac{2P_{\rm out}}{T_s V_C\left(\frac{V_C - V_o}{L_2}\right)}}. \tag{40}$$

Equation (40) shows that, if the voltage ripple on the energy storage capacitor C is small, then regulating the output voltage is sufficient to insure a constant i_{L2}. In this case, the duty cycle remains relatively constant during a half-line cycle. Therefore, the fast controller has almost no effect on the emulated input resistance (15) of the converter, which is a desirable feature.

V. Simulation and Experimental Results

The converter of Fig. 1 is simulated using PSPICE for the following input and output data specifications:

- input voltage: 110 $V_{\rm rms}$ at 50 Hz;
- output voltage: 20 V $\pm$ 2%;
- maximum load power: 50 W;
- minimum switching frequency: 60 kHz.

Input inductor L_1 is designed for the DCM operation, whereas L_2 is designed for the BCM operation. The circuit components are calculated based on the analysis performed in previous sections, and they are given as $L_1 = 100$ μH, $L_2 = L_{2,\rm crit} = 47$ μH, $C = 680$ μF, and $C_o = 100$ μF. Duty cycle D_1 is set to 0.22. A high-frequency input filter ($L_F =$ 2 mH, and $C_F = 0.68$ μF) is inserted after the bridge rectifier to filter the ripples in the rectified line current. PSPICE actual semiconductor models have been used to simulate the switches: IRF840 for the active switch and MUR1560 for the diodes. The simulated waveforms are shown in Fig. 12, which correctly demonstrates the DCM/BCM operating mode. The simulation result gives a total harmonic distortion in the input line current of about 1%. Moreover, it is clear from Fig. 12(c) that output voltage V_o has a significant low-frequency ripple, which is unacceptable for some specific applications. However, as discussed in Section IV-C, the low-frequency ripple in V_o can be greatly reduced by simply regulating the output voltage. Therefore, a simple feedback controller has been implemented to regulate V_o at 20 V. The simulated transient response of the input line current and output voltage to a step load change from 50% to 100% and vice versa is shown in Fig. 13. It can be observed from Fig. 13 that the related low-frequency ripple in the output voltage is almost negligible, and the output voltage is tightly regulated due to the high bandwidth of the loop.

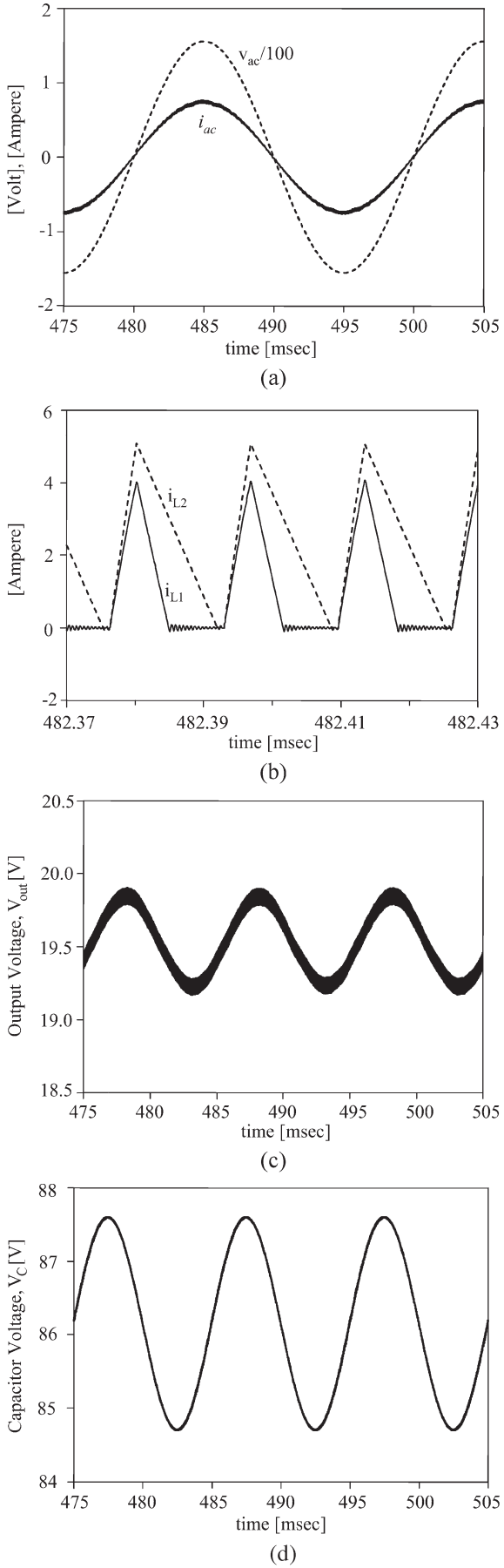

Fig. 12. PSPICE simulated waveforms.

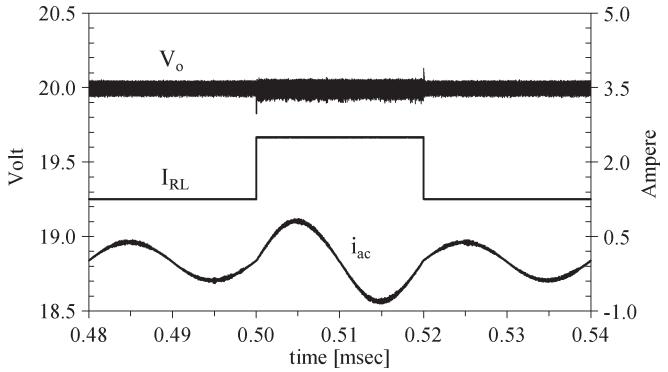

Fig. 13. Simulated closed-loop transient response of the output voltage (top trace), load current (middle trace), and input line current (bottom trace) when subjected to an output load change from 50% to 100% and back.

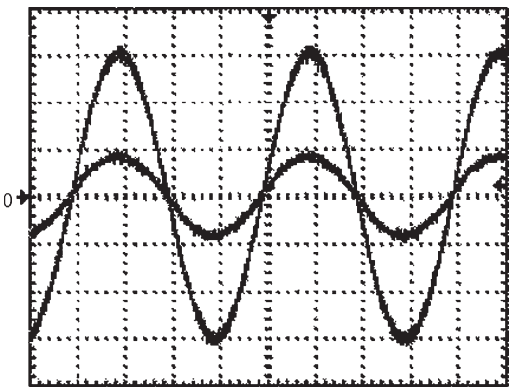

Fig. 14. Experimental waveforms: input line voltage of 50 V/div (higher peak) and filtered input line current of 1 A/div (lower peak) (horizontal scale: 5 ms/div).

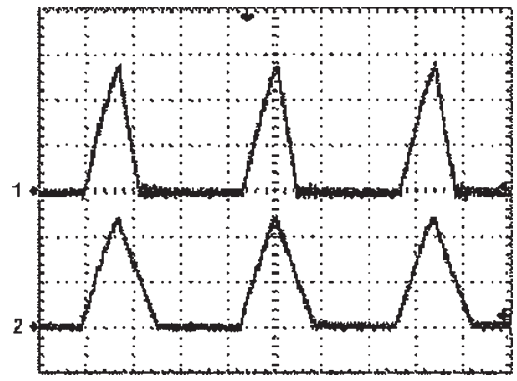

Fig. 15. Experimental waveforms: inductor L_1 current (upper trace) and inductor L_2 current (bottom trace) over several switching periods (vertical scale: 2 A/div, horizontal scale: 5 μs/div).

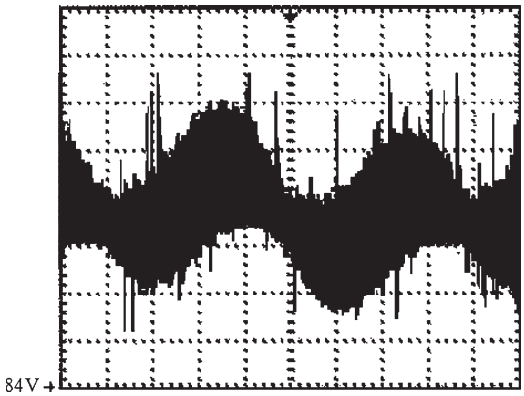

Fig. 16. Experimental waveforms: dc capacitor voltage V_C (vertical scale: 1.0 V/div, horizontal scale: 2.5 ms/div).

A laboratory prototype has been built to validate the theoretical results as well as the simulation previously described. The circuit parameters were all the same as those for simulation. The measured full-load efficiency was about 77%. It should be mentioned here that the laboratory prototype has been conceived on a proof-of-concept basis; therefore, it was implemented using standard "off-the-shelf" devices and components, including magnetics. The input voltage and the filtered input line current waveforms are shown in Fig. 14, whereas the discontinuous inductor currents i_{L1} and i_{L2} during couple switching frequencies are shown in Fig. 15. Moreover, the voltage on the energy storage capacitor V_C is shown in Fig. 16.

The measured waveforms are in a good agreement with the simulated ones given in Fig. 12. In addition, it can be observed from measured waveforms that the input current is nearly sinusoidal and the power factor is close to unity.

VI. Conclusion

In this paper, a converter topology is proposed by combining a buck–boost and a buck converter. As a result, a single-switch single-stage UPF with extended voltage conversion ratio capability is obtained.

The steady-state behavior has been studied and analyzed with performance characteristics, and a large-signal averaged model is presented. It has been shown that several advantages can be obtained by operating both input and output inductors in the DCM. These advantages include automatic PFC, low-voltage stress on the semiconductor components, zero-current switch turn-on, and a well-regulated output voltage with a small low-frequency voltage ripple. These advantages are gained at the expense of increasing current stresses in the power circuit components, which will limit the proposed converter for power applications to less than 150 W.

Moreover, the presented analysis shows that the converter is well suited for universal-line PFC applications. The performance of the proposed converter was experimentally verified on a 50-W universal-line range.

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