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DC-DC multiplier boost converter with resonant switching

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ABSTRACT

This paper proposes an improved Multilevel Boost Converter, also known as Multiplier Boost Converter, in which the spike-type current among capacitors is eliminated through one resonant inductor, achieving some resonant-type current waveforms. Experimental results demonstrate the applicability of the proposition.

1. Introduction

There are many practical applications where a Switching Mode Power Supply (SMPS) requires wide conversion ratios such as laser, X-ray systems, automotive, telecommunication, ion pumps, uninterruptible power supplies UPS, industrial systems, electrostatic systems, battery-powered portable devices, and renewable energy conversion systems [1–4]. For instance, PV panels and fuel cells generate a low amplitude dc-voltage that needs to be boosted to some hundred volts to feed grid-tie inverters. In telecom standard equipment, in order to provide Internet services, the 48 V of the DC battery set has to be boosted to a 380-V intermediate DC bus, etc.

Conventional transformerless topologies are not suitable to effectively perform the mentioned tasks, so that transformer or coupled-inductor-based topologies are commonly used [5,6]. However, it is also known that there exist several disadvantages with respect to the use of transformers such as: size, weight and frequency limitation for the resultant topologies. For this reason, there exists an increasing interest in the development of novel transformerless topologies that can perform efficiently through a wide conversion ratio [1–3,7–13].

In order to step-up or-down the voltage, several topologies have been proposed based on Switched Capacitor (SC) circuits that do not include transformers, providing high efficiency [3,7–13]. These topologies offer a state of the art solution, combining conventional converters with either switched capacitors voltage multipliers or dividers, depending on the converter's step-up or step-down mode, respectively.

For the stepping-up case, some propositions indicate that the combination of one conventional converter with a diode-capacitor voltage multiplier achieves a voltage gain that would be impractical for that converter [1–4,14–20].

Particularly, the multilevel boost converter [2], also known as multiplier boost converter, Fig. 1(a), combines the boost converter with the Cockcroft-Walton Voltage Multiplier for controlling the output voltage by pulse width modulation (PWM), achieving a high voltage gain because the diode-capacitor voltage multiplier.

There are different ways for implementing the voltage multiplier stage; Fig. 1 shows three of them. The advantage of the topology in Fig. 1(a) is that all capacitors hold the same voltage,

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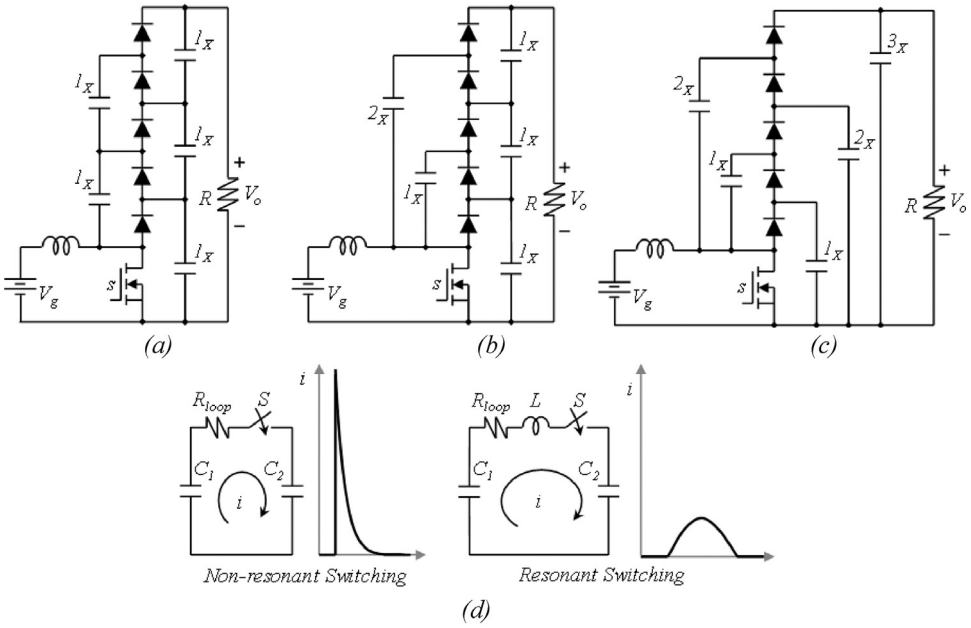

Fig. 1. (a), (b) and (c) Multiplier boost converters, (d) current among capacitors depending on the switching behavior.

which is relatively low. On the other hand, in Fig. 1(b), capacitor 2_X holds twice of the voltage on the others. However, it has been shown in [15] that by separated capacitors in the voltage multiplier, Fig. 1(b), the converter attains better performance.

A similar analysis may be applied to the capacitor bank on the right side, which would lead to the scheme depicted in Fig. 1(c). Such circuit does not have been reported in the open research. It represents the starting point of the proposed topology. The capacitors' labels indicate the voltage across them, assuming 1_X the voltage of a boost converter.

Diode-capacitor voltage multipliers are unidirectional Switched Capacitor (SC) converters operated in full charge interchange [7]. Their primary drawback is the current waveform among capacitors (through diodes), which are spike-shape [2–4,7,14,15,18,20], Fig. 1(d). The current in this case is limited only by the parasitic resistance in the loop. A major disadvantage of currents with spikes is that such condition force overrating in the components. This leads to a sub-utilization of the installed devices because switching devices are not designed to drain an average current that is much smaller than their peak current. Moreover, conduction losses in MOSFETS and capacitors are proportional to the RMS current, and then, the spikes lead to higher conduction losses on those components, even for low average currents. This situation worsens using devices with smaller parasitic resistance.

Resonant switching has proved to overcome this issue with a reasonable size and cost in topologies combining conventional converters with diode-capacitor voltage multipliers [21]. Fig. 1(d) illustrates the current between two capacitors in both the non-resonant and resonant switching, for the same charge interchange (same area under the current waveforms). The non-resonant switching reaches a larger peak current. The peak increases if the parasitic resistance decreases. It is expected that new devices will get lower parasitic resistance increasing this issue, which increases the EMC difficulties [22]. The current in the resonant switching branch exhibits a lower maximum peak. For this reason, it is highly desirable to achieve resonant switching in the diode-capacitor voltage multiplier.

This paper proposes an improved version of the multiplier boost converters based on resonant switching. Moreover, the principle may be extended to other hybrid converters, which use voltage multipliers. The proposed converter achieves a high voltage gain without the use of extreme duty cycles or transformers. The main characteristics become: (i) every switching device blocks a similar voltage; (ii) the input current is naturally continuous while the converter includes only one inductor for energy storage.

The paper is organized as follows. Section 1 provides the state of the art, motivation and introduction. Section 2 exposes the proposed topology and simulation waveforms to explain the theoretical analysis. Section 3 presents design guidelines with an easy and innovative point of view. Experimental results validate the approach in Section 4, and the conclusions of Section 5 close the paper.

2. Proposed topology

The main objective of the topology design is to implement resonant switching in the diode-capacitor voltage-multiplier for improving the operation.

Adding an inductor for resonant switching somewhere in the circuit, would cause a resonant-type waveform in a couple of capacitors while the rest of them will still present spikes. To connect a small resonant inductor in series with each capacitor becomes undesirable since the number of components would increase, moreover the output impedance would also be degraded if an inductor is in series with the output capacitor.

In the proposed topology only one resonant inductor is necessary in order to shape the current for all the switching devices, making it resonant when the inductor is connected as in Fig. 2(a). This situation is possible since this is the only point (apart from the ground) for draining the current among capacitors during both switching stages. Diodes in Fig. 2 are termed s_2 to s_6, to avoid confusions with the duty cycle.

2.1. Boost converter stage

Assuming small ripple and continuous conduction mode [29] for the energy storage inductor L, its average voltage becomes,

$$L\frac{d\left\langle i_L\right\rangle}{dt} = \langle v_L\rangle = V_g - (1-d)\langle v_1\rangle \tag{1}$$

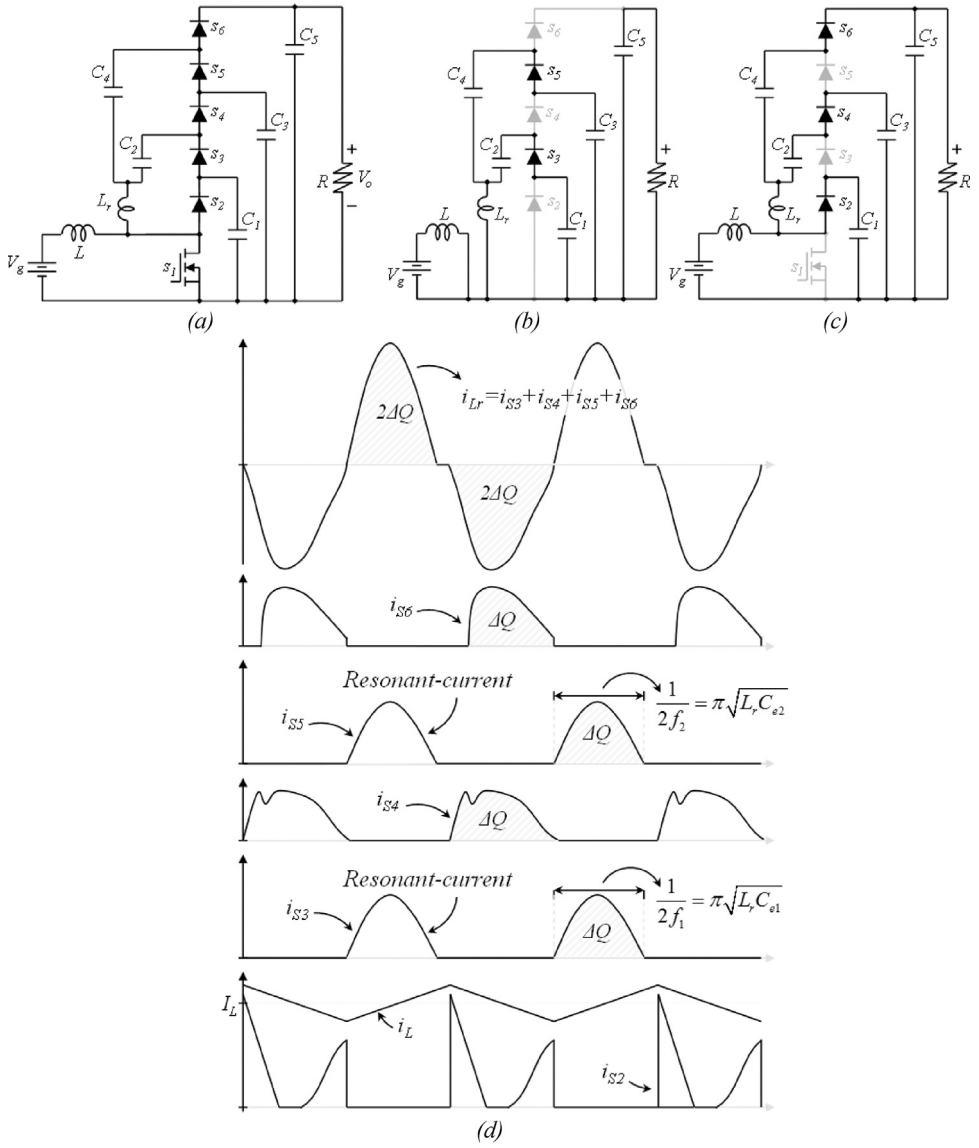

Fig. 2. Multiplier boost converter with resonant current among capacitors.

where d is the converter's duty cycle defined as the time when the switch s_1 is *on* over the total switching period T, v_g and v_1 are the input voltage and the voltage across C_1, respectively. At steady state, the average voltage across L is zero. Assuming that the derivative in Eq. (1) is zero the voltage across C_1 may be expressed by,

$$V_1 = \frac{1}{1-D}V_g \tag{2}$$

Note that capital letters indicate steady state values. Thus, the converter has two equivalent circuits according to the switching state. When the switch is *on*, the converter behaves as the circuit depicted in Fig. 2(b). For the *off* condition, the converter behaves as the circuit in Fig. 2(c).

2.2. Applicability to other circuits

It is noteworthy that the above-mentioned principle may be applied to the other voltage multipliers embedding a resonant inductor at the bus where the energy storage capacitor is connected to the voltage multiplier stage. For instance, Fig. 3 illustrates this principle on two topologies [15].

2.3. Voltage multiplier stage

This subsection introduces the voltage-multiplier operation and exhibits important waveforms obtained from simulations. When

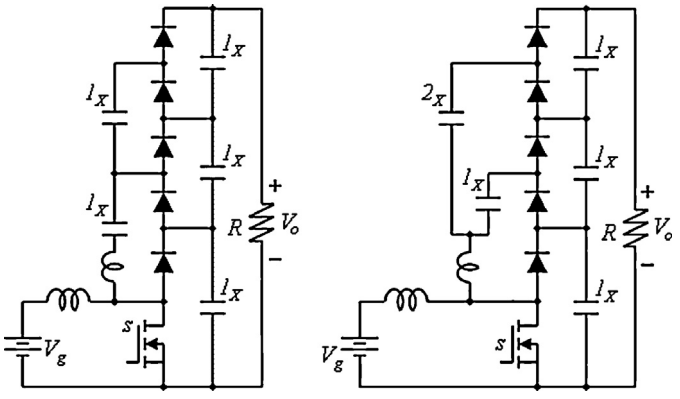

Fig. 3. The same principle can be used in other voltage multipliers.

the switch is *on*, capacitor C_1 transfers charge to C_2 through s_1, s_3 and the resonant inductor L_r.

L_r is used for resonance purposes, not for energy storage. Consequently, it is several hundred times smaller than the main inductor L, and its stored energy may be neglected. Ideal switches and capacitors large enough to operate with a small ripple are assumed [29]. The switched capacitor action creates the same steady state voltage in C_2 and C_1.

Fig. 2(d) displays the current i_L through the energy storage inductor. Notice that when current i_L starts rising, a resonant current i_{S3} flows through s_3, Fig. 2(b). The integral of i_{S3} becomes the charge that C_1 transfers to C_2. If the inductor is removed, the current would be non-resonant as shown in Fig. 1(d), leading to higher conduction losses in transistors and capacitors, and increasing the EMC issues.

When the switch is *off*, diode s_2 closes due to the current in L, connecting the negative side of C_2 to the same potential of the positive side of C_1, Fig. 1(c). Such quasi-series connection is in parallel with C_3, and then C_3 is charged with twice the voltage expressed in (2). Fig. 2(d) shows the current i_{S2} through s_2. Such current tends to be i_L but since L_r starts draining current (the one through s_4 and s_6), i_{S2} slowly decreases as i_{Lr} increases trying to reach i_L.

When the switch is *on* again, C_3 transfers charge to C_4 clamping it to the same voltage, and then both C_3 and C_4 hold twice the voltage in Eq. (2). The steady state current i_{S5} is also shown in Fig. 2(d).

When the switch is *off* again, the quasi-series connection of C_4 and C_1 charges C_5 to three times the boost converter voltage expressed in Eq. (2).

As in Fig. 1(c) capacitors hold different voltages. C_1, and C_2 hold a lower voltage, which corresponds to the conventional boost converter equation (2). C_3 and C_4 hold twice this voltage, while C_5 holds three times that voltage.

It is worth noting that capacitors lost their charge when transfer charge to others. However, as in any power converter, they may be selected correctly and keep their voltage in a certain acceptable range named *small ripple approximation* [29].

The current among diodes is the same in average, see Fig. 2(d). The area under the current is difficult to express from the waveform, but notice that the DC component of the output current is drained by all diodes (since the dc-current through capacitors become zero). The charge interchange ΔQ during one switching period is,

$$\Delta Q = \int_{t}^{t+T_S} i_{out}\,dt = I_{out}T_S \tag{3}$$

where I_{out} is the output current and T_S is the switching period. This definition is extensively used in the next section.

On the other hand, the current through the resonant inductor L_r is zero, since it is the sum of the current (zero in average) of two capacitors. In Fig. 2(d) the area under currents is the same for all diodes.

The current in the energy storage inductor L is shown at the bottom. It exhibits the conventional triangular waveform, which rises when the switch s_1 is *on* with a slope of (V_g/L), and decreases when the s_1 is *off*.

When s_1 closes, s_3 and s_5 also closes, Fig. 2(b), because the voltage in C_2 and C_4 has been discharged in the last switching cycle, and the current from C_1 and C_3 starts to charge them through s_3 and s_5, respectively, see i_{S3} and i_{S5} in Fig. 2(d). The current presents a semi-sinusoidal waveform; diodes prevent the negative semi-cycle.

Actually, there are two resonant circuits in this switching state, one composed by L_r and the series connection of C_1 and C_2, which resonant frequency becomes,

$$f_1 = \frac{\omega_1}{2\pi} = \frac{1}{2\pi\sqrt{L_r C_{e1}}} \tag{4}$$

where C_{e1} is the equivalent capacitance of the series connection C_1–C_2. The other resonant circuit is made by L_r and the series connection of C_3–C_4, which frequency is,

$$f_2 = \frac{\omega_2}{2\pi} = \frac{1}{2\pi\sqrt{L_r C_{e2}}} \tag{5}$$

where C_{e2} is the equivalent capacitance of the series connection C_3–C_4.

The resonant frequencies may be chosen to differ from each other but capacitors in voltage multipliers are usually selected to be equal, and in such case they generate the same resonant frequency. It is important to specify this frequency because charge-interchange depends on it. In order to avoid overlapping allowing the current to be zero and reducing switching losses, it is possible to set a minimum value of the duty cycle, see sub-section III.D.

When the current i_{S3} reaches zero (see Fig. 2(d)), the voltages across the capacitor C_2, v_2 is slightly larger than v_1 (v_2 is exactly equal to v_1 when the current reaches the maximum value), and s_3 keeps open the rest of the switching period (after the half of a sinusoidal cycle). Similarly with s_5 since v_4 is larger than v_3.

This causes that the circuit actually has more than two switching states. There is an equivalent circuit similar to Fig. 1(b) when s_3 and s_5 are *off*. The use of the averaging technique is still possible since the charge interchanged by capacitors is known, and the average current through the diodes is the same as the output current.

When the switch s_1 opens, s_2 closes because the current through L_r is zero and then the current through L is initially drained through s_2, which is closed, virtually connecting the negative side of C_2 and C_4 to the positive side of C_1. This tends to close s_4 and s_6 to transfer charge towards C_3 and C_5 from the charge in C_2 and C_4, respectively. This leads to a current increment through L_r, which is the sum of i_{S4} and i_{S6} at such moment, Fig. 2(d). When the current through L_r reaches the current in L, s_2 naturally opens. Thus i_{S2} becomes similar to Fig. 2(d). It tends to be i_L and then decreases to zero.

Currents i_{S4} and i_{S6} decrease as long as C_3 and C_5 are charged, reducing the current through L_r. When the current i_{Lr} is lower than i_L the rest of i_L smoothly closes s_2 again. The current tends to be i_L until the main switch s_1 closes in the next switching period.

3. Design guidelines

The selection of components main design guidelines is explained in this section.

3.1. Energy storage Inductor

The energy storage inductor L may be selected using the traditional method. Assume the equivalent circuit shown in Fig. 2(b), where the inductor is connected to the input voltage source V_g, during a period given by the duty cycle D times the switching period T_s. According to the desired current ripple Δi_L, the following expression may be used,

$$L\frac{di_L}{dt} = L\frac{\Delta i_L}{\Delta t} = V_g = L\frac{\Delta i_L}{DT_S} \tag{6}$$

Note that Eq. (6) assumes steady state and small ripple approximation for the input voltage V_g; Eq. (6) leads to Eq. (7),

$$L = \frac{V_g D T_S}{\Delta i_L} \tag{7}$$

3.2. Capacitors

The procedure for calculating the capacitors in a SMPS is similar to that for evaluating the inductor's energy storage in Eq. (7). This

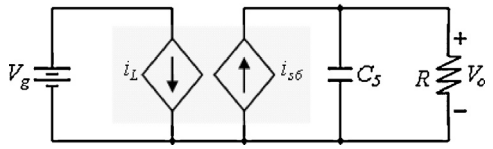

Fig. 4. Output capacitor decouples the load current shape effects.

holds for C_5, for example, when the switch is *on* (see Fig. 2), the capacitor C_5 is discharged with the output current,

$$C\frac{dv_C}{dt} = i_C = C\frac{\Delta v_C}{\Delta t} = \frac{V_5}{R} \tag{8}$$

Considering the time increment $\Delta t = DT_S$, the capacitor can be estimated as:

$$C_5 = \frac{V_5\Delta t}{\Delta v_5 R} = \frac{V_5 DT_S}{\Delta v_5 R} = \frac{V_5 D}{\Delta v_5 f_S R} \tag{9}$$

where V_5 is the dc-component of the voltage in capacitor C_5, Δv_5 is the voltage ripple (ac-component) expected for C_5, T_S is the switching period, and f_S is the switching frequency. If the resonant inductor L_r is too small this time is shorter.

For the worst case (or when the time is unknown) C_5 may be estimated by:

$$C_5 = \frac{V_5\Delta t}{\Delta v_5 R} = \frac{V_5 T_S}{\Delta v_5 R} = \frac{V_5}{\Delta v_5 f_S R} \tag{10}$$

This strategy is useful when the current has low ripple [29]. In switched capacitor structures this principle cannot be used because the current waveform. This subsection presents a convenient, innovative, and simplified method to calculate the capacitors in the switched capacitors stage.

Notice that at steady state, when the switch is *off*, C_5 receives through s_6 the total charge required for feeding the load. In the subsequent cycle, this charge is expressed by Eq. (3). This charge interchange always appears in the procedures for capacitors' selection. Actually, rewriting Eq. (9), the charge may be identified as the product of time and current,

$$C_5 = \frac{1}{\Delta v_5} \times DT_S \times \frac{V_5}{R} = \frac{1}{\Delta v_X} \times \Delta Q_X \tag{11}$$

where ΔQ_X, represents the amount of charge which is being interchanged. This principle may be used to calculate C_4. Note that the dc component of the load current is drained by all diodes (due to the null dc current through the capacitors), and then C_4 receives ΔQ, Eq. (3), through s_5 from C_3 when the switch is *on* (Fig. 2(b)); C_4 can be estimated as:

$$C_4 = \frac{1}{\Delta v_4} \times \Delta Q \tag{12}$$

where ΔQ is defined in Eq. (3) and Δv_4 is the voltage ripple expected for C_4. ΔQ, defined in Eq. (3), is different from ΔQ_X used as example in Eq. (11). The charge interchange may also be used to calculate C_3, C_2 and C_1 as,

$$C_3 = \frac{1}{\Delta v_3} \times \Delta Q; \quad C_2 = \frac{1}{\Delta v_2} \times \Delta Q; \quad C_1 = \frac{1}{\Delta v_1} \times \Delta Q \tag{13}$$

where Δv_3, Δv_2 and Δv_1 are the voltage ripples expected for C_3, C_2 and C_1, respectively.

Similarly, C_1 can be estimated. From Fig. 2, all the C_1's current discharge flows through s_3 in the resonant shape and its integral is equal to ΔQ Eq. (3).

Capacitor C_5 truly behaves as the boost output capacitor, which is charged from the input-part and discharged to the load, see Eq. (8). Thus, it is important to select C_5 and also decoupling the load effect to the input-part of the converter, Fig. 4.

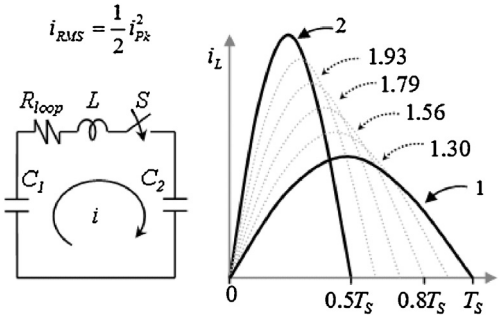

Fig. 5. Different possibilities for the resonant period if an RLC circuit.

3.3. RMS current in resonant type waveforms

The resonant period selection is important in applications where the resonant frequency should be controlled. For example, in high power converters where the switching frequency needs to be reduced, the resonant period of the multiplier stage may be selected to fill the full time of the *on*-state, Fig. 5. It is not recommended to design it too short since the losses in capacitors and MOSFETs are proportional to the RMS current. Fig. 5 illustrates different current waveforms with the same charge interchange (same area under the curve). The RMS value of a periodic current constituted by segments is:

$$rms = \sqrt{\sum_{k=1}^{n} D_k u_k} \tag{14}$$

where D_k is the duty cycle of the signal and u_k is the rms current of each segment, appendix two in [29]. Particularly, when the segments are half-sine waveforms, their u_k is expressed as the square of the peak value over two. In Fig. 5 the numbers besides the half-sine represent the square rms values normalized to the lower curve, since they have the same area under the curve. Selecting a resonant frequency that represents half of the period produces twice of losses in the mosfets, for the same output power.

3.4. Minimum duty cycle

Finally, the circuit's tradeoff needs to be discussed. There is a minimum duty cycle that can be selected during the design process. However, an inappropriate duty cycle reduces the circuit advantages.

Fig. 6 depicts the switching states and some important related waveforms. Fig. 6(a and b) shows the equivalent switching circuits, while Fig. 6(c) displays the inductor current and the resonant current through s_3. This current is equal to the current through s_5, if all capacitors have the same value. The resonant period may be selected using Eqs. (4) and (5), and the designer should make sure that the switch does not open before the resonant current reaches zero.

If the switch is open before the current reaches zero, the switching losses would increase and EMI will be generated due to the discontinuous current in some paths of the circuit. This constraint sets a minimum duty cycle for the converter, which can be expressed as the half-period of the resonant current (see Fig. 6(c)) divided by the switching period:

$$D_{\min} = \frac{1}{T_S}\pi\sqrt{L_r C_e} \tag{15}$$

As discussed previously, as wide the resonant current is, the RMS value is lower, reducing the conduction losses. This implies a larger minimum duty cycle, so that it is a tradeoff between the

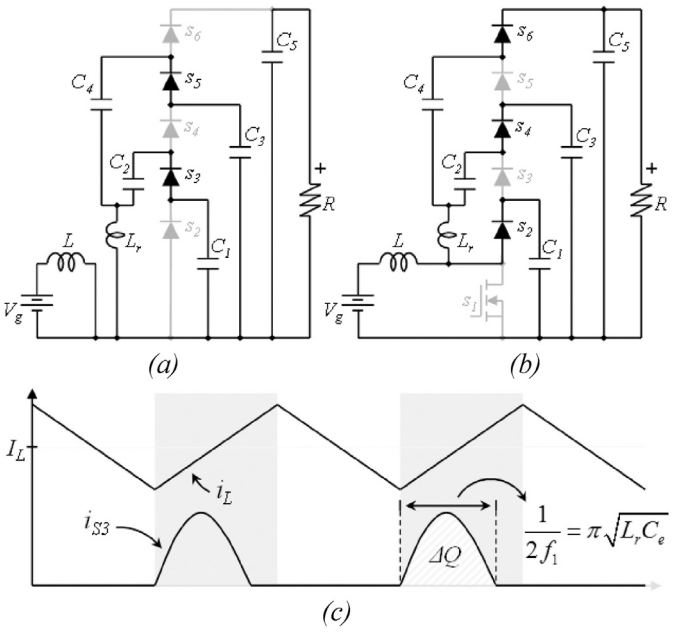

Fig. 6. Equivalent switching states and current waveforms in the energy storage inductor and the resonant part.

Table 1
Experimental components.

Component	Digikey number and maximum ratings
Mosfet s_1	IPP110N20NA, 200 V, 88 A,On-resistance 10.7 mΩ
Ultra-Fast Diodes s_2 to s_6	BTW29E-200, 200 V, 8 A,Forward voltage 1.5 V
Film Capacitors C_1 to C_5	B32674D4335 K, 3.3 μF, 450 V, ESR 5.2 mΩ
Inductor L_r	FP1006R1-R10-R, 100 nH, 53 A, ESR 0.27 mΩ
Inductor L	Toroid type, 40 μH, 16 A, ESR 40 mΩ

output voltage range and the conduction losses. This decision has to be taken according to the desired output voltage during the design process.

4. Experimental results

An experimental prototype was built to test the proposed principle. The schematic is that in Fig. 2(a), where the input voltage is V_g = 15 V and the switching frequency 200 kHz. Table 1 summarizes the experimental components parameters.

Fig. 7 exhibits important waveforms in both continuous conduction mode CCM and discontinuous conduction mode DCM. The gate voltage is 10 V with a duty cycle of 0.5. Waveforms shown in this section were recorded with a load of 200 Ω, except Fig. 7(b) that is the discontinuous mode waveforms, which resistance is 2.4 kΩ.

Fig. 7(a) indicates the CCM signals, where the average inductor current is equal to 2.75 A, with a ripple of 0.9 A, which is consistent with Eq. (7) since:

$$L = \frac{V_g \times D \times T_S}{\Delta i_L} = 40\mu = \frac{15 \times 0.5 \times 5\mu}{0.9} \tag{16}$$

Likewise, the voltage in C_1 (V_1) is consistent with Eq. (2) since:

$$V_1 = \frac{1}{1-D} V_g = \frac{1}{1-0.5} 15 = 30V \tag{17}$$

The charge interchange is given in Coulombs. Fig. 8(a) shows the voltage ripple of v_1, across capacitor C_1. It is the same voltage shown in Fig. 7 but with AC coupling and a zoom-in the vertical scale (200 mV-per-div). Fig. 8(a) also presents the current through diode s_2, and Fig. 8(b) shows the voltage ripple in v_1 along with the current in diode s_3. Basically the capacitor C_1 is charged by the current in Fig. 8(a) when the switch is *off*, and discharged by the current in Fig. 8(b) when the switch is *on*, Fig. 2 (both currents have the same average value).

The charge interchanged is calculated as Eq. (3) with the load current (in this case measured as 0.44 A) and the switching period, in this case 5 μS (measured 4.96 μS). Then, the charge interchange becomes,

$$\Delta Q = I_{out} \times T_S = 0.44 \times 5\mu = 2.2\mu C \tag{18}$$

The voltage ripple across C_1 can be calculated from Eq. (13) as:

$$\Delta v_1 = \frac{1}{C_1} \times \Delta Q = \frac{1}{3.3\mu} \times 2.2\mu = 0.66V \tag{19}$$

The voltage ripple is given in volts, the calculation may be approximated due to the components' tolerance. As shown in Fig. 8, results are consistent with those in Fig. 2.

Similarly to Fig. 8(a) and (b), Fig. 8(c) and (d) indicates the voltage ripple of v_2, and the current through diodes s_3 and s_4, respectively. Basically, the capacitor C_2 is charged by the current in Fig. 8(c) and discharged by the current in Fig. 8(d).

Since the capacitance is the same for all capacitors (3.3 μF) and the charge interchanged is also the same as described in equations (12) and (15), the voltage ripple in all capacitors has the same value.

The same behavior is observed in capacitors C_3 and C_4. Fig. 9 shows the voltage ripple in C_5 along with the current in diode s_6, which voltage ripple is calculated from Eq. (11),

$$\Delta v_5 = \frac{DT_S}{C_5} \times \frac{V_5}{R} = \frac{0.5(5\mu)}{3.3\mu} \times 0.44 = 0.33V \tag{20}$$

The efficiency is measured from the experimental prototype as shown in Fig. 10, where also the efficiency of the non-resonant multilevel boost converter is plotted as reported in [2]. The efficiency is larger, specially on the light load condition.

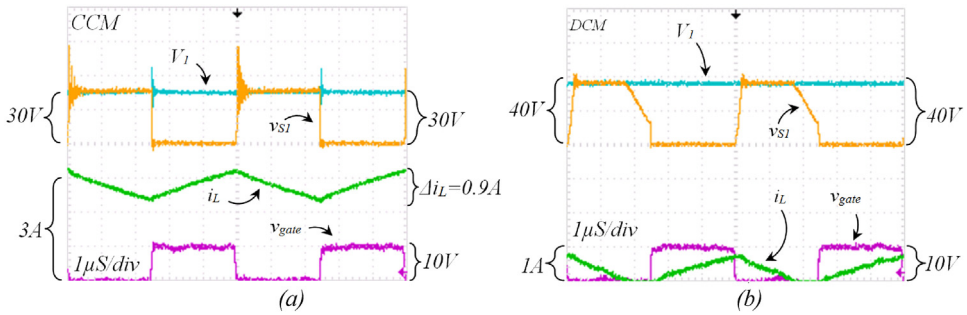

Fig. 7. Important waveforms in (a) continuous conduction mode CCM and (b) discontinuous conduction mode DCM.

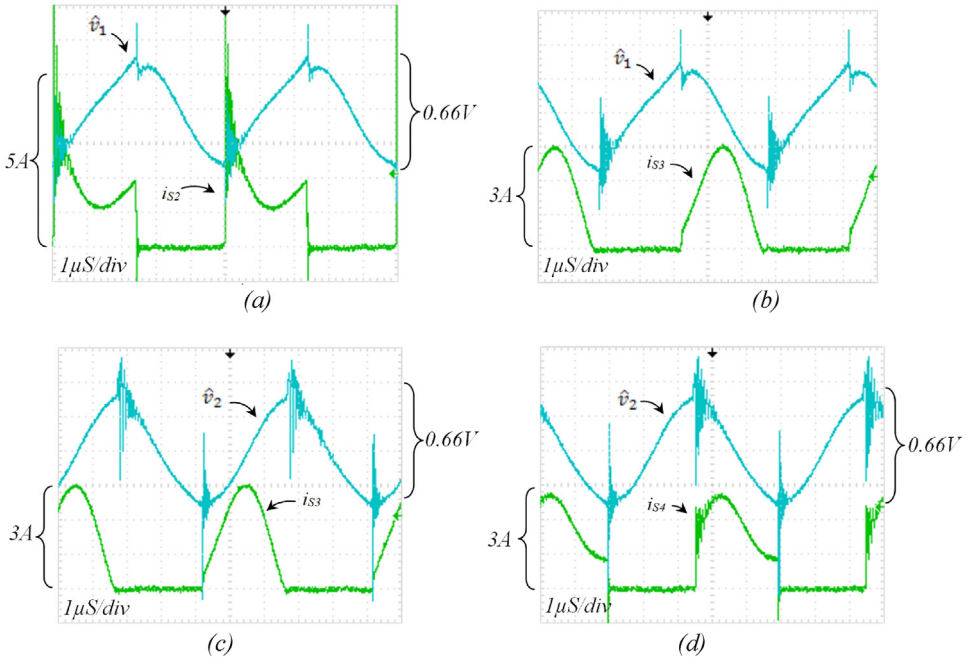

Fig. 8. Voltage ripple (only ac component) in capacitors C_1 and C_2 at 200 mV per division and current across diodes S_2, S_3 and S_4.

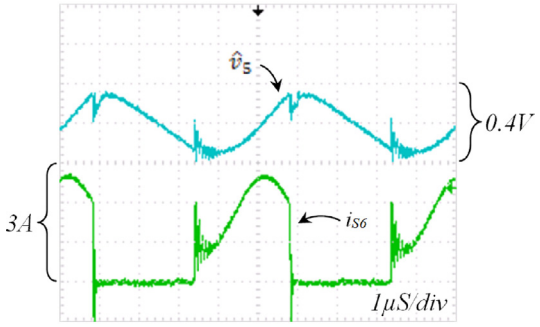

Fig. 9. Voltage ripple (only ac component) in capacitor C_5 at 200 mV per division and current across diodes S_6.

4.1. Experimental results

The proposed topology is a hybrid converter, where a conventional circuit (boost converter) is combined with a resonant switched capacitor voltage multiplier. There are pure resonant SC circuits in the state of the art [8–11]. They usually require a relatively large number of transistors while the proposed topology requires only one. They are not able to regulate the output voltage. On the other hand, one drawback of the proposition is an energy storage inductor requirement, when the output voltage is regulated, similarly to other hybrid configurations [23].

The main advantages of the proposed converter respect to the state of the art topologies are summarized in the following.

(i) The current among all capacitors (through diodes) in the voltage multiplier is resonant-type with only one resonant inductor.
(ii) The resultant resonant inductor is quite small compared to the energy storage inductor.
(iii) Regulation of the output voltage.

Possible applications for the proposed device include X-ray systems, automotive, ion pumps, uninterruptible power supplies UPS, telecommunication and renewable energy generation. For example, in PV panels and fuel cells, a high voltage-gain converter with continuous input current is required. The resonant multilevel boost converter is ideal for that purpose along with a wide range of emerging applications, where switched capacitor converters are used and resonant topologies may be explored [2–4,7,14,15,18,20–28].

Fig. 3 demonstrates that the proposed principle may be applied on different topologies, attaining the expected results.

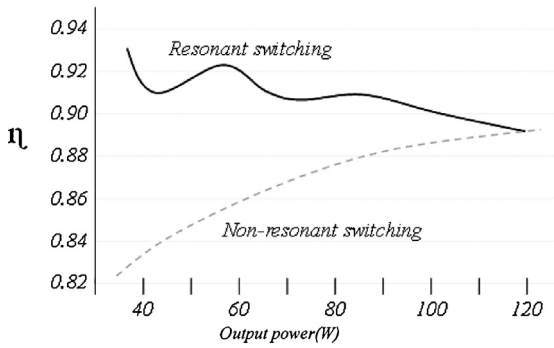

Fig. 10. Efficiency measured on the experimental prototype vs a non-resonant version [2].

5. Conclusions

This paper proposes an improved version of the multilevel boost converter, where resonant switching is performed with only one resonant inductor. This principle can be extended to other hybrid converters that use voltage multipliers. The proposed converter achieves a high voltage gain without the use of extreme duty cycles or transformers, with the property that every switching device blocks the same voltage. The input current is naturally continuous and the converter includes only one inductor for energy storage.

As an additional contribution, a design procedure was developed to select a capacitor in a case when the current-waveform is unknown, which can be applied to other switched capacitors

converters. Experimental results are provided to demonstrate the feasibility of the proposition.

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References

[1] G. Rong, L. Zhigang, A.Q. Huang, A family of multimodes charge pump based DC-DC Converter with high efficiency over wide input and output range, IEEE Trans. Power Electron. 27 (2012) 4788–4798.
[2] J.C. Rosas-Caro, J.M. Ramirez, F.Z. Peng, A. Valderrabano, A DC-DC multilevel boost converter, IET Power Electron. 3 (2010) 129–137.
[3] F.L. Tofoli, D. de Souza Oliveira, B. Torrico, R.P. x, Y.J.A. Alcazar, Novel nonisolated high-voltage gain DC-DC converters based on 3SSC and VMC, IEEE Trans. Power Electron. 27 (2012) 3897–3907.
[4] B. Axelrod, Y. Berkovich, A. Shenkman, G. Golan, Diode-capacitor voltage multipliers combined with boost-converters: topologies and characteristics, IET Power Electron. 5 (2012) 873–884.
[5] C. Shih-Ming, L. Tsorng-Juu, Y. Lung-Sheng, C. Jiann-Fuh, A boost converter with capacitor multiplier and coupled inductor for AC module applications, IEEE Trans. Ind. Electron. 60 (2013) 1503–1511.
[6] H. Yi-Ping, C. Jiann-Fuh, L. Tsorng-Juu, Y. Lung-Sheng, Novel high step-up DC-DC converter with coupled-inductor and switched-capacitor techniques, IEEE Trans. Ind. Electron. 59 (2012) 998–1007.
[7] S. Ben-Yaakov, Behavioral average modeling and equivalent circuit simulation of switched capacitors converters, IEEE Trans. Power Electron. 27 (2012) 632–636.
[8] C. Dong, P. Fang Zheng, Zero-current-switching multilevel modular switched-capacitor dc-dc converter, Proc. 2009 IEEE Energ. Conversion Congress Exposition ECCE (2009) 3516-3522.
[9] Z. Ke, M.J. Scott, W. Jin, A switched-capacitor voltage tripler with automatic interleaving capability, IEEE Trans. Power Electron. 27 (2012) 2857–2868.
[10] C. Dong, P. Fang Zheng, Multiphase multilevel modular DC-DC converter for high-current high-gain TEG application, IEEE Trans. Ind. Appl. 47 (2011) 1400–1408.
[11] Z. Ke, M.J. Scott, W. Jin, Switched-capacitor-cell-based voltage multipliers and DC-AC inverters, IEEE Trans. Ind. Appl. 48 (2012) 1598–1609.
[12] P. Sungsik, C. Sewan, Soft-switched CCM boost converters with high voltage gain for high-power applications, IEEE Trans. Power Electron. 25 (2010) 1211–1217.
[13] P. Sungsik, P. Yohan, C. Sewan, C. Woojin, L. Kyo-Beum, Soft-switched interleaved boost converters for high step-up and high-power applications, IEEE Trans. Power Electron. 26 (2011) 2906–2914.
[14] F.H. Dupont, C. Rech, R. Gules, J.R. Pinheiro, Reduced-order model and control approach for the boost converter with a voltage multiplier cell, IEEE Trans. Power Electron. 28 (2013) 3395–3404.
[15] M. Uno, K. Tanaka, Single-switch multioutput charger using voltage multiplier for series-connected lithium-ion battery/supercapacitor equalization, IEEE Trans. Ind. Electron. 60 (2013) 3227–3239.
[16] M. Prudente, L.L. Pfitscher, G. Emmendoerfer, E.F. Romaneli, R. Gules, Voltage multiplier cells applied to non-isolated DC-DC converters, IEEE Trans. Power Electron. 23 (2008) 871–887.
[17] Y.J.A. Alcazar, D. de Souza Oliveira, F.L. Tofoli, R.P. Torrico-Bascope, DC-DC non-isolated boost converter based on the three-state switching cell and voltage multiplier cells, IEEE Trans. Ind. Electron. 60 (2013) 4438–4449.
[18] Y. Chung-Ming, C. Ming-Hui, C. Tsun-An, K. Chun-Cho, J. Kuo-Kuang, Cascade cockcroft-walton voltage multiplier applied to transformerless high step-Up DC-DC converter, IEEE Trans. Ind. Electron. 60 (2013) 523–537.
[19] S. Busquets-Monge, x. Nicola, J. s-Apruzzese, An m-level active-clamped converter topology - operating principle, in: Proc. 2010 IEEE International Symposium on Industrial Electronics ISIE, 2010, pp. 3211–3217.
[20] M. Evzelman, S. Ben-Yaakov, Modeling and analysis of hybrid converters, in: Proc. 2012 IEEE Energy Conversion Congress and Exposition ECCE, 2012, pp. 1592–1598.
[21] J.C. Rosas-Caro, F. Mancilla-David, J.C. Mayo-Maldonado, J.M. Gonzalez-Lopez, H.L. Torres-Espinosa, J.E. Valdez-Resendiz, A transformer-less high-gain boost converter with input current ripple cancelation at a selectable duty cycle, IEEE Trans. Ind. Electron. 60 (2013) 4492–4499.
[22] J. Wittmann, J. Neidhardt, B. Wicht, EMC optimized design of linear regulators including a charge pump, IEEE Trans. Power Electron. 28 (2013) 4594–4602.
[23] Q. Wei, C. Honnyong, P. Fang-Zheng, L.M. Tolbert, 55-kW variable 3X DC-DC converter for plug-in hybrid electric vehicles, IEEE Trans. Power Electron. 27 (2012) 1668–1678.
[24] L. Ding, L. Poh Chiang, Z. Miao, G. Feng, F. Blaabjerg, Generalized multi-cell switched-inductor and switched-capacitor Z-source inverters, IEEE Trans. Power Electron. 28 (2013) 837–848.
[25] C. Chun-Kit, T. Siew-Chong, C.K. Tse, A. Ioinovici, On energy efficiency of switched-capacitor converters, IEEE Trans. Power Electron. 28 (2013) 862–876.
[26] Z. Jing, Y. Han, H. Xiangning, T. Cheng, C. Jun, R. Zhao, Multilevel circuit topologies based on the switched-capacitor converter and diode-clamped converter, IEEE Trans. Power Electron. 26 (2011) 2127–2136.
[27] Y. Ye, K.W.E. Cheng, Multi-port voltage-subtracting circuit based on resonant switched-capacitor, IET Power Electron. 5 (2012) 693–701.
[28] R.L. Andersen, T.B. Lazzarin, I. Barbi, A 1-kW step-up/step-down switched-capacitor AC-AC converter, IEEE Trans. Power Electron. 28 (2013) 3329–3340.
[29] R. Erickson, D. Maksimovic, Fundamentals of Power Electronics, Kluwer Academic Publishers, Norwell, MA, 2001.