Step-up DC–DC converter by coupled inductor and voltage-lift technique

S.-K. Changchien  T.-J. Liang  J.-F. Chen  L.-S. Yang

Abstract: A DC–DC converter with high step-up voltage gain is presented. The proposed converter uses the coupled inductor and the voltage-lift technique to achieve high step-up voltage gain. Additionally, the voltage on the active switch is clamped, and the energy stored in the leakage inductor is recycled in the proposed converter. Therefore the voltage stress on the active switch is reduced, and the conversion efficiency is improved. Finally, a laboratory prototype circuit with input voltage 12 V, output voltage 100 V and output power 35 W is implemented to demonstrate the performance of the proposed converter.

1 Introduction

High step-up DC–DC converters are widely used in many applications, such as in high-intensity discharge (HID) lamp ballasts for automobile headlamps, DC back-up energy systems for uninterruptible power supplies, front-stages of clean-energy sources and the drive systems of electric vehicles. Theoretically, the conventional boost converter can be used for high step-up voltage conversion with a large duty ratio. However, the conversion efficiency and step-up voltage gain of the boost converter are limited under a large duty ratio condition owing to the loss of power switches and rectifier diodes, as well as the equivalent series resistance of inductors and capacitors [1–3]. A very large duty ratio results in serious reverse-recovery problems and increases the rating of the output diode leading to very low efficiency. Additionally, a power converter operating at a duty ratio of greater than 50% requires a slope compensation in current-mode pulse width modulation (PWM) to overcome the instabilities with load disturbances. Therefore a step-up converter with a reasonable duty ratio to achieve high efficiency and high voltage gain performance is very important for high voltage gain applications.

Flyback and forward converters generally achieve high step-up voltage gains by adjusting the winding ratio of the transformer. However, the active switch of this converter produces high voltage spike and poor efficiency because of the leakage inductance. To reduce the voltage spike, the resistor–capacitor–diode (RCD) snubber is adopted to limit the voltage stress on the active switch. However, this approach reduces the efficiency [4]. Hence, non-dissipative snubbers have been applied to recycle the leakage inductance energy and to suppress the voltage spike on the active switch [5, 6]. Since the energy regeneration snubber circuit requires additional components, it has an increased cost.

Many boost converters have been presented to improve the conversion efficiency and raise the step-up voltage gain [7–22]. Various high step-up converters with low current ripple using the coupled inductor have been developed [7–10]. However, leakage inductance issues relating to voltage spike and efficiency remain significant. Liang et al. proposed a very simple topology for a high efficiency DC–DC converter with a high step-up voltage gain. An integrated boost-flyback converter based on a coupled inductor has been presented. The energy stored in the leakage inductance is recycled into the output during the switch-off period, increasing the efficiency and limiting the voltage spike. Several counterpart converters have been proposed based on this converter integration and output stacking concept [13–16]. Dunrongkittigule et al. [13] presented a high step-up DC–DC converter with integrated coupled inductor and common-mode electromagnetic interference reduction filter. Park et al. [14] developed a sepic-flyback converter with a coupled inductor and output voltage stacking. Baeck et al. [15] introduced a high step-up gain converter that uses coupled inductor and...
voltage-double technique on output stacking to achieve high voltage gain. Zhao and Lee [16] proposed a high step-up gain boost converter that utilises multiple coupled inductors for output voltage stacking. Moreover, a simple and effective converter has been presented for high step-up voltage gain. Kolar et al. [17] presented a switching converter, which recycles the leakage inductor energy stored to increase the conversion efficiency and suppress the switch voltage stress. Also, the converter alleviates the problem of the reverse-recovery time on the output diode. However, since most of the energy is stored in the coupled inductor, a large magnetic core is required for the demand of high output power application. Luo and Ye [18, 19] introduced the voltage-lift technique for high step-up voltage conversion. Because the switch must endure large current during switch-on period, voltage-lift technique is suitable for low-output-power applications. Wai et al. [20–22] investigated high-gain step-up converters with coupled inductor for applying in fuel-cell electrical conversion. The step-up converter with coupled inductor and a sub-converter are presented for high step-up converter [20]. The step-up converter with low voltage stress on output diode and power switch uses an integrated coupled inductor and the voltage-lift technique for high step-up voltage conversion [21, 22]. Besides, the leakage inductance of the coupled inductor in [21] can be used to limit the current spike in these topologies. However, a three-winding coupled inductor is required in [22]. Since high step-up voltage gain, high efficiency and low voltage rating require an appropriate power switch, these converters are suitable for high-output-power applications. However, the requirement for a coupled inductor with high coupling coefficient increases the manufacturing difficulty and cost increment and solves the circulating current problem.

This paper presents a novel high-efficiency DC–DC converter, which uses the coupling inductor and voltage-lift technique to achieve a high voltage gain. The proposed converter has the following features:

1. High step-up voltage gain.
2. The duty ratio can be designed to less than 0.5 by adjusting the turns ratio of the coupled inductor. Thus, the converter can be operated under current-mode PWM.
3. The energy stored in the leakage inductance of the transformer is recycled, thus, increasing the efficiency.
4. The voltage is clamped on the active switch, enabling the power switch to be selected with a low voltage rating and low conducting resistance $r_{ds(on)}$.
5. The converter uses low-rating switch and diodes to minimise the cost.

The rest of this paper is organised as follows. Section 2 presents the operating principle of the proposed converter in detail. Section 3 then describes the circuit design and experimental results of the proposed converter. Conclusions are finally drawn in Section 4.

## 2 Operation principle of the proposed converter

Fig. 1 shows the proposed converter, which is a boost converter with voltage-lift technique and a coupled inductor. The equivalent model of the coupled inductor includes the magnetising inductor $L_m$, leakage inductors $L_{d1}$ and $L_{d2}$ and an ideal transformer. This converter consists of a DC input voltage $V_{in}$, one power switch, one coupled inductor, three diodes and three capacitors. The boost converter is adopted to generate a stable voltage $V_{C1}$ and to supply the energy for the load. Additionally, the diode $D_1$ is tuned on when switch $S$ is in turned-off period, the voltage across switch $S$ is clamped at a low voltage level, and the energy stored in the leakage inductance is recycled into $C_1$. Since switch $S$ has a low voltage rating and low conducting resistance $r_{ds(on)}$, the proposed converter has high efficiency. The voltage-lift technique is applied to generate a constant voltage $V_{C2}$ and provide the energy to output. Because the voltage across $C_2$ is constant, the voltage gain can be enhanced. Furthermore, the turn ratio of the coupled inductor is adjusted to achieve a high step-up voltage gain.

To simplify the circuit analysis, the following conditions are assumed:

1. Capacitors $C_1$, $C_2$ and $C_o$ are large enough that the $V_{C1}$, $V_{C2}$, and $V_o$ are constant values in one switching period.
2. All semiconductor components are ideal.
3. Most of the energy is stored in the magnetising inductance $L_m$, which is larger than the leakage inductances $L_{d1}$ and $L_{d2}$.
4. Turns ratio of the coupled inductor $n = N_2/N_1$.

The proposed converter operating in continuous conduction mode (CCM) and discontinuous conduction mode (DCM) are analysed as follows.
2.1 Continuous conduction mode

Based on the above assumption, the operating principle of CCM is divided into six modes during each switching period. Fig. 2 illustrates some typical key waveforms under CCM operation in one switching period. The operating modes are described as follows:

Mode 1 \([t_0-t_1]\): At \(t = t_0\), \(S\) is turned on, \(D_2\) and \(D_3\) are turned on and \(D_1\) is turned off. Fig. 3a shows the equivalent circuit of the proposed converter in this mode. Because the energy of \(C_S\) is discharged quickly, \(V_{DS} = 0\) in this mode. The voltage across \(C_2\) is charged to \(V_{in} + V_{C1}\). The energy stored in leakage inductor \(L_{k2}\) continues to release to the output. Since magnetising inductor \(L_m\) and leakage inductor \(L_{k1}\) are charged from \(V_{in}\), \(i_{Lm}\) and \(i_{Lk1}\) are increased linearly. At \(t = t_1\), \(i_{D3} = i_{Lk2} = 0\), thus ending this mode.

Mode 2 \([t_1-t_2]\): At \(t = t_1\), \(S\) is turned on, \(D_1\) and \(D_3\) are turned off and \(D_2\) is turned on. Fig. 3b presents the equivalent circuit of this mode. In this time interval, the inductors \(L_{k1}\) and \(L_m\) are charged from DC input voltage \(V_{in}\). The currents, \(i_{Lk1}\) and \(i_{Lm}\), are equal and are increased linearly with a slope of \(V_{in}/L_m \ (L_m \gg L_{k1})\). The voltage across \(C_2\) is charged to \(V_{in} + V_{C1}\). The load energy is supplied by capacitor \(C_o\). This mode is ended at \(t = t_2\) when \(i_{D2} = 0\).

Mode 3 \([t_2-t_3]\): At \(t = t_2\), \(S\) is turned on, \(D_1\), \(D_2\) and \(D_3\) are turned off. Fig. 3c shows the equivalent circuit of this mode.
The operating principle of this mode is the same as mode 2 except $i_{332} = 0$. This mode is ended at $t = t_3$ when switch $S$ is turned off.

Mode 4 [$t_3$–$t_4$]: At $t = t_3$, $S$ is turned off, $D_1$, $D_2$ and $D_3$ are also turned off. Fig. 3d illustrates the equivalent circuit of the proposed converter in this mode. In this time interval, the magnetising current charges the parasitic capacitor $C_s$ of switch $S$, and so the voltage across $S$ is increased linearly until time instant $t_4$ when $V_{DS} = V_{in} + V_{C1}$. The voltage across $C_s$ is maintained at $V_{in} + V_{C1}$. The load energy is supplied by capacitor $C_o$.

Mode 5 [$t_4$–$t_5$]: At $t = t_4$, $V_{DS} = V_{in} + V_{C1}$. In this time interval, $S$ is still turned off, $D_1$ and $D_3$ are turned on and $D_2$ is turned off. Fig. 3e shows the equivalent circuit of the proposed converter in this mode. The energy stored in $L_m$ and $L_{41}$ is released to capacitor $C_1$ and $C_0$ when $D_1$ and $D_3$ start to conduct in this mode. Thus, $i_{31}$ is decreased linearly and $i_{33}$ is increased linearly. The leakage inductor energy can thus be recycled, and the voltage stress of the switch can be limited. This mode is ended at $t = t_5$ when $\mathcal{L}_{41}a = i_{33}$.

Mode 6 [$t_5$–$t_6$]: At this mode, $V_{DS} = V_{in} + V_{C1}$. $S$ is still turned off, $D_1$ and $D_3$ are turned on and $D_2$ is turned off. The equivalent circuit of the proposed converter of this mode is the same as Fig. 3c. The circuit operating principle of this mode is the same as mode 5. But, in this time interval, $i_{33}$ is decreased linearly. This mode is ended at $t = t_5$ when switch $S$ is turned on.

To analyse the CCM steady-state characteristics of the proposed converter, the leakage inductances are neglected. The coupled inductance is modelled as a magnetising inductor $L_m$. Since the time durations of modes 1 and 4 are very short, the following steady-state analysis considers modes 2, 3, 5 and 6. During the switch-on period, $V_{Lm}$ and $V_{N2}$ are written as

$$v_{Lm} = V_{in}$$
$$v_{N2} = nV_{Lm} = nV_{in}$$

During the switch-off period, $V_{Lm}$ and $V_{N2}$ can be expressed as

$$v_{Lm} = -V_{C1}$$
$$v_{N2} = nV_{Lm} = nV_{C1} = V_{C2} + V_{in} - V_o = 2(V_{C1} + V_{in}) - V_o$$

where

$$V_{C2} = V_{C1} + V_{in}$$

By using the voltage-second balance principle on $N_1$ and $N_2$ of the coupled inductor, the following equations are given

$$\int_0^{DT} (V_{in})dt + \int_0^T (-V_{C1})dt = 0$$
$$\int_0^{DT} nV_{in}dt + \int_0^T [2(V_{C1} + V_{in}) - V_o]dt = 0$$

Equation (9) indicates that the proposed converter accomplishes a high voltage gain by utilising the voltage-lift technique and increasing the turns ratio of the coupled inductor. Fig. 4 plots the ideal voltage gain against the duty ratio, under various turns ratios of the coupled inductor. These family curves can be used to determine the duty ratio of the converter and the turns ratio of the coupled inductor. Fig. 5 illustrates the voltage gain against duty ratio of the proposed converter and the other coupled inductor-based converters under a fixed turns ratio of coupled inductor, $n = 1.25$. The proposed converter achieved the highest voltage gain among these counterparts. However, the components of the proposed converter are more than these counterparts.

![Figure 4 Voltage gain against duty ratio under various turns ratio of the coupled inductor](image1)

![Figure 5 Voltage gain against duty ratio of several counterparts](image2)
According to (8) and (9), the voltage stresses on the switch and the diodes are as follows

\[ v_{DS} = V_{C1} + V_{in} = \frac{1}{1-D} V_{in} \]  
(10)

\[ v_{D1} = V_{C2} = V_{C1} + V_{in} = \frac{1}{1-D} V_{in} \]  
(11)

\[ v_{D2} = V_{C2} = V_{C1} + V_{in} = \frac{1}{1-D} V_{in} \]  
(12)

\[ v_{D3} = nV_{in} + V_o - V_{C2} = \frac{n+1}{1-D} V_{in} \]  
(13)

From (9) and (10), the voltage stress of the main switch is clamped at a low voltage, and less than output voltage.

2.2 Discontinuous conduction mode

To simplify the DCM analysis, the leakage inductors of the coupled inductor are neglected. The coupled inductance is modelled as magnetism inductor \( L_m \). The operating modes with DCM operation are divided into four modes during each switching period. Fig. 6 shows the equivalent circuit of the mode 4 and the key waveforms under DCM operation in one switching period. \( i_2 \) is denoted as in Fig. 6b. The operating modes are described as follows:

**Mode 1 \([t_0-t_1]\):** At \( t = t_0 \), \( S \) is turned on, \( D_1 \) and \( D_3 \) are turned off and \( D_2 \) is turned on. The equivalent circuit of the proposed converter in this mode is the same as Fig. 3b. In this interval, the inductor \( L_m \) is charged from DC input voltage \( V_{in} \). The current \( i_{Lm} \) is increased linearly. The voltage across \( C_2 \) is charged to \( V_{in} + V_{C1} \). The load energy is supplied by capacitor \( C_o \). This mode is ended at \( t = t_1 \) when \( i_{D2} = 0 \).

**Mode 2 \([t_1-t_2]\):** At \( t = t_1 \), \( S \) is turned on and \( D_1, D_2 \) and \( D_3 \) are turned off. The equivalent circuit of the proposed converter in this mode is the same as Fig. 3c. The operating principle of this mode is the same as mode 1 except \( i_{D2} = 0 \). This mode is ended at \( t = t_2 \) when switch \( S \) is turned off. Thus, the equations are derived as

\[ v_{Lm} = V_{in} \]  
(14)

\[ v_{N2} = nV_{Lm} = nV_{in} \]  
(15)

\[ I_{Lmp} = \frac{V_{in}}{L_m} DT \]  
(16)

where \( I_{Lmp} \) denotes the peak value of the magnetising current.

**Mode 3 \([t_2-t_3]\):** At \( t = t_2 \), \( S \) is turned off, \( D_1 \) and \( D_3 \) are turned on and \( D_2 \) is turned off. The equivalent circuit of the proposed converter in this mode is the same as Fig. 3e. In this interval, the energy stored in \( L_m \) is released to \( C_1 \) and \( C_o \), thus, \( i_{D2} \) and \( i_{D3} \) are decreased linearly. Since the average current of \( C_2 \) should be zero during one switching period, thus \( i_{D1} \) is equal to \( i_{D3} \). The equations are given as

\[ v_{Lm} = -V_{C1} = \frac{1}{n} [2(V_{C1} + V_{in}) - V_o] \]  
(17)

\[ v_{N2} = 2(V_{C1} + V_{in}) - V_o \]  
(18)

\[ I_{Lmp} = \frac{V_{C1}}{L_m} D_L T \]  
(19)

\[ I_{D3p} = \frac{I_{Lmp}}{n+2} \]  
(20)

where \( I_{D3p} \) denotes the peak value of \( i_{D3} \). This mode ends at \( t = t_3 \), when the magnetising current \( i_{Lm} \) reaches zero.
Mode 4 $[t_3-t_4]$ : At $t = t_3$, $i_{Lm}$ is equal to zero. $S$ is still turned off and $D_1$, $D_2$ and $D_3$ are also turned off. Fig. 6 shows the equivalent circuit of the proposed converter in this mode. The energy stored in $C_o$ is released to the load during this time interval.

By using the voltage-second balance principle on $N_1$ and $N_2$ of the coupled inductor, the following equations are derived as

$$
\int_0^{DT} V_{in} \, dt + \int_0^{(D+D_L)T} (-V_{C1}) \, dt = 0
$$

(21)

$$
\int_0^{DT} nV_{in} \, dt + \int_0^{(D+D_L)T} [2(V_{C1} + V_{in}) - V_o] \, dt = 0
$$

(22)

From (21) and (22), $V_{C1}$ and $V_o$ are given by

$$
V_{C1} = \frac{D}{D_L} V_{in}
$$

(23)

$$
V_o = \left[ \frac{(2+n)D}{D_L} + 2 \right] V_{in}
$$

(24)

Thus

$$
D_L = \frac{(2+n)DV_{in}}{V_o - 2V_{in}}
$$

(25)

From Fig. 6, the average value of $i_{co}$ is computed as

$$
I_{co} = \frac{(1/2)D_L T(I_{Lmp}/n + 2) - I_o T}{T} = \frac{1}{2} D_L \frac{I_{Lmp}}{n + 2} - I_o
$$

(26)

$I_{co} = 0$ under a steady-state. Thus, substituting (16), (25) and $I_{co} = 0$ into (26), the following equation is obtained as

$$
\frac{(n + 2)D^2 V_o^2 T}{2(V_o - 2V_{in}) n Lm} = \frac{V_o}{R}
$$

(27)

The normalised inductor time constant is then defined as

$$
\tau_L = \frac{Lm f}{R}
$$

(28)

where $f$ is the switching frequency.

Substituting (28) into (27), the DCM voltage gain is given by

$$
\frac{V_o}{V_{in}} = 1 + \sqrt{1 + \frac{n + 2}{2n} \frac{D^2}{\tau_L}}
$$

(29)

If the proposed converter is operated in the boundary conduction mode (BCM), then the voltage gain of CCM operation is equal to the voltage gain of DCM operation. From (9) and (29), the boundary normalised inductor time constant $\tau_{LB}$ can be derived as

$$
\tau_{LB} = \frac{D(1-D)^3}{2(n+2)(2+nD)}
$$

(30)

Fig. 7 plots the curves of $\tau_{LB}$ against the duty ratio when $n = 6$. The proposed converter is operated in CCM if $\tau_L > \tau_{LB}$, and in DCM otherwise.

3 Design and experiment of proposed converter

A prototype circuit was implemented to demonstrate the performance of the proposed converter. The prototype converter had the following specifications:

- input DC voltage = 12 V;
- output DC voltage = 100 V;
- maximum output power = 35 W;
- boundary condition = 20 W;
- switching frequency = 50 kHz.

Based on the above circuit specifications, the circuit design consideration can be described as below:

1. The efficiency against duty ratio under $V_{in} = 12$ V, $V_o = 100$ V and $P_o = 35$ W is illustrated in Fig. 8 by using

![Figure 8](https://example.com/image8.png)
simulation software IsSpice. From Fig. 8, it can be seen that the better conversion efficiency of the proposed converter is at duty ratio $D = 0.61–0.71$ and turns ratio $n = 0.5–2.2$. Hence, $D$ and $n$ are selected as 0.65 and 1.25, respectively.

2. From (28) and (30), the boundary magnetising inductance of the coupled inductor can be expressed as

$$I_m = \frac{D(1 - D)^2 R}{2(n + 2)(2 + nD)}$$

(31)

Thus, the magnetising inductance is calculated approximately 44 $\mu$H.

3. The voltage stresses of power switch and diodes are determined according to (10)–(13).

4. The leakage inductance of winding $N_2$ and the junction capacitance of $D_3$ result in a ringing spike on $D_3$ in the transient state associated with switch $S$ from OFF to ON. Generally, a resistor–capacitor or RCD snubber can be utilised to suppress the ringing spike, if necessary. In this circuit design, an RCD snubber is added across $D_3$ to reduce this ringing spike.

The proposed converter had the following key components:

- power switch: IR, IRF3710, $R_{\text{ds(on)}} = 23$ mΩ;
- diodes $D_1$ and $D_2$: ST, STPS20L60CT, $V_F = 0.56$ V;
- diode $D_3$: ST, STTH8R06, $V_F = 1.4$ V;

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**Figure 9** Experimental results of the proposed converter under the full load, boundary mode and light load condition

- **a** and **b** Full load
- **c** and **d** Boundary mode
- **e** and **f** Light load
• coupled inductor: EI-30 core, PC-40, \( N_1 = 12T \), \( N_2 = 15T \), \( L_{\text{ms}} = 44 \mu\text{H} \), \( L_{\Delta} = 0.6 \mu\text{H} \);
• capacitor \( C_1 \): 100 \( \mu\text{F} / 50 \text{ V} \), aluminium capacitor;
• capacitor \( C_2 \): 12 \( \mu\text{F} / 50 \text{ V} \), ceramic capacitor;
• capacitor \( C_0 \): 360 \( \mu\text{F} \) (180 \( \mu\text{F} / 250 \text{ V} \times 2 \)), aluminium capacitor;
• RCD snubber: \( R = 5 \text{ k}\Omega \), \( C = 1000 \text{ pF} \), \( D = 1\text{N4947} \).

Fig. 9 shows the experimental measured waveforms at CCM, BCM and DCM, respectively, which were measured to verify the performance of the proposed converter under different output powers. These results indicate that the duty ratio must be raised to maintain a constant output voltage when the output power is increased. Figs. 9a and b show the experimental results of the proposed converter under the full load condition. The waveforms agree with the steady-state analysis, and the voltage stress of switch is effectively clamped by diode \( D_1 \) and capacitor \( C_1 \).

Fig. 10 shows the experimental conversion efficiency of the proposed converter at the two conditions \( (D, n) = (0.42, 6.67) \) and \( (0.65, 1.25) \). When \( D \) and \( n \) are equal to 0.42 and 6.67, respectively, the efficiency is 90.8% at full load and the maximum efficiency is 92.8% at \( P_o = 20 \text{ W} \). When \( D \) and \( n \) are 0.65 and 1.25, the efficiency is 93% at full load and the maximum efficiency is 93.8% at an output power of 25 W. Therefore the conversion efficiency under the condition \( (D, n) = (0.65, 1.25) \) is higher than under the condition \( (D, n) = (0.42, 6.67) \). These results verify that the approach by IsSpice simulation can assist to determine the duty ratio for achieving better efficiency performance.

Owing to the current spike on the switch \( S \) and diode \( D_2 \) during the switch-on period, the current spike suppressing circuit is required to alleviate this current spike. Fig. 11 shows the proposed converter with the current spike suppressing circuit. The additional inductor \( L_1 \) is utilised for limiting the raising rate of the current to reduce the conduction loss. In this circuit design, the additional inductor \( L_1 \) is selected as 5.8 \( \mu\text{H} \) for the proposed converter. Figs. 12a and b show the experimental current waveforms of the proposed converter and the proposed

![Figure 10](image1.png)
**Figure 10** Experimental conversion efficiency of the proposed converter at different output powers

![Figure 11](image2.png)
**Figure 11** Proposed converter with current spike suppressing circuit

![Figure 12](image3.png)
**Figure 12** Experimental results of the proposed converter and the proposed converter with the current spike suppressing circuit

\( a \) Measured waveforms of \( i_{DS} \) and \( i_{D2} \) without \( L_1 \)
\( b \) Measured waveforms of \( i_{DS} \) and \( i_{D2} \) with \( L_1 (L_1 = 5.8 \mu\text{H}) \)
\( c \) Conversion efficiency of the proposed converter at different output powers
converter with the current spike suppressing circuit, respectively. From the figures, the current spike of diode $D_2$ can be reduced from 4.4 A to 1 A. The current spike of switch $S$ is also diminished from 7 A to 6 A.

Fig. 12c shows the experimental conversion efficiency of the proposed converter and the proposed converter with the current spike suppressing circuit at different output powers. The maximum efficiency of the proposed converter with the current spike suppressing circuit is 93.9% at an output power of 25 W. The full-load efficiency of the proposed converter with the current spike suppressing circuit is approximately 93.7%. These results confirm that the efficiency of the proposed converter with current spike suppressing circuit has high efficiency conversion performance.

4 Conclusions

This paper presents a step-up DC–DC converter that uses voltage-lift technique, adjusts the turns ratio of the coupled inductor and achieve high step-up voltage gain. The proposed converter is highly efficient because it recycles the energy stored in the leakage inductor of the coupled inductor. Moreover, the voltage across the switch is clamped at the lower voltage level, enabling the converter to use the low rating switch to improve efficiency. This paper also describes the operating principle and the steady-state analysis in detail. Finally, a prototype converter is implemented to verify the performance of the proposed converter. In the circuit design, an IsSpice simulation approach is presented to determine the duty ratio and turns ratio for high efficiency of the proposed converter. The measured results verify that this approach can assist to determine the duty ratio to achieve better efficiency performance. Additionally, the measured waveforms agree with the steady-state analysis of the CCM and DCM operation, and the voltage stress of switch is effectively clamped. Also, a current spike suppressing circuit is proposed to alleviate the current raising rate for the proposed converter. The experimental results verify that the proposed current spike suppressing circuit can not only reduce the current spike effectively, but also improve the conversion efficiency for the proposed converter. Moreover, the proposed converter is appropriate for applications involving power conversion systems, such as HID lamps for automobile headlamps, small fuel-cell power conversion systems, etc. This approach is presented to determine the duty ratio and turns ratio for high efficiency of the proposed converter. The measured results verify that this approach can assist to determine the duty ratio to achieve better efficiency performance. Additionally, the measured waveforms agree with the steady-state analysis of the CCM and DCM operation, and the voltage stress of switch is effectively clamped. Also, a current spike suppressing circuit is proposed to alleviate the current raising rate for the proposed converter. The experimental results verify that the proposed current spike suppressing circuit can not only reduce the current spike effectively, but also improve the conversion efficiency for the proposed converter. Moreover, the proposed converter is appropriate for applications involving power conversion systems, such as HID lamps for automobile headlamps, small fuel-cell power conversion systems, and small solar-cell power conversion systems.

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