Field-Oriented Control and Direct Torque Control for Paralleled VSIs Fed PMSM Drives With Variable Switching Frequencies

Zheng Wang, *Senior Member, IEEE*, Jian Chen, Ming Cheng, *Fellow, IEEE*, and K. T. Chau, *Fellow, IEEE*

***Abstract*—In this paper, three control schemes with variable switching frequencies are proposed and analyzed for the paralleled voltage source inverters (VSIs) fed permanent magnet synchronous motor (PMSM) drive. The proposed schemes could be applied in the low-speed operation region of high-power drive system, where the frequency modulation index is high. First, the field-oriented control (FOC) with phase-shifted chaotic space vector modulation (SVM) under synchronous frame and the FOC with phase-shifted chaotic sinusoidal pulse width modulation under stationary frame is proposed for the paralleled VSIs fed PMSM drive. The proposed phase-shifted chaotic PWM schemes not only eliminate specific switching harmonics completely but also suppress all remaining switching harmonic peaks in the spectrum. The avoidance of inherent circulating current is also considered in designing these two schemes. Second, the direct torque control (DTC) for the paralleled VSIs fed PMSM drive is proposed with circulating current suppression. Besides inheriting the advantages of DTC, the output currents of paralleled VSIs are kept balanced. The working principles of these three methods are presented in detail. Experimental results on a laboratory prototype are given to verify the validity of the three proposed control schemes for the paralleled VSIs fed PMSM with variable switching frequencies.**

***Index Terms*—Chaotic PWM, direct torque control (DTC), field-oriented control (FOC), paralleled VSIs, permanent magnet synchronous motor (PMSM) drive.**

I. Introduction

THE paralleled inverters fed electric drives have the advantages of large current ratings, easy modular design, good current waveforms, and high fault-tolerant capability [1]. Therefore, they are used widely in high-power applications where two or more power converters are needed for the necessary power capacity such as the high-power compressor trains for liquefied natural gas, high-power gas/steam turbine, and high-speed elevator [2]–[4]. They are also used for wind power generation [5].

Manuscript received January 19, 2015; revised March 23, 2015; accepted April 25, 2015. Date of publication June 1, 2015; date of current version November 16, 2015. This work was supported in part by the National Key Basic Research Program of China (973 program) under Grant 2013CB035603, in part by the Aeronautical Science Foundation of China under Grant 20142869014, and in part by Jiangsu Province Qin Lan Project (1116000195). This paper was presented in part at the *IEEE International Power Electronics and Application Conference and Exposition*, Shanghai, China, November 5–8, 2014. Recommended for publication by Associate Editor J. O. Ojo.

Z. Wang, J. Chen, and M. Cheng are with the School of Electrical Engineering, Southeast University, Nanjing 210096, China (e-mail: zwang@eee.hku.hk; hnsorry@yeah.net; mcheng@seu.edu.cn).

K. T. Chau is with the Department of Electrical and Electronic Engineering, University of Hong Kong, Hong Kong (e-mail: ktchau@eee.hku.hk).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2015.2437893

For paralleled inverters fed electric drives, several inverters are paralleled at their ac output sides in such a way that the output current ratings are increased.

These paralleled inverters could share one common dc link. This arrangement not only saves the cost but also makes the regulation of dc-link voltage easier. However, the circulating current may occur due to the informality in switching instants and difference in parameters of paralleled inverters [6], [7].

Related modulation techniques for paralleled voltage source inverters (VSIs), the carrier-phase-shifted pulse width modulation (CPS-PWM) has been proposed to improve the harmonic performance of paralleled converters [8]. By applying the CPS-PWM technique to sinusoidal PWM (SPWM), the CPS-SPWM is obtained and the switching harmonics is reduced for paralleled inverters [9]. This phase-shift concept could also be applied to space vector modulation (SVM), and the sampling time staggered SVM (STS-SVM) is thus available [10]. For STS-SVM in paralleled inverters, the sampling instants of different inverters are interleaved so that the harmonics performance is improved. The phase-shifted selective harmonic elimination technique is also presented to eliminate the low-order harmonics in output voltages and currents of paralleled inverters by optimizing switching angles [11].

Most of previous work on control schemes of the paralleled VSIs fed drives is based on synchronous frame reference control. The three-phase currents are transformed into the d-axis and q-axis components under the synchronous frame. Then, the d-axis and q-axis currents are regulated with the standard PI controllers. In [5], the synchronous frame-based control is used on both line side and generator side of the paralleled VSIs fed permanent magnet synchronous generator (PMSG) wind power generation system. In [6], the double-sequence synchronous frame reference control is proposed for the three-phase-paralleled boost rectifiers to regulate the positive- and the negative-sequence components of phase currents. In [12], both continuous and discrete control methods are proposed for the paralleled three-phase boost rectifiers based on manifold control instead of stability analysis in vicinity of equilibrium. Thus, better dynamic performance is provided though slightly higher current harmonics are induced. The control of paralleled VSIs fed drives is also proposed under stationary frame, where the three-phase currents are transformed into α-axis and β-axis currents and a proportional control is used to regulate them [4].

The power sharing of the paralleled VSIs fed drives is usually implemented by using the average current reference for the paralleled VSIs. For example, the torque current reference is

shared among the paralleled VSIs on machine side [5] and the average current reference for active power is applied for paralleled VSIs on grid side [6]. Another method to implement the power sharing is to control the total output current of paralleled VSIs and regulate the difference in currents of different VSIs at the same time [4]. To suppress the circulating current among the paralleled VSIs, a kind of SVM has been proposed for interleaved operation of paralleled inverters by using opposite active vectors to synthesize zero vectors in such a way that the mechanism of producing the zero-sequence current by zero-vector overlap is eliminated [13]. In [7], the dwelling time of zero-voltage vectors in SVM are tuned dynamically to adjust zero-sequence output voltages of paralleled inverters. Thus, the zero-sequence current generated by each VSI could be controlled. In [6], a closed-loop zero-sequence current controller is used to generate a perturbation term in modulation waveforms for SPWM. Thus, the zero-sequence current can track the zero reference value. In [14], an interphase inductor is designed to suppress the circulating current resulted from interleaved PWM for paralleled inverters. A shared three-phase line inductor is integrated with the interphase inductor for smaller size.

However, to the best of authors' knowledge, all of the previous studies are for paralleled VSIs with fixed switching frequency. Differently, this paper will study the field-oriented control (FOC) and direct torque control (DTC) schemes for the paralleled VSIs fed permanent magnet synchronous motor (PMSM) drives with variable switching frequencies. It should be mentioned that the synchronous PWM is normally used for high-power drives with limited switching frequency [15]. However, the variable-speed drives also might operate at low-speed range, where the asynchronous PWM can still be used since the ratio of switching frequency to fundamental frequency is high in that region.

For FOC scheme of paralleled VSIs fed drives, this paper proposes the phase-shifted chaotic SVM strategy and the phase-shifted chaotic SPWM strategy under synchronous frame and under stationary frame, respectively. Besides the ability of eliminating specific switching harmonics, the proposed phase-shifted chaotic PWM strategies can reduce remaining peaky switching harmonics in the spectrum. The avoidance of circulating current will be considered with the phase-shifted PWM techniques. Essentially, the chaotic PWM is a kind of pseudorandom PWM technique. The random PWM are drawing more attentions and has been widely used in power converters and drive systems today. By randomizing the switching frequency and pulse position, the distinct switching peaks are destroyed in the spectrum [16], [17]. Thus, the electromagnetic interference and acoustic noise are reduced for isolated and nonisolated dc/dc converters [18], [19], voltage source rectifiers and inverters [20], and multilevel inverters [21]–[23]. The converters and drive systems with random PWM have been proposed for various applications, such as active power filters [24], electric vehicles [17], naval propulsion system [25], etc. Due to the random-like behavior and easy implementation, the chaotic PWM is often used to take place of random PWM to shape the harmonic spectrum [26]–[28]. Recently, the chaotic PWM has been proposed for security management of wireless charging for electric vehicles [29].

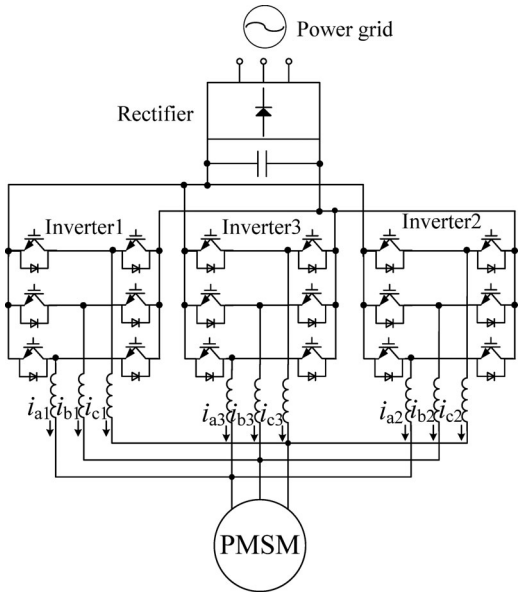


Fig. 1. Configuration of three inverters fed PMSM drive.

The DTC method is another widely used control scheme for electric drives with variable switching frequencies. The torque and stator flux are regulated directly by using a switching status table and independent of current controllers. The DTC has been studied in both academia and industry [30], [31]. But the discussion of electric drives with DTC is focused on a single converter thread. Differently, the traditional DTC is modified in this paper by adding a hysteresis output current controller for each VSI to track the average reference. Thus, not only the fast dynamic response of DTC is inherited but also the circulating currents are avoided. The contents of this paper are listed as follows: In Section II, the system configuration of the paralleled VSIs fed drive is introduced, and the dynamic modeling of the system is analyzed. The FOC with chaotic SVM under synchronous frame and the FOC with chaotic SPWM under stationary frame are proposed and analyzed for paralleled PMSM drive in Sections III and IV, respectively. Then, the DTC with hysteresis circulating current suppression is proposed and designed in Section V. In Section VI, the experimental verification is given for all the three proposed control schemes for paralleled VSIs fed drive. The comparison and discussion of the three methods are presented in Section VII. Finally, the conclusions are drawn in section VIII.

II. Configuration and Modeling

Fig. 1 shows the configuration of a three VSIs fed PMSM system, where the three inverters share a common dc link, and the ac output sides are paralleled directly through balancing impedances. To analyze the circulating currents in the system, the equivalent circuit in a three-phase stationary frame is plotted in Fig. 2 [4]. On the basis of Fig. 1, the PMSM can be equivalent to the three-phase inductive load with back EMF if the mutual inductances are ignored. The three-phase ac voltage sources are used to represent the three-phase VSIs, which are relative to their suppositional neutral points on dc sides, respectively. In

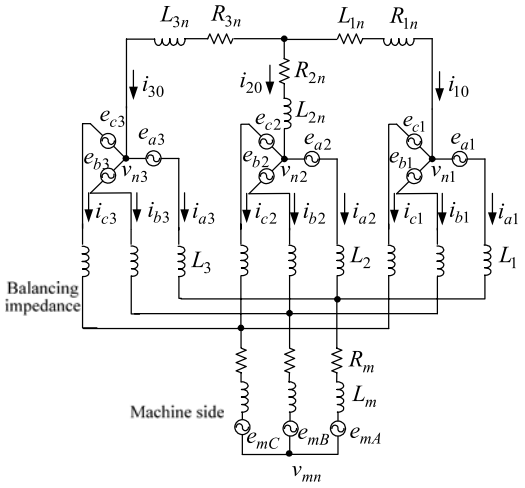


Fig. 2. Equivalent circuit of three inverters fed PMSM drive.

configuration of Fig 1, the zero-sequence current could flow among paralleled VSIs through their balancing impedances and dc capacitors. So, the suppositional neutral points of paralleled VSIs are connected by the equivalent neutral lines. e_{ai}, e_{bi}, and e_{ci} $(i = 1, 2, 3)$ are the equivalent inverter output voltages of inverter *i*. i_{ai}, i_{bi}, and i_{ci} $(i = 1, 2, 3)$ are the injected currents of inverter *i*; i_{aj}, i_{bj}, and i_{cj} $(j = 1, 2, 3,$ and $j \neq i)$ are the injected currents of inverter *j*; and L_i $(i = 1, 2, 3)$ are the balancing impedance of inverter *i*. R_m and L_m are the resistor and inductance of PMSM, and e_{mA}, e_{mB}, and e_{mC} are the back EMF of PMSM. R_{in} and L_{in} $(i = 1, 2, 3)$ are the resistors and inductances in the neutral line of each inverter. The dynamic equations of the system under three-phase stationary frame are described by

$$\begin{bmatrix} e_{ai} \\ e_{bi} \\ e_{ci} \end{bmatrix} = \begin{bmatrix} Z_i + Z_m & 0 & 0 \\ 0 & Z_i + Z_m & 0 \\ 0 & 0 & Z_i + Z_m \end{bmatrix} \begin{bmatrix} i_{ai} \\ i_{bi} \\ i_{ci} \end{bmatrix} + \begin{bmatrix} Z_m & 0 & 0 \\ 0 & Z_m & 0 \\ 0 & 0 & Z_m \end{bmatrix} \begin{bmatrix} \sum_{j=1}^{N} i_{aj} \\ \sum_{j=1}^{N} i_{bj} \\ \sum_{j=1}^{N} i_{cj} \end{bmatrix} + \begin{bmatrix} v_{mn} - v_{ni} \\ v_{mn} - v_{ni} \\ v_{mn} - v_{ni} \end{bmatrix} - \begin{bmatrix} e_{ma} \\ e_{mb} \\ e_{mc} \end{bmatrix} \quad (1)$$

$$\begin{bmatrix} e_{ai} - e_{aj} \\ e_{bi} - e_{bj} \\ e_{ci} - e_{cj} \end{bmatrix} = \begin{bmatrix} Z_i & 0 & 0 \\ 0 & Z_i & 0 \\ 0 & 0 & Z_i \end{bmatrix} \begin{bmatrix} i_{ai} \\ i_{bi} \\ i_{ci} \end{bmatrix} - \begin{bmatrix} Z_j & 0 & 0 \\ 0 & Z_j & 0 \\ 0 & 0 & Z_j \end{bmatrix} \begin{bmatrix} i_{aj} \\ i_{bj} \\ i_{cj} \end{bmatrix} + \begin{bmatrix} Z_{ni} & 0 & 0 \\ 0 & Z_{ni} & 0 \\ 0 & 0 & Z_{ni} \end{bmatrix} \begin{bmatrix} i_{ni} \\ i_{ni} \\ i_{ni} \end{bmatrix} - \begin{bmatrix} Z_{nj} & 0 & 0 \\ 0 & Z_{nj} & 0 \\ 0 & 0 & Z_{nj} \end{bmatrix} \begin{bmatrix} i_{nj} \\ i_{nj} \\ i_{nj} \end{bmatrix} \quad (2)$$

where v_{mn} is the voltage of neutral PMSM, v_{ni} is the voltage of the equivalent neutral point of three-phase voltage source $(i = 1, 2, 3)$, Z_i $(i = 1, 2, 3)$, and Z_j $(j = 1, 2, 3$ and $j \neq i)$ are the balancing impedance of each inverter, and Z_{ni} $(i = 1, 2, 3)$ and Z_{nj} $(j = 1, 2, 3$ and $j \neq i)$ are the impedances in the neutral line of each inverter. The out currents of each inverter i_{ai}, i_{bi}, i_{ci} $(i = 1, 2, 3)$ can be controlled by the equivalent inverter output voltages e_{ai}, e_{bi}, e_{ci} $(i = 1, 2, 3)$, in such a way that the output currents can be controlled equally for paralleled inverters

$$\begin{bmatrix} e_{di} \\ e_{qi} \\ e_{0i} \end{bmatrix} = \begin{bmatrix} Z_i + Z_m & 0 & 0 \\ 0 & Z_i + Z_m & 0 \\ 0 & 0 & Z_i + Z_m \end{bmatrix} \begin{bmatrix} i_{di} \\ i_{qi} \\ i_{0i} \end{bmatrix} + \begin{bmatrix} Z_m & 0 & 0 \\ 0 & Z_m & 0 \\ 0 & 0 & Z_m \end{bmatrix} \begin{bmatrix} \sum_{j=1}^{N} i_{dj} \\ \sum_{j=1}^{N} i_{qj} \\ \sum_{j=1}^{N} i_{0j} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ (v_{mn} - v_{ni}) \end{bmatrix} - \begin{bmatrix} e_{md} \\ e_{mq} \\ e_{m0} \end{bmatrix}. \quad (3)$$

By using Park transform, the model of the paralleled VSIs fed system under synchronous frame is given in (3), where e_{di}, e_{qi}, and e_{0i} $(i = 1, 2, 3)$ are the equivalent *d*-axis, *q*-axis, and 0-axis output voltages of inverter *i*. i_{di}, i_{qi}, and i_{0i} $(i = 1, 2, 3)$ are the equivalent *d*-axis, *q*-axis, and 0-axis output currents of inverter *i*. The *d*-axis and *q*-axis output voltages e_{di} and e_{qi} are modulated to regulate i_{di} and i_{qi} for inverter *i*. To enable controlling the zero-sequence current i_{0i}, the zero-sequence output voltage e_{0i} could be adjusted by tuning the dwelling time of zero-sequence voltage vectors dynamically [7].

III. FOC Under Synchronous Frame With Chaotic SVM

A. FOC Under Synchronous Frame

The synchronous frame-based FOC for paralleled inverters fed PMSM system is presented in Fig. 3. The *d*-axis is aligned with the magnetic field excited by a rotor, and the *q*-axis is $\pi/2$ ahead of *d*-axis. The *q*-axis current reference is generated by the closed-loop speed controller. Divide this value by the inverter number, the *q*-axis current reference for each inverter is obtained. The *d*-axis current references are all set as zero. The *d*-axis and *q*-axis current controllers generate the voltage

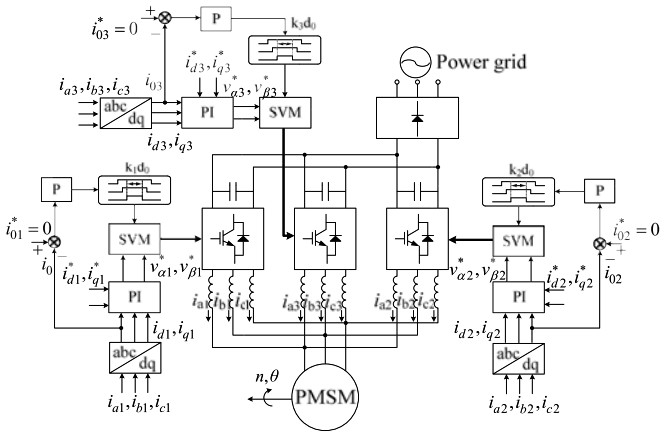


Fig. 3. Control diagram of FOC with SVM for paralleled VSIs fed PMSM drive under synchronous frame.

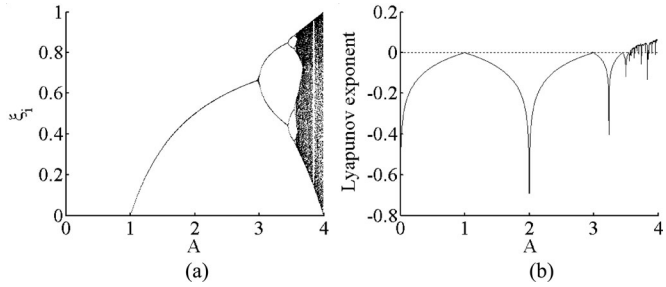


Fig. 4. Logistic map: (a) Bifurcation diagram; (b) Lyapunov exponent.

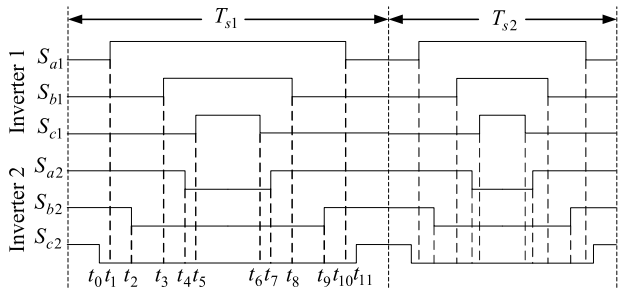


Fig. 5. Switching pattern design-based phase-shifted chaotic SVM.

references, and the SVM can be used to modulate the voltage references. Besides, to control the zero-sequence currents for the drive system, the dynamic tuning of dwelling time of zero-voltage vectors is introduced in Fig. 3. The variable k_i $(i = 1, 2, 3)$ are defined to represent the ratio of dwelling time of zero-voltage vector (*ppp*) to the total dwelling time of zero-voltage vectors (*ppp*) and (*nnn*), where (*ppp*) means all the three upper switches of the inverter are turned ON and (*nnn*) means all the three lower switches are turned ON. The symbol d_0 represents the total dwell time of zero-voltage vectors (*ppp*) and (*nnn*) in one switching period. The increase in dwelling time of voltage vector (*ppp*) of inverter *i* indicates the zero-sequence output voltage e_{0i} becomes larger. Otherwise, e_{0i} is smaller.

B. Phase-Shifted Chaotic SVM Strategies

For the switching strategies for the paralleled VSI fed drives, some specific switching harmonics can be suppressed by shifting switching intervals among paralleled inverters. For SPWM, the carriers can be shifted with $1/f_sN$ in time domain, where f_s is the switching frequency and N is the paralleled inverter number. Thus, the switching harmonics around f_s, $2f_s$,...,$(N-1)f_s$ and their multiples will be suppressed. The equivalent switching harmonics is increased to Nf_s [32]. The principle of the phase-shifted SVM is similar to that of phase-shifted SPWM. An interleaved sampling interval of $1/f_sN$ is used for SVM in different inverters.

To further improve the harmonic performance of paralleled VSIs fed drives, the phase-shifted chaotic SVM is proposed to reduce the remaining peaky switching harmonics. The key is to tune the switching frequency chaotically within each switching interval. The simple chaotic map such as the Logistic map given in (4) is used to generate the chaotic series to chaoize the switching frequency. Fig. 4 shows the bifurcation diagram and Lyapunov exponents of the Logistic map with change of control parameter *A*. The real switching frequency can be implemented by using (5), where $f_{\exp}$ is the average value of switching frequency and Δf is the varying range of switching frequency. It indicates that the values of the chaotic series ξ_i will be distributed uniformly within (0, 1) while *A* is approaching to 4. The magnitude of peaky harmonics will be reduced with the increase of Δf_s. On the other hand, the increase of Δf_s will result in variable switching frequencies. The switching frequencies become higher in some periods and become lower in other periods. The higher switching frequencies will result in larger switching losses, and the lower switching frequencies will produce more harmonics in the low-frequency domain. So, Δf_s should be designed by considering these aspects comprehensively. In this paper, Δf_s is given to be 1/5 of the average switching frequency $f_{\exp}$

$$\xi_{i+1} = A\xi_i(1-\xi_i), \quad A \in [0, 4) \tag{4}$$

$$f_s = f_{\exp} + \Delta f_s(\xi_i - 0.5). \tag{5}$$

By using (5), the values for switching frequency f_s are generated with the iterated series of ξ_i. At the end of each switching interval, the period of the next switching interval will be updated according to the generated f_s. This could be implemented by setting the period registers of counters in controller chip. Since the series of ξ_i are chaotic, the values of switching frequency f_s and the switching periods will vary in a chaotic way.

To find a proper phase-shifted chaotic SVM strategy, two phase-shifted chaotic SVM schemes are designed and compared. The two VSIs system is used for exemplification. The first phase-shifted chaotic SVM is proposed based on designing different switching patterns for paralleled inverters, and the so-called switching pattern design-based method. As shown in Fig. 5, the switching patterns of the two inverters are designed for sector I. $S_{x1}(x = a, b, c)$ represent the states of three upper switches of inverter 1, and $S_{x2}(x = a, b, c)$ represent the states of three upper switches of inverter 2. When S_{x1} or S_{x2} is in

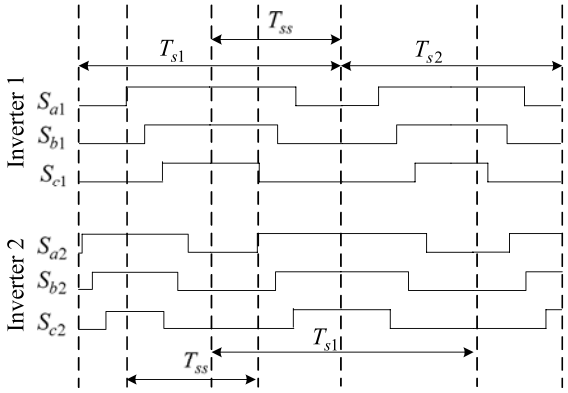


Fig. 6. Uniquely interleaved sampling-based phase-shifted chaotic SVM.

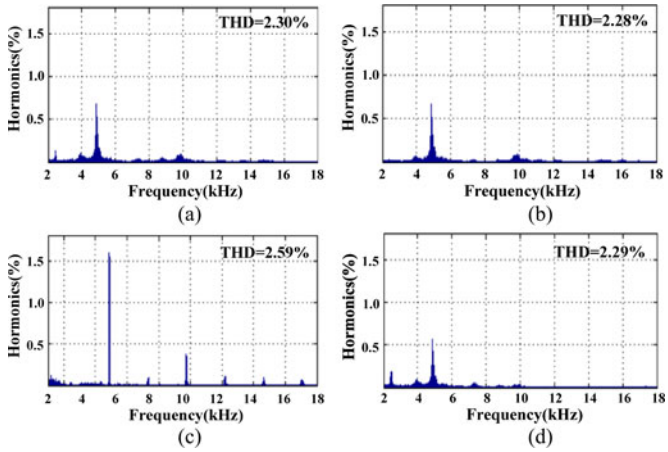


Fig. 7. Spectrum comparison: (a) phase-shifted chaotic SVM with switching pattern design method; (b) phase-shifted chaotic SVM with uniquely interleaved sampling method; (c) phase-shifted fixed-switching frequency SVM; (d) asynchronous chaotic SVM.

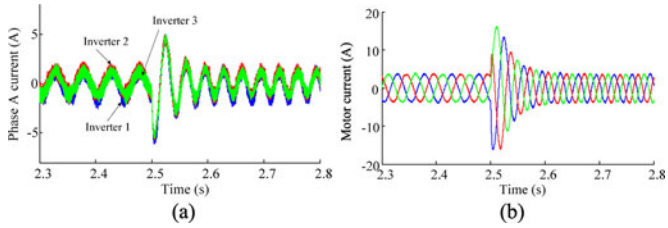


Fig. 8. Simulated drive performance with phase-shifted chaotic SVM by uniquely interleaved sampling: (a) phase A currents in three inverters; (b) PMSM motor current.

high level, the upper switch of the corresponding phase turns ON. Otherwise, the upper switch turns OFF. For inverter 1, the *ppp* zero-voltage vector is located at the center of each switching period, while the dwell time of *nnn* zero-voltage vector is divided and distributed at two sides of the switching period. For inverter 2, the *nnn* zero-voltage vector is in the middle, while the dwell time of *ppp* zero-voltage vector is divided and located at two sides of the switching period. This design corresponds to 180° shift in phases of two inverters. At the same time, the switching periods are changed chaotically during operation. The switching periods $T_{s1} \neq T_{s2}$. The switching patterns are similar in other sections. This phase-shifted chaotic SVM method has symmetric switching waveforms and the sampling instants are kept synchronously for the two inverters. However, this switching pattern design-based method is very difficult to be applied in more inverters fed drive system.

To implement the phase-shifted chaotic SVM more flexibly, the second phase-shifted chaotic SVM, namely the uniquely interleaved sampling method is proposed. The principle is shown in Fig. 6. As shown in this figure, the switching periods are chaoized at first. The switching periods $T_{s1} \neq T_{s2}$. Although the switching periods are variable, there is a uniquely interleaved sampling period, namely T_{ss} among paralleled inverters. Such interleaved sampling period is kept constant throughout the operation. The value of T_{ss} is designed as $1/N$ of the average value of chaotic switching periods.

To evaluate the performance of these phase-shifted chaotic SVM strategies, the simulation on two paralleled inverters fed PMSM is given with the average switching frequency of 2.5 kHz, the change range of switching frequency is 500 Hz, and the fundamental frequency of 15 Hz. Since the signals are sample once within each switching period, the sampling frequencies vary with the change of switching frequency. So, the sampling frequencies of interleaved chaotic PWM schemes vary around 2.5 kHz. The results are shown in Fig. 7. In the comparison, the PMSM parameters are: the pole pair number $n_p = 2$, the d-axis and q-axis inductances are 4.607 and 4.713 mH, respectively, the stator resistor is 0.767 Ω, the PM flux peak is 0.1377 Wb, the balancing impedance is 7 mH, and the dc-link voltage is 100 V. The result indicates that the two phase-shifted chaotic SVM strategies exhibit similar performance in spectrum in Fig. 7(a) and (b). The phase-shifted chaotic SVM strategies cannot only eliminate the switching harmonics around 2.5 kHz and their multiples, but also reduce the peaks for all remaining switching harmonics. Besides, the uniquely interleaved sampling method is easier to be applied for more inverters fed drive system. Furthermore, the traditional phase-shifted SVM with fixed switching frequency and asynchronous chaotic SVM are given for comparison in Fig. 7(c) and (d), respectively. It is observed that the traditional phase-shifted SVM with fixed switching frequency can eliminate the switching harmonic around 2.5 kHz but the remaining switching harmonics still exhibit distinct peaks. By using independent chaotic switching frequencies for paralleled inverters, the asynchronous chaotic SVM can reduce the peaky values for all switching harmonics. However, the switching harmonics around 2.5 kHz and their multiples still exist.

Fig. 8 shows the simulated performance of three paralleled VSIs fed PMSM drive with the proposed phase-shifted chaotic SVM by uniquely interleaved sampling. The system parameters are same as those in the last paragraph. The balancing impedances of the three inverters are purposely designed with different values of 7, 5, and 7 mH. The speed increases from 600 to 900 r/min at $t = 2.5$ s. During the transient process, it can be observed that the currents of three inverters can be balanced well. Besides, as shown in Fig. 8(b), the PMSM currents

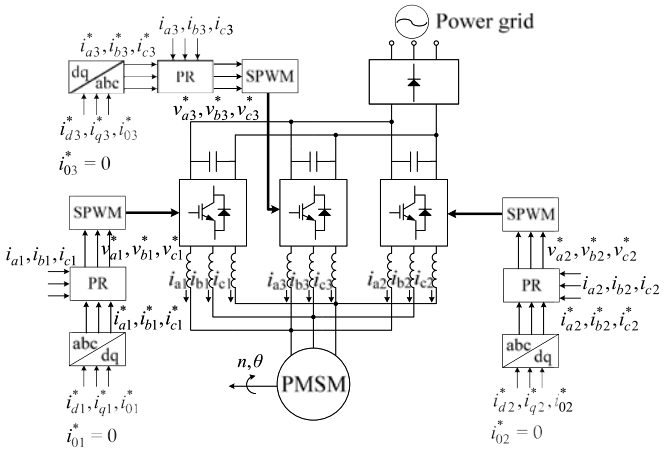


Fig. 9. Control diagram for paralleled inverters fed PMSM drive under stationary frame.

exhibit good waveforms though large ripples appear in the current waveforms of inverters, which are caused by the interleaved operation and different balancing impedances.

IV. FOC Under Stationary Frame With Chaotic SPWM

A. FOC Under Stationary Frame

The FOC of PMSM can also be implemented in stationary frame reference, and the block diagram is shown in Fig. 9. The q-axis current references $i^*_{qi}(i = 1, 2, 3)$ are also generated by dividing the output of the closed-loop motor speed controller, and the d-axis and 0-axis current references $i^*_{di}(i = 1, 2, 3)$ and $i^*_{0i}(i = 1, 2, 3)$ are fixed to be zero. Different from the control under synchronous frame, i^*_{di}, i^*_{qi}, and i^*_{0i} $(i = 1, 2, 3)$ are transformed to the three-phase current references, namely i^*_{ai}, i^*_{bi}, and i^*_{ci} for the ith inverter under stationary frame. To regulate the sinusoidal currents under stationary frame, the proportional resonant (PR) control can be used and generate the voltage references v^*_{ai}, v^*_{bi}, and v^*_{ci}. Then, the SPWM are used to modulate the voltage references. The current references i^*_{ai}, i^*_{bi}, and i^*_{ci} will not contain zero-sequence component, since zero-sequence current references $i^*_{0i}(i = 1, 2, 3)$ are fixed to be zero, as shown in Fig. 9. By using PR current controller, the actual phase current i_{ai}, i_{bi}, i_{ci} could track i^*_{ai}, i^*_{bi}, i^*_{ci} accurately. Thus, the zero-sequence circulating current can be suppressed naturally.

B. Phase-Shifted Chaotic SPWM Strategy

Similar to the phase-shifted chaotic SVM, the phase-shifted chaotic switching technique can also be applied for SPWM strategies. Also, the uniquely interleaved chaotic SPWM is easy to extend to more VSIs fed drives. Fig. 10 shows the principle of the phase-shifted chaotic SPWM used in this paper. A uniquely shifted phase is designed among carrier signals for paralleled VSIs. Moreover, the frequencies of carrier signals are varying chaotically for paralleled VSIs. By comparing the three-phase modulating signals and chaotic carrier signals, the gating signals, namely $u_{\rm ga1}$ and $u_{\rm ga2}$ are generated for phase A of two paralleled inverters.

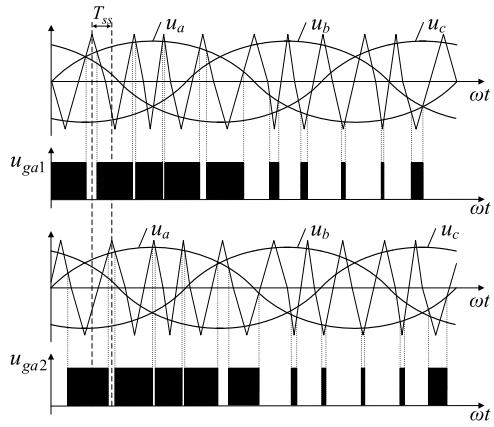


Fig. 10. Principle of phase-shifted chaotic SPWM.

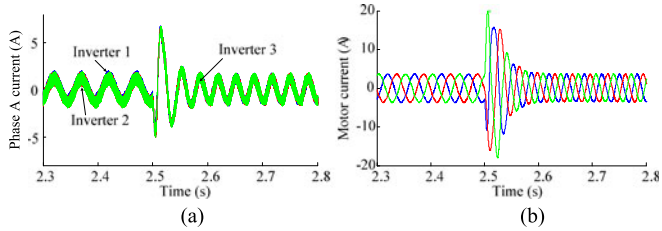


Fig. 11. Simulated drive performance with interleaved chaotic SPWM: (a) phase A currents in three inverters; (b) PMSM motor current.

Fig. 11 shows the simulated performance of three inverters fed PMSM drive by using the proposed phase-shifted chaotic SPWM under the stationary frame. The system parameters are same as those in Fig. 8. First, the PMSM current in Fig. 11(b) is good by using the interleaved chaotic SPWM although large current ripples exist in the inverter currents in Fig. 11(a). Second, the inverter currents are balanced well and there is no circulating current during the transient process with the proposed current controller.

V. DTC With Circulating Current Suppression

The DTC is another control scheme for paralleled VSIs fed PMSM drives with variable switching frequencies. Two control targets are to be considered in the proposed DTC for paralleled VSIs fed PMSM: the torque and stator flux regulation of PMSM, and the suppression of circulating currents among paralleled VSIs. Fig. 12 shows the block diagram of the proposed DTC for paralleled VSIs fed PMSM. There are two parts in the control diagram: one is the traditional DTC for each VSI, and the other is the circulating currents suppression among paralleled VSIs. The DTC for each VSI is shown in Fig. 13(a), and the torque and stator flux are calculated by measured stator voltages and currents of PMSM. By using a switching logic in Fig. 13(b), the proper switching vector is chosen to track the torque and stator flux references. To suppress the circulating currents, the hysteresis current controller is used for the phase currents in each inverter i_{ai}, i_{bi}, and i_{ci} $(i = 1, 2, 3)$ to track average phase currents of paralleled inverters $i_{a\_\rm ave}$, $i_{b\_\rm ave}$, and

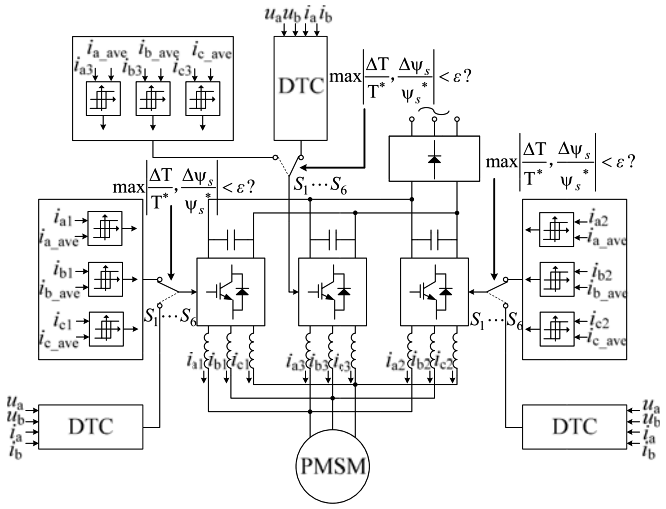


Fig. 12. Proposed DTC with circulating current suppression for paralleled inverters fed PMSM drive.

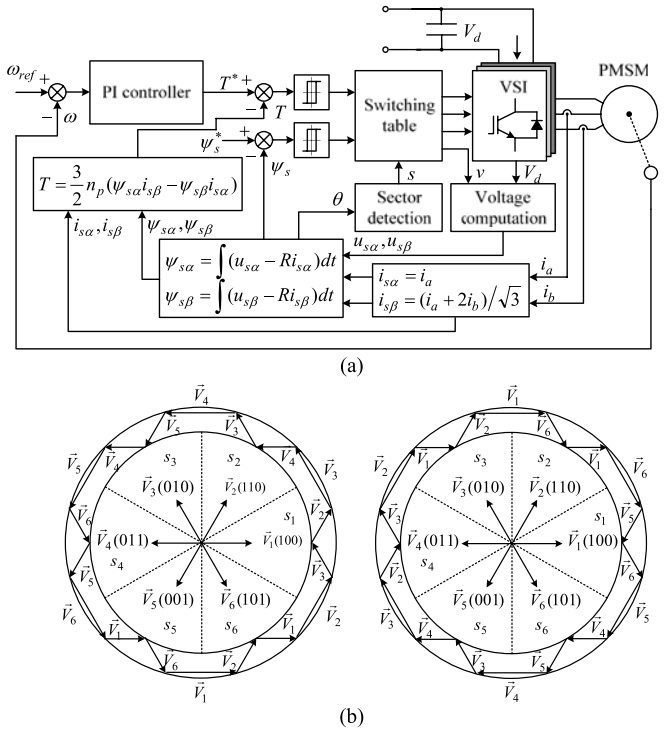


Fig. 13. Control scheme of DTC: (a) control diagram; (b) switching logics.

i_{c_ave}. For example, If all phase currents of inverter 1 are less than the corresponding average phase currents, the condition will be $i_{a1} < i_{a\_ave}$, $i_{b1} < i_{b\_ave}$, and $i_{c1} < i_{c\_ave}$. Based on the hysteresis current controller, all the three upper switches of inverter 1 are turned ON and the three-phase output voltages of inverter 1 are maximized. Thus, the three-phase currents of inverter 1 will increase and approach close to the average values i_{a_ave}, i_{b_ave}, and i_{c_ave}. When the phase currents of all inverters could track the average phase currents, the currents of inverters will be balanced and the circulating currents are suppressed naturally.

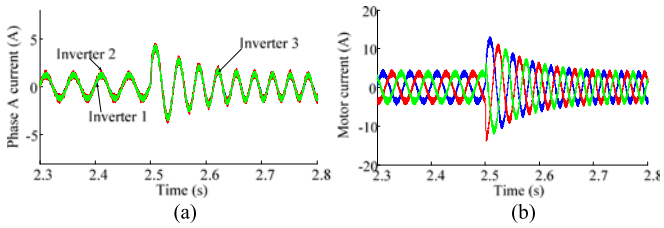


Fig. 14. Simulated drive performance by using DTC with circulating current suppression: (a) phase A currents in three inverters; (b) PMSM motor current.

The two parts in the control are chosen according to the performance of regulating torque and stator flux. As shown in Fig. 12, if the maximum value of relative torque tracking error and the stator flux tracking error is larger than a threshold ε, the DTC part in Fig. 13 will be ineffective. On the other hand, when the maximum value of the relative torque tracking error and the stator flux tracking error is smaller than the threshold ε, the hysteresis controllers for suppressing the circulating currents will be effective. Thus, the torque and the flux regulation, and the suppression of circulating current are implemented. The DTC adopts the torque hysteresis and the flux hysteresis loop to generate the switching signals, while the circulating current controllers use the current hysteresis loop to generate the switching signals. The switching actions of inverters are dependent of dynamics of torque, flux, circulating currents, and hysteresis band.

Fig. 14 shows the simulated performance of three VSIs fed PMSM drive using the proposed DTC scheme with circulating current suppression. The system parameters are same as those in Figs. 8 and 11. But different from Figs. 8 and 11, the sampling frequency of the DTC scheme is set as 10 kHz. It should be noted that the actual switching frequency is much lower than the sampling frequency for DTC since the switching state may not be changed within some sampling periods. It is also observed that the currents of three paralleled inverters are controlled synchronously by incorporating the circulating current suppression. Meanwhile, the effect of DTC is maintained.

VI. Experimental Verification

The experimental setup is given to verify the performance of the proposed FOC schemes with chaotic PWM and DTC scheme for paralleled VSIs fed PMSM. Fig. 15 shows the photograph of the experimental setup. As shown in the figure, paralleled inverters are used to supply a PMSM. The key parameters of PMSM are shown in Table I. The PMSM is coupled to a PMSG mechanically. The PMSG supplies power for the three-phase load resistors. The power inverters are built with the Mitsubishi intelligent power module PS21A79, and the control platform is constructed based on DSP TMS320F2812 and FPGA (Xilinx XC6LX16-CSG324). The speed is measured by an encoder (Omron E6B2-CW21X) with 1024 pulses per rotation. The phase currents are measured by current sensors (LEMLA-25P). The communication between DSP and FPGA is implemented with the serial peripheral interface.

First, the performance of the FOC under synchronous frame is investigated. Fig. 16 shows the steady-state current

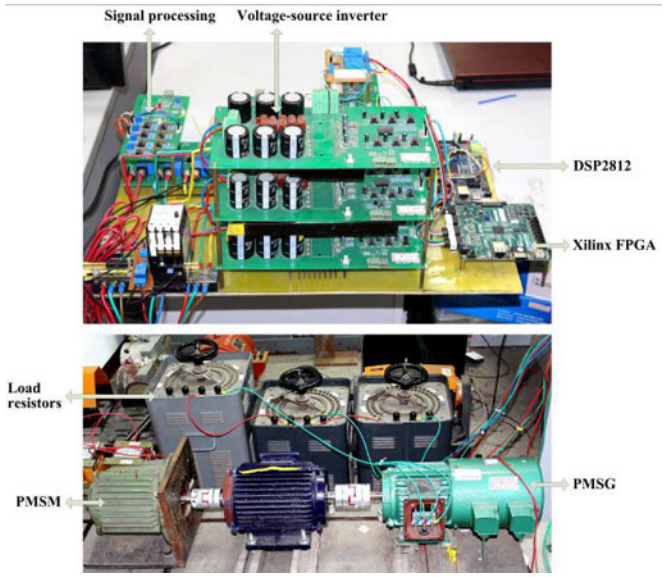


Fig. 15. Photograph of experimental setup of three paralleled inverters fed PMSM drive.

TABLE I
EXPERIMENTAL PARAMETERS

Name	Quantity	Unit
Pole pair number	2	
Stator resistance	0.767	Ω
PM flux (peak)	0.1377	Wb
q-axis inductance	4.607	mH
d-axis inductance	4.713	mH
Average switching frequency	2.5	kHz
Changing range of switching frequency	500	Hz
Rated power	0.4	kW
Rated speed	1500	rpm
Rated current	4.66	A
Rated torque	2.5	Nm
Inertia	6.876×10^{-3}	kg·m^2

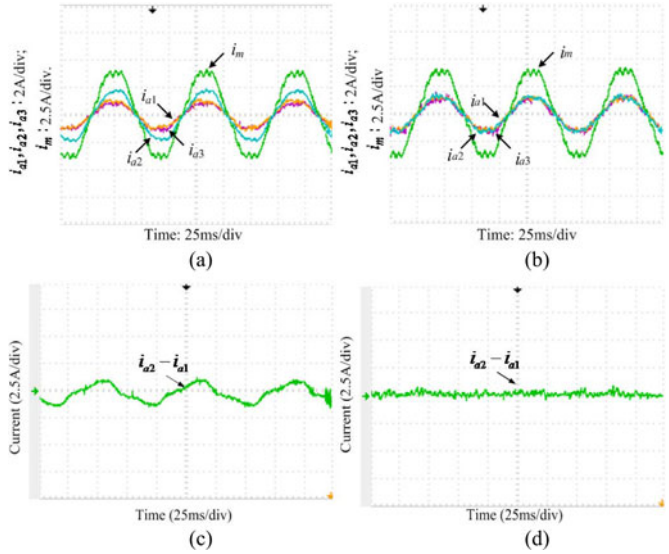


Fig. 16. Measured currents for three paralleled inverters fed PMSM drive (i_{a1}, i_{a2}, i_{a3}: inverter currents; n: rotor speed): (a) without circulating current suppression; (b) with circulating current suppression; (c) imbalance current without circulating current suppression; (d) imbalance current with circulating current suppression.

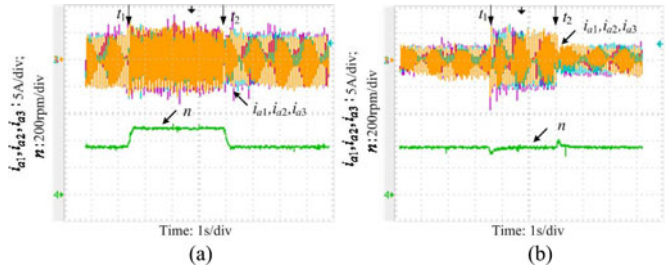


Fig. 17. Measured currents for three paralleled inverters fed PMSM drive (i_{a1}, i_{a2}, i_{a3}: inverter currents; n: rotor speed): (a) dynamic speed response; (b) dynamic load response.

waveforms of inverters and PMSM. The rotor speed is 360 r/min; as shown in Fig. 16(a), the currents in three paralleled inverters are not identical without circulating current suppression due to the different balancing impedances. By using the circulating current suppression method, the currents in paralleled inverters are controlled identically as shown in Fig. 16(b). The total current in PMSM in Fig. 16(a) is same as that in Fig. 16(b)–(d) plot the imbalance current of paralleled inverters without and with circulating current suppression, respectively. Fig. 17 shows the dynamic performance of paralleled inverters fed PMSM drive with FOC under synchronous frame. Fig. 17(a) plots the speed response of system, where the drive is accelerated from 360 to 500 r/min at t_1 instant, while it is decelerated back to 360 r/min at t_2 instant. The rotor speed tracks the reference value well. It is noticed that the load torque is changed during the change of rotor speed. The reason is that the back EMF of PMSG is changed and the power consumed is changed with the change of rotor speed. Fig. 17(b) plots the load response, where the load is increased suddenly at t_1 instant, while it is reduced suddenly at t_2 instant. The amplitudes of current waveforms are changed, while the rotor speed is kept stable during the process.

The harmonic performance of PMSM current is compared among different switching strategies for paralleled inverters fed PMSM with FOC under synchronous frame in Fig. 18. As shown in Fig. 18(a), the distinct switching harmonics around multiples of switching frequencies appear in the PMSM current spectrum with the traditional fixed-switching-frequency SVM for paralleled inverters. By using the phase-shifted fixed-switching-frequency SVM, the switching harmonics around 2.5 and 5 kHz are eliminated in Fig. 18(b). Then, the chaotic switching frequency is applied. In Fig. 18(c), the switching harmonics is spread out around the multiples of switching frequency, and the peaky harmonics are reduced with asynchronous chaotic SVM. By using the proposed phase-shifted chaotic SVM, not only the switching harmonics around 2.5 and 5 kHz are eliminated but also the peaks around all remaining switching harmonics are reduced effectively, as shown in Fig. 18(d).

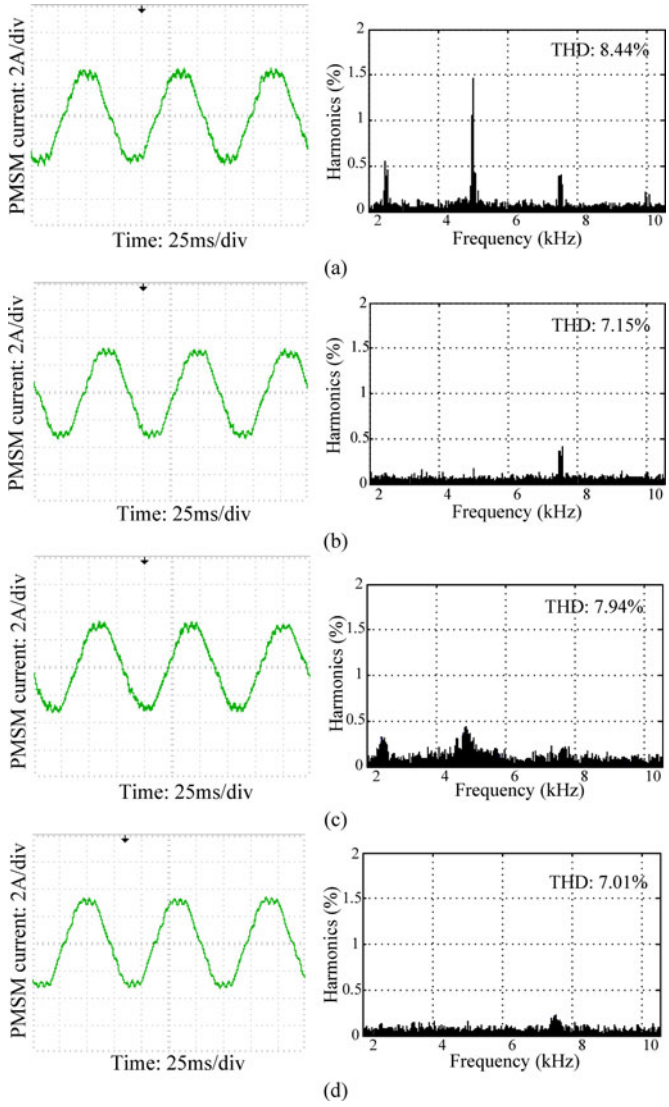


Fig. 18. Measured current waveforms and spectrum for three paralleled inverters fed PMSM drive under synchronous frame: (a) synchronous SVM with fixed switching frequency; (b) phase-shifted SVM with fixed switching frequency; (c) asynchronous chaotic SVM; (d) phase-shifted chaotic SVM.

Second, the performance of the FOC under stationary frame is investigated for the paralleled VSIs fed drive. Fig. 19(a) and (b) shows the steady-state current waveforms of inverters with equal balancing impedances and with unequal balancing impedances in paralleled inverters, respectively. The rotor speed is 500 r/min. In Fig. 19(a), the balancing impedances are all 7 mH, while the balancing impedance of one inverter is changed to 5 mH in Fig. 19(b). Under both of these two conditions, the currents in the three inverters can be controlled identically under stationary frame. The dynamic performance of the drive in stationary frame is plotted in Fig. 20. Fig. 20(a) shows the starting process of the drive system with speed from 0 to 500 r/min. During the process, the q-axis current tracks the q-axis current reference quickly and accurately and the rotor accelerates stably. Fig. 20(b) presents the dynamic performance while the load torque is changed suddenly. The q-axis current is controlled effectively to accommodate for the change of load. The rotor

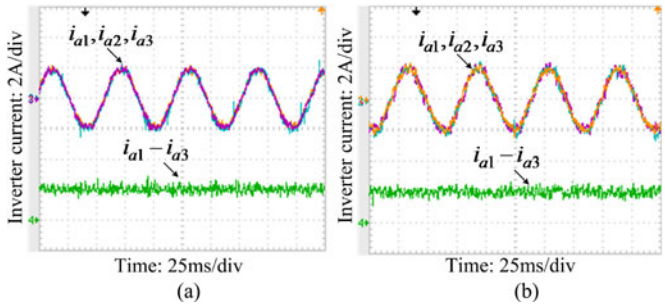


Fig. 19. Measured inverter output currents for three paralleled inverters fed PMSM drive under stationary frame (i_{a1}, i_{a2}, i_{a3}: inverter output currents): (a) with equal balancing impedances; (b) with different balancing impedances.

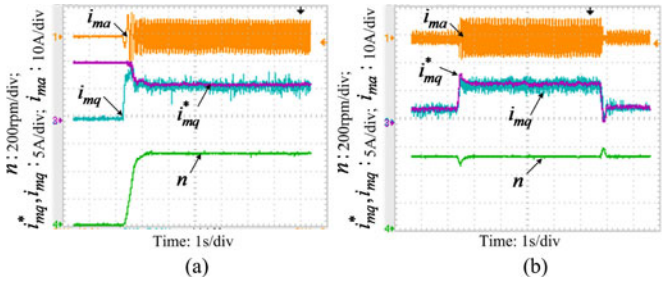


Fig. 20. Measured dynamic performance for three paralleled inverters fed PMSM drive under stationary frame (n: rotor speed; i^*_{mq}: q-axis current reference of PMSM; i_{mq}: q-axis current of PMSM; i_{ma}: phase A current): (a) starting process; (b) dynamic load response.

speed is maintained at 500 r/min except slight perturbation at the instants of sudden change in load.

Then, the spectrum performance of PMSM current is compared among different switching strategies for paralleled inverters fed PMSM with FOC under stationary frame in Fig. 21. Similar to comparison under synchronous frame, the distinct switching harmonics can be observed clearly with fixed-switching-frequency SPWM in Fig. 21(a). The switching harmonics around 2.5 and 5 kHz are eliminated by phase-shifted SPWM with fixed switching frequency in Fig. 21(b). By using the asynchronous chaotic SPWM for paralleled inverters in Fig. 21(c), the peaky harmonics around multiples of switching frequency are reduced but the switching harmonics around 2.5 and 5 kHz still exist. Consequently, the phase-shifted chaotic SPWM is used and the best performance is obtained in Fig. 21(d), where the spectrum seems flat compared the three other SPWM strategies.

The DTC for two VSIs fed PMSM is tested by experiments. Fig. 22 shows the steady-state performance of the proposed method. It is observed that the torque tracking is effective and the stator flux is controlled stable with DTC in Fig. 22(a). The three-phase current waveforms in PMSM are also good in Fig. 22(b). For comparison, the performances of DTC for the system with and without circulating current suppression are shown in Fig. 23(a) and (b), respectively. It indicates that the unbalance of currents in two VSIs is mitigated effectively by incorporating the proposed hysteresis control for circulating current. The dynamic performance of the paralleled PMSM

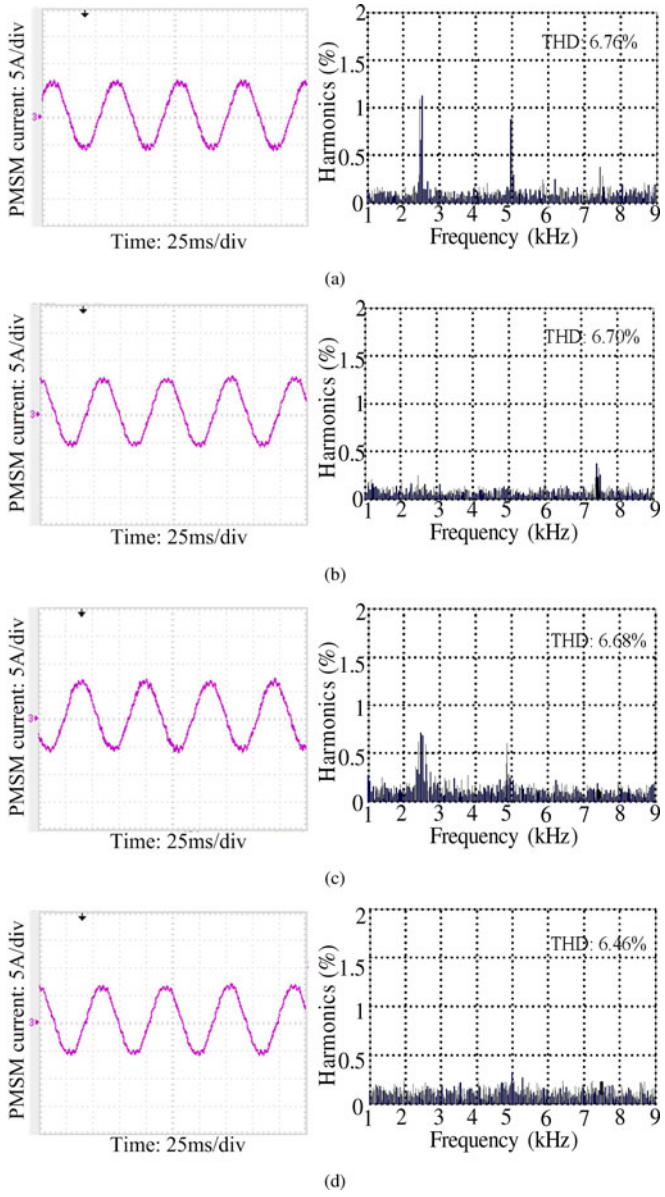


Fig. 21 Measured current waveforms and spectrum for three paralleled inverters fed PMSM drive under stationary frame: (a) synchronous SPWM with fixed switching frequency; (b) phase-shifted SPWM with fixed switching frequency; (c) asynchronous chaotic SPWM; (d) phase-shifted chaotic SPWM.

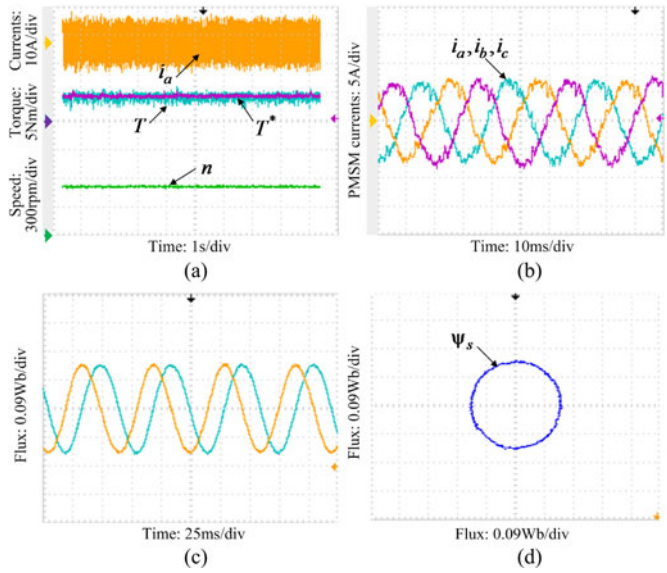


Fig. 22. Measured steady-state performance of two VSIs fed PMSM drive with proposed DTC: (a) torque and rotor speed waveforms; (b) PMSM current waveforms; (c) stator flux waveforms; (d) stator flux trajectory.

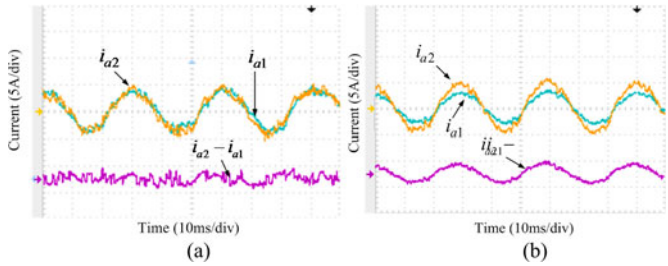


Fig. 23. Measured steady-state performance of two VSIs fed PMSM drive with DTC: (a) with circulating current suppression; (b) without circulating current suppression.

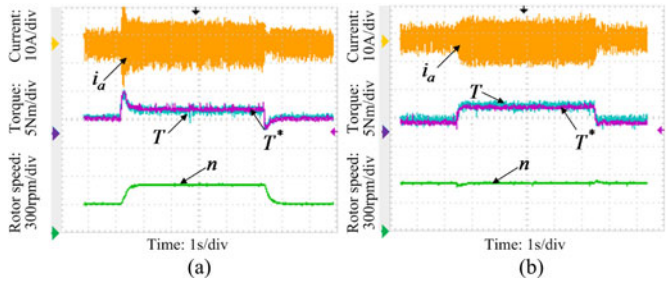


Fig. 24. Measured dynamic performance of two VSIs fed PMSM drive with the proposed DTC: (a) dynamic speed response; (b) dynamic load response.

drives with the proposed DTC is shown in Fig. 24. In Fig. 24(a), the rotor speed is accelerated from 300 to 500 r/min, and decelerated back to 300 r/min again. In Fig. 24(b), when the load resistors are connected, the load torque is increased suddenly. On the contrary, the load resistors are disconnected and the load torque will be decreased suddenly. This figure indicates that good dynamic performance is given by the paralleled VSIs fed PMSM with the proposed DTC.

Finally, the low-order harmonics of the paralleled VSIs fed drives are investigated. Fig. 25(a) shows the measured low-order harmonics of the back EMF of PMSM, while Fig. 25(b)—(d) shows the measured low-order harmonics of PMSM currents with the proposed interleaved SVM under synchronous frame, the proposed interleaved SPWM under stationary frame and the DTC with circulating current suppression, respectively. It can be observed that the low-order harmonics of currents using the three proposed schemes are similar, and they are also related to the low-order harmonics in back EMF of PMSM.

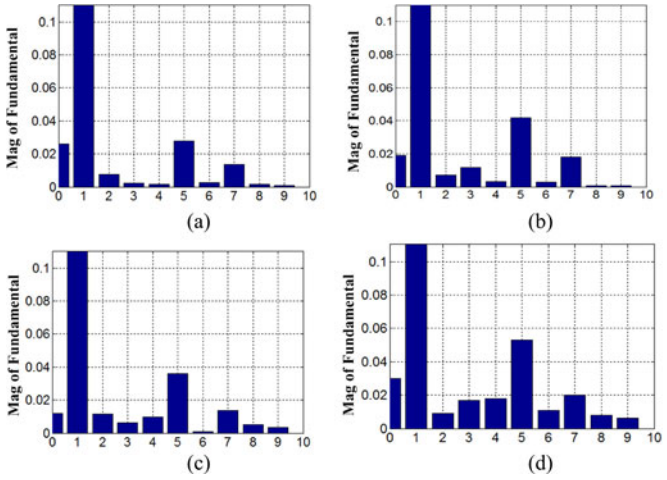


Fig. 25. Measured low order harmonics: (a) back EMF; (b) phase-shifted chaotic SVM; (c) phase-shifted chaotic SPWM; (d) DTC with circulating current suppression.

REFERENCES

[1] S. Kouro, J. Rodriguez, B. Wu, S. Bernet, and M. Perez, "Powering the future of industry: High-power adjustable speed drive topologies," *IEEE Ind. Appl. Mag.*, vol. 18, no. 4, pp. 26–39, Jul./Aug. 2012.

[2] S. Schröder, P. Tenca, T. Geyer, P. Soldi, L. Garces, R. Zhang, T. Toma, and P. Bordignon, "Modular high-power shunt-interleaved drive systems: A realization up to 35 MW for oil and gas applications," *IEEE Ind. Appl. Soc. Annu. Meet.*, Oct. 2008, pp. 1–8.

[3] L. J. J. Offringa and J. L. Duarte, "A 1600kW IGBT converter with interphase transformer for high speed gas turbine power plants," *IEEE Ind. Appl. Soc. Annu. Meet.*, Oct. 2000, pp. 2243–2248.

[4] T. Yoshikawa, H. Inaba, and T. Mine, "Analysis of parallel operation methods of PWM inverter sets for an ultra-high speed elevator," *Proc. IEEE 15th Annu. Appl. Power Electron. Conf. Expo.*, 2000, pp. 944–950.

[5] R. Li and D. Xu, "Parallel operation of full power converters in permanent-magnet direct-drive wind power generation system," *IEEE Trans. Ind. Electron.*, vol. 60, no. 4, pp. 1619–1629, Apr. 2013.

[6] C. T. Pan and Y. H. Liao, "Modeling and coordinate control of circulating currents in parallel three-phase boost rectifier," *IEEE Trans. Ind. Electron.*, vol. 54, no. 2, pp. 825–838, Apr. 2007.

[7] Z. Ye, D. Boroyevich, J. Y. Choi, and F. C. Lee, "Control of circulating current in two parallel three-phase boost rectifiers," *IEEE Trans. Power Electron.*, vol. 17, no. 5, pp. 609–615, Sep. 2002.

[8] J. Zhang, J. Lai, R. Kim, and W. Yu, "High-power density design of a soft-switching high-power bidirectional dc–dc converter," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1145–1153, Jul. 2007.

[9] B. Mwinyiwiwa, B. T. Ooi, and Z. Wolanski, "UPFC using multiconverter operated by phase-shifted triangle carrier SPWM strategy," *IEEE Trans. Ind. Appl.*, vol. 34, no. 3, pp. 495–500, May/Jun. 1998.

[10] E. P. Wiechmann, R. P. Burgos, and J. Holtz, "Active front-end converter for medium-voltage current-source drives using sequential-sampling synchronous space-vector modulation," *IEEE Trans. Ind. Electron.*, vol. 50, no. 5, pp. 1275–1289, Dec. 2003.

[11] G. Konstantinou, V. G. Agelidis, and J. Pou, "Theoretical considerations for single-phase interleaved converters operated with SHE-PWM," *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5124–5128, Oct. 2014.

[12] S. K. Mazumder, "Continuous and discrete variable-structure controls for parallel three-phase boost rectifier," *IEEE Trans. Ind. Electron.*, vol. 52, no. 2, pp. 340–354, Apr. 2005.

[13] K. Xing, F. C. Lee, D. Borojevic, Z. Ye, and S. Mazumder, "Interleaved PWM with discontinuous space-vector modulation," *IEEE Trans. Power Electron.*, vol. 14, no. 5, pp. 906–917, Sep. 1999.

[14] D. Zhang, F. Wang, R. Burgos, and D. Boroyevich, "Total flux minimization control for integrated inter-phase inductors in paralleled, interleaved three-phase two-level voltage-source converters with discontinuous space-vector modulation," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1679–1688, Apr. 2012.

[15] Z. Wang, B. Wu, D. Xu, and N.R. Zargari, "Hybrid PWM for high-power current-source-inverter-fed drives with low switching frequency," *IEEE Trans. Power Electron.*, vol. 26, no. 6, pp. 1754–1764, Jul. 2011.

[16] R. Lynn Kirlin, S. Kwok, S. Legowski, and A. M. Trzynadlowski, "Power spectra of a PWM inverter with randomized pulse position," *IEEE Trans. Power Electron.*, vol. 9, no. 5, pp. 463–472, Sep. 1994.

[17] A. M. Trzynadlowski, Z. Wang, J. M. Nagashima, C. Stancu, and M. H. Zelechowski, "Comparative investigation of PWM techniques for a new drive for electric vehicles," *IEEE Trans. Ind. Appl.*, vol. 39, no. 5, pp. 1396–1403, Sep./Oct. 2003.

[18] Y. S. Lai and B. Y. Chen, "New random PWM technique for a full-bridge dc/dc converter with harmonic intensity reduction and considering efficiency," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 5013–5023, Nov. 2013.

[19] E. N. Y. Ho and P. K. T. Mok, "Design of PWM ramp signal in voltage-mode CCM random switching frequency buck converter for conductive EMI reduction," *IEEE Trans. Circuits Syst. I, Reg. Papers*, pp. 505–515, Feb. 2013.

[20] C. M. Liaw, Y. M. Lin, C. H. Wu, and K. I. Hwu, "Analysis, design, and implementation of a random frequency PWM inverter," *IEEE Trans. Power Electron.*, vol. 15, no. 5, pp. 843–854, Sep. 2000.

[21] Y. Shrivastava and S. Y. Hui, "Analysis of random PWM switching methods for three-level power inverters," *IEEE Trans. Power Electron.*, vol. 14, no. 6, pp. 1156–1163, Nov. 1999.

[22] B. R. Lin and H. H. Lu, "Single-phase three-level rectifier and random PWM inverter drives," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 35, no. 4, pp. 1334–1343, Oct. 1999.

[23] A. Kavousi, B. Vahidi, R. Salehi, M. K. Bakhshizadeh, N. Farokhnia, and S. H. Fathi, "Application of the bee algorithm for selective harmonic elimination strategy in multilevel inverters," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1689–1696, Apr. 2012.

[24] K. Borisov, H. L. Ginn II, and A. M. Trzynadlowski, "Attenuation of electromagnetic interference in a shunt active power filter," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 1912–1918, Sep. 2007.

[25] K. Borisov, T. E. Calvert, J. A. Kleppe, E. Martin, and A. M. Trzynadlowski, "Experimental investigation of a naval propulsion drive model with the PWM-based attenuation of the acoustic and electromagnetic noise," *IEEE Trans. Ind. Electron.*, vol. 53, no. 2, pp. 450–457, Apr. 2006.

[26] K. T. Chau and Z. Wang, *Chaos in Electric Drive Systems—Analysis, Control and Application*. New York, NY, USA: Wiley, 2011.

[27] H. Li, Z. Li, B. Zhang, F. Wang, and W. Halang, "Design of analogue chaotic PWM for EMI suppression," *IEEE Trans. Electromagn. Compat.*, vol. 52, no. 4, pp. 1001–1007, Nov. 2010.

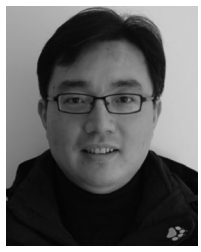
[28] Z. Wang, K. T. Chau, and C. Liu, "Improvement of electromagnetic compatibility of motor drives using chaotic PWM," *IEEE Trans. Magn.*, vol. 45, no. 6, pp. 2612–2614, Jun. 2007.

[29] Z. Zhang, K. T. Chau, C. Liu, C. Qiu, and F. Lin, "An efficient wireless power transfer with security considerations for electric vehicle applications," *J. Appl. Phys.*, vol. 115, no. 17, pp. 17A328–1–17A328-3, 2014.

[30] G. S. Buja, and M. P. Kazmierkowski, "Direct torque control of PWM inverter-fed ac motors—A survey," *IEEE Trans. Ind. Electron.*, vol. 51, no. 4, pp. 744–757, Aug. 2004.

[31] A. Steimel, "Direct self-control and synchronous pulse techniques for high-power traction inverters in comparison," *IEEE Trans. Ind. Electron.*, vol. 51, no. 4, pp. 810–820, Aug. 2004.

[32] S.K.T. Miller, T. Beechner, and J. Sun, "A comprehensive study of harmonic cancellation effects in interleaved three-phase VSCs," in *Proc. Power Electron. Spec. Conf.*, 2007, pp. 29–35.



Zheng Wang (S'05–M'09–SM'14) received the B.Eng. and M.Eng. degrees from Southeast University, Nanjing, China, in 2000 and 2003, respectively, and the Ph.D. degree from The University of Hong Kong, Hong Kong, in 2008.

From 2008 to 2009, he was a Postdoctoral Fellow in Ryerson University, Toronto, ON, Canada. He is currently an Associate Professor at the School of Electrical Engineering, Southeast University. He has authored or coauthored more than 70 internationally refereed papers and four books in these areas. His research interests include electric drives, power electronics, and distributed generation.

Dr. Wang received several academic awards including the IEEE PES Chapter Outstanding Engineer Award, the Best Paper Award of International Conference on Electrical Machines and Systems, the Best Session Paper Award of the IEEE Annual Meeting of Industrial Electronics, and the Nanjing Outstanding Paper Award of Natural Science.

Jian Chen received the B.Eng. degree from the Anhui University of Science and Technology, Huainan, China, in 2013. He is currently working toward the M.Eng. degree at Southeast University, Nanjing, China.

His research interests include multilevel converter, multilevel PWM strategy, control of multiphase permanent magnet synchronous motor, and fault tolerant control of multiphase motor.

Ming Cheng (M'01–SM'02–F'15) received the B.Sc. and M.Sc. degrees from the Department of Electrical Engineering, Southeast University, Nanjing, China, in 1982 and 1987, respectively, and the Ph.D. degree from the Department of Electrical and Electronic Engineering, The University of Hong Kong, Hong Kong, in 2001.

Since 1987, he has been with Southeast University, where he is currently a Professor at the School of Electrical Engineering and the Director of the Research Center for Wind Power Generation. From January to April 2011, he was a Visiting Professor with the Wisconsin Electric Machine and Power Electronics Consortium, University of Wisconsin, Madison. He has authored or coauthored more than 300 technical papers and four books and is the holder of 55 patents in these areas. His teaching and research interests include electrical machines, motor drives for electric vehicles, and renewable energy generation.

Prof. Cheng is a Fellow of the Institution of Engineering and Technology. He has served as the Chair and an Organizing Committee Member for many international conferences. He is a Distinguished Lecturer of the IEEE Industry Applications Society for 2015/2016.

K. T. Chau (M'89–SM'04–F'13) received the B.Sc. (Eng.), M.Phil., and Ph.D. degrees in electrical and electronic engineering from The University of Hong Kong, Hong Kong, in 1988, 1991, and 1993, respectively.

Since 1995, he has been with The University of Hong Kong, where he is currently a Professor with the Department of Electrical and Electronic Engineering and the Director of the International Research Center for Electric Vehicles. He is the author of four books and more than 400 refereed technical papers. His research interests include electric and hybrid vehicles, power electronics and drives, and renewable energy systems.

Dr. Chau is a Fellow of the Institution of Engineering and Technology and of the Hong Kong Institution of Engineers. He currently serves as a Coeditor of the *Journal of Asian Electric Vehicles*. He is a Chartered Engineer. He received the Changjiang Chair Professorship from the Ministry of Education, China, and the Environmental Excellence in Transportation Award for Education, Training, and Public Awareness from the Society for Automotive Engineers International.