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Passive islanding detection using inverter nonlinear effects

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***Abstract*— This paper analyzes the use of the voltage distortions in PWM voltage-source-inverters (VSIs) caused by the inverter switching for islanding detection purposes. The non-ideal characteristics of the inverters, mainly due to the dead-time needed to have safe commutations, produces fundamental frequency dependent harmonics (-5th, 7th …) in the output voltage. These harmonics are in principle an unwanted effect as they reduce the power quality. However, they can potentially be used for islanding detection purposes. The physical principles of the method would be the same as for high frequency signal injection methods that have already been proposed, but without the need of injecting a high frequency signal, behaving therefore as a passive islanding detection technique.**

Index Terms— distributed generation, grid impedance estimation, dead-time, passive islanding detection, power system monitoring.

I. Introduction

Distributed Power Generation (DPG) architectures are a useful mechanism to decrease the transmission losses as well as emissions. Generally speaking, DPG units can be based on renewable and non-renewable energy resources. One of the most versatile ways to introduce the DPG into the electrical network is throughout the use of microgrids [1], which can be understood as small-scale versions of the classical large centralized electric distribution system.

The connection of microgrids and/or distributed energy resources into the utility grid is regulated by local, regional and national authorities, while standardizing institutions (e.g. IEEE or IEC) publish standards and recommendations for connecting distributed energy resources into electric power systems [2-9]. In every case, the system must have the ability to detect if the DPG unit is connected or disconnected from the utility grid: this is normally referred as islanding detection [10-18]. IEEE-1547 [2], UL-1741 [3], IEC-62116 [4], AS-4777 [5] and IEEE-929 [6] are examples of islanding standards.

Islanding detection methods can be classified into three major groups: passive [10, 11], communication-based [12] and active methods [10-18, 33 and 35-38]. Passive islanding detection techniques detect changes in a grid variable (such as magnitude, frequency or phase of the PCC voltage). These methods are grid friendly, as they do not produce any disturbance in the grid. However, they usually have a large non-detection zone (NDZ), especially when the power mismatch between the power generated by the DPG unit and the power imported from the grid is relatively small. Communication-based methods exchange some information between the grid and the DPGs, requiring therefore a communication infrastructure, which results in additional investments. These methods do not have a NDZ unless the communication channel is unavailable [12]. Finally, active islanding detection methods inject a disturbing signal into the grid, the islanding condition being detected by the system response to such a signal [10-13]. These methods present a low NDZ [10-13], but they have a negative impact on the grid power quality. In addition, the implementation of active methods in a multi-inverter scenario can be problematic due to the interference that can occur between inverters. Strategies to prevent this from happening have been proposed [12, 13].

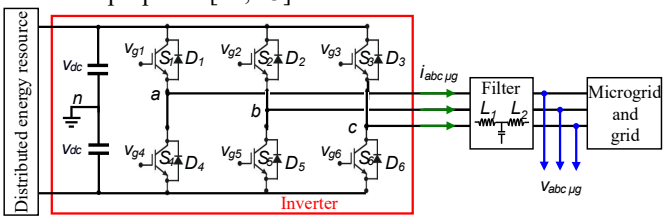

Fig. 1.- Simplified distributed energy resource connection to the utility grid/microgrid using a VSI.

It is possible to use voltage harmonics that are naturally produced during the normal operation of electronic power converters for islanding detection purposes. Distributed energy resources are usually connected to the main grid/microgrid by means of a three-phase PWM-VSI [12-13] (see Fig. 1). VSIs produce a distortion of the output voltage with respect to the commanded voltage, mainly due to the blanking time (dead-time) needed for safe commutation of the inverter legs [19-24], the turn-on and turn-off times, as well as the voltage drop across the diodes and power switches. Among the aforementioned effects, the dead-time is normally the most relevant. The resulting output voltage distortion in this case is known to depend on the inverter current polarity [22-23], with the -5th, 7th… harmonics of the fundamental frequency appearing in the voltage frequency spectrum [19, 21]. Note that the inverter is connected to the grid via an LCL filter which acts to reduce switching frequency related harmonics entering the grid: it usually has a corner frequency higher than the frequency of the harmonics considered here, but will have a small attenuating influence on them.

This paper proposes a new passive islanding detection technique that uses the inverter's non-ideal behavior to estimate the grid high frequency impedance. Since no test signal needs to be injected, there is no adverse impact on the power quality (THD), which is a drawback of active islanding detection

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methods [12-13, 10-18, 35-38]. On the other hand, the method shares the reduced NDZ of active islanding detection methods. Consequently, it combines advantages of both active and passive islanding detection methods.

The paper is organized as follows: the analysis of the effects due to the dead-time in PWM inverters is presented in section II; the principles of the proposed islanding detection method are presented in section III. Section IV contains some implementation issues that must be carefully taken into account while simulation and experimental results to confirm the viability of the proposed method are finally provided in sections V, VI and VII.

II. Dead-time effects in PWM inverters

Fig. 1 schematically shows the typical scheme of a three-phase PWM-VSI used to connect distributed energy resources to the three-phase utility grid/microgrid. Fig. 2 shows the gate signals for one leg without (subplots a) to c)) and with (subplots d) to g)) the dead-time.

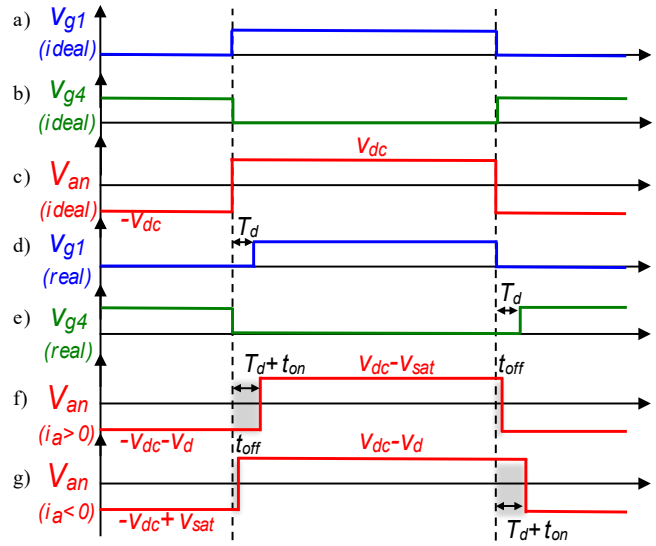

Fig. 2.- a) to c): gate signals for switches S1, a), and S4, c), and output voltage when no dead time is considered. d) to g): gate signals for switches S1, d), and S4, e), when the dead-time is inserted. Output voltage when the output current is positive, f) and negative g).

Fig. 2a and 2b show the ideal gate signals for switches 1 and 4, while Fig. 2c shows the ideal output voltage, i.e. when no voltage drop exists across the switches and the on-off transitions of the upper and lower switches occurring simultaneously. In practice, due to the non-zero turn-on and turn-off times, a dead-time has to be inserted into every commutation to guarantee that the two switches in a branch (e.g. S1 and S4) do not conduct simultaneously. Fig. 2d and 2e show the real gate signals, after inserting the dead-time, when switches S1 and S4 are turned-on and off respectively. When both transistors are turned-off, one of the freewheeling diodes will conduct, depending on the polarity of the output current. If the current is positive (see Fig. 1), D4 will be conducting (see Fig. 2f), the output voltage being connected to the negative pole of the DC bus. If the current is negative, D1 will conduct and the output voltage will be connected to the positive pole of the of the DC bus. The voltage drops across the switches and diodes as well as the turn-on/off times are also schematically shown in Fig. 2f and 2g.

The average voltage errors caused by the non-ideal behavior of the inverter (turn-on, turn-off, voltage drops and dead-time) during each switching period can be understood from (1) and (2) for the case of the current being positive and negative respectively (see Fig. 2f and g), where T_d is the dead-time, t_{on} is the turn-on time of the power switch, t_{off} is the turn-off time of the power switch, T_s is the sampling period, V_{dc} is the dc bus voltage, V_d is forward voltage drop of the diode and V_{sat} is the on-state voltage drop across the power switch. Assuming that $V_d \approx V_{sat}$ (1) and (2) can be simplified to (3) and (4) [22].

Fig. 3a shows the current for phase *a,* while Fig. 3b shows the average voltage error over each switching cycle. The average voltage corresponds to a square wave, which can be expressed using a Fourier series as (5). Taking into account the $2\pi/3$ phase shift between phases in a balanced three-phase system, the average voltage errors for phases *b* and *c* can be expressed as (6) and (7), with *n* being the harmonic order.

$$\Delta V = \frac{T_d + t_{on}}{2T_s}\left(-V_{dc} - V_d\right) + \frac{t_{off}}{2T_s}\left(V_{dc} - V_{sat}\right) = \\ = \frac{-T_d - t_{on} + t_{off}}{2T_s}V_{dc} + \frac{-T_d - t_{on}}{2T_s}V_d + \frac{-t_{off}}{2T_s}V_{sat} \quad (1)$$

$$\Delta V = \frac{T_d + t_{on}}{2T_s}\left(V_{dc} + V_d\right) + \frac{t_{off}}{2T_s}\left(-V_{dc} + V_{sat}\right) = \\ = \frac{T_d + t_{on} - t_{off}}{2T_s}V_{dc} + \frac{T_d + t_{on}}{2T_s}V_d + \frac{t_{off}}{2T_s}V_{sat} \quad (2)$$

$$\Delta V = \frac{-T_d - t_{on} + t_{off}}{2T_s}V_{dc} - \frac{T_d + t_{on} + t_{off}}{2T_s}V_{sat} \quad (3)$$

$$\Delta V = \frac{T_d + t_{on} - t_{off}}{2T_s}V_{dc} + \frac{T_d + t_{on} + t_{off}}{2T_s}V_{sat} \quad (4)$$

$$V_{an} = \frac{4\Delta V}{\pi}\sum_{n=1,5,7\ldots}\frac{1}{n}\sin\left(n\omega t\right) \quad (5)$$

$$V_{bn} = \frac{4\Delta V}{\pi}\sum_{n=1,5,7\ldots}\frac{1}{n}\sin\left[n\left(\omega t - \frac{2\pi}{3}\right)\right] \quad (6)$$

$$V_{cn} = \frac{4\Delta V}{\pi}\sum_{n=1,5,7\ldots}\frac{1}{n}\sin\left[n\left(\omega t - \frac{4\pi}{3}\right)\right] \quad (7)$$

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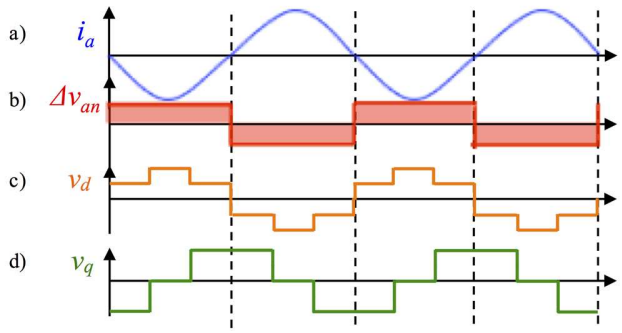

Fig. 3.- Phase current, a), average voltage error, b), d and q components of the average voltage complex vector, c) and d).

Using the transformation from a generic set of three-phase quantities (*fa, fb, fc*) to *dq* quantities (8), the resulting voltage vector due to the non-ideal behavior of the inverter (8) is obtained, the corresponding *d- and q-axis* components being shown in Fig. 3c and 3d respectively. Voltage and current complex vectors in the following equations and figures are referred to the stationary reference frame. It is noted however that other reference frames could be used in practice for the implementation of the control and signal processing algorithms described in this paper.

$$v_{dq} = \sum_{n=1,-5,7...} V_n e^{j(n\omega_0 t+\theta)} \tag{8}$$

$$f^s_{dq} = f_d + jf_q = \frac{2}{3}\left(f_a + f_b e^{j2\pi/3} + f_c e^{j4\pi/3}\right) \tag{9}$$

$$V_n = \frac{2*\Delta V}{n\pi}\left[-2\cos(n\pi) - \cos(n2\pi/3) + \cos(n\pi/3)\right] \tag{10}$$

where $\theta = \pi$ when n<0 and $\theta = -\pi$ when n>0, ω_0 is the grid/microgrid frequency and the magnitude of the harmonic voltage V_n is given by (10).

It is concluded from (5)-(8) that the inverter non-ideal behavior produces harmonics having orders of -5, 7…, with the corresponding harmonic magnitude being inversely proportional to the harmonic order, (10) [27] (see Fig. 4).

Fig. 5 and 6 show the experimentally measured frequency spectrum of the output voltage and current of a VSI, both for the case of island and grid connected operation (the experimental setup is shown in Fig. 16, its parameters being shown in Table III). An LCL filter was used to connect the VSI to the grid. The current for the case of island operation corresponds therefore to the current absorbed by the LCL filter. Harmonics of order -5th and 7th are readily observed in the voltage and current spectrums, their magnitudes being inversely proportional to the harmonic order. It can also be seen that harmonics induced in the resulting current vector due to the non-ideal behavior of the inverter are noticeably higher in the grid-connected case compared to the island case. This is due to the lower output impedance for the case of grid-connected mode. It is also noted that the resulting higher order harmonics at the output voltage of the LCL filter are smaller for grid-connected case with respect to the island case. This is due to the increased voltage drop across the filter due to the larger harmonic currents.

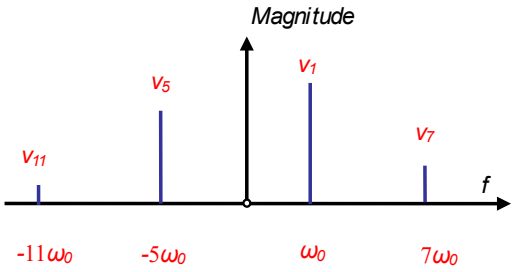

Fig. 4.- Schematic representation of the complex vector spectrum of the output voltage vector showing the harmonics due to the non-ideal behavior of the inverter, v_{dq}.

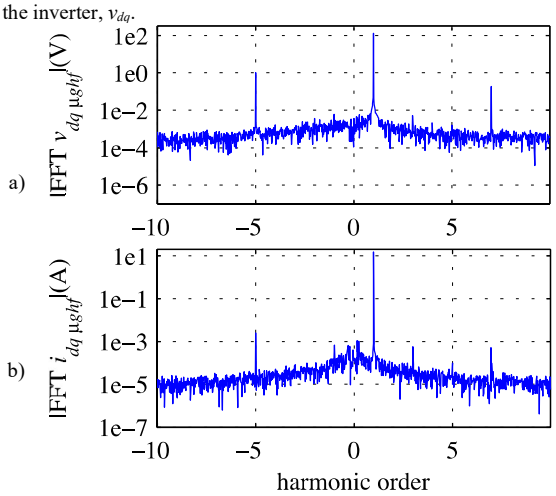

Fig. 5.- a) Voltage complex vector ($v_{dq\mu g}$) and b) current complex vector ($i_{dq\mu g}$) spectrums in island mode. The fundamental frequency is 50 Hz, with a dead-time of 3µs and a switching frequency of 10kHz.

III. ISLANDING DETECTION USING HARMONICS DUE TO THE INVERTER SWITCHING

The harmonics due to non-ideal behavior of the VSI (8), can be modeled as (11). Every harmonic in the output voltage (v_{dqn} , Fig. 7) will produce a harmonic in the inverter current at the same frequency (i_{dqn} , Fig. 7). The resulting harmonic component at the output of the LCL filter (12), can be obtained by applying Kirchhoff's voltage law to the output LCL filter as shown in Fig. 7.

$$v_{dqn\omega_0} = V_n e^{jn\omega_0 t} \tag{11}$$

$$i_{dq\mu gn\omega_0} = \frac{v_{dqn\omega_0} - v_{dq\mu gn\omega_0} - jn\omega_0 L_1 i_{dqn\omega_0}}{jn\omega_0 L_2} \tag{12}$$

$$Z_{dq\mu gn\omega_0} = \frac{v_{dq\mu gn\omega_0}}{i_{dq\mu gn\omega_0}} \tag{13}$$

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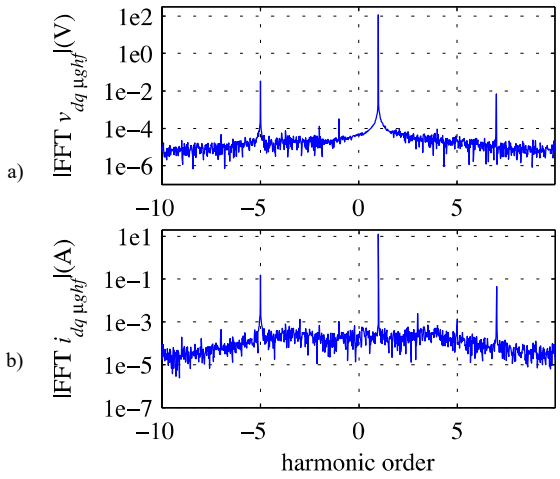

Fig. 6.- a) Voltage complex vector ($v_{dq\mu g}$) and b) current complex vector ($i_{dq\mu g}$) spectrums in grid-connected mode. . The operating conditions are the same as in Fig. 5.

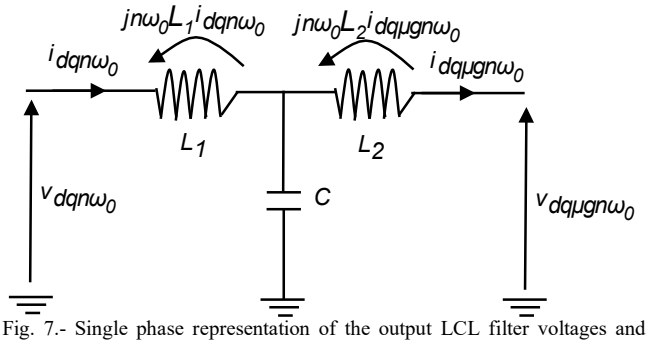

Fig. 7.- Single phase representation of the output LCL filter voltages and currents.

where $v_{dq\mu gn}$ is the magnitude of the resulting voltage harmonic at the filter output (see Fig. 7), L_1 is the inverter side inductance and L_2 is the grid/microgrid side inductance. The high frequency impedance (13) is obtained from the voltage and current harmonics due to the non-ideal behavior of the inverter. Variations of the high frequency impedance will be used to detect islanding [12, 13, 33, 36].

In principle, any of the high order harmonics due to the non-ideal behavior of the inverter could be potentially used for islanding detection purposes. However lower order harmonics will provide a larger signal-to-noise ratio, improving the accuracy of the method. This is due both to the decrease of the harmonic voltage magnitude with the harmonic order (10), as well as to the increase of the impedance with the harmonic order due to its inductive nature. The maximum harmonic order might also be limited by the interaction between the injected harmonics, the LCL filter resonance frequency and the grid resonance frequency [12]. It is concluded that the -5th and the 7th harmonics are the preferred candidates for the implementation of the method.

In the following subsections, two different strategies for the implementation of the proposed methods are discussed, namely *open-loop mode* and *current cancellation mode*.

A. *Open-loop mode*

In this mode of operation, no mechanism is implemented to compensate the effects due to the non-ideal behavior of the inverter. The harmonics in the inverter output voltage (v_{dqn} in Fig. 7 and (11)) and current (i_{dqn} in Fig. 7 and (12)) are used to estimate the high frequency impedance (13). Islanding is detected from the changes in the high frequency impedance magnitude and phase.

Fig. 8 shows the block diagram of the signal processing used for islanding detection using this mode of operation, including the current control of the inverter as well as the filtering. A voltage control loop and higher-level control functionalities are not included in the diagram since they do not interfere with the proposed islanding detection method. Two band-pass filters (BPF1 and BPF2, see Fig. 8), tuned at the frequency of the harmonic used for islanding detection, are used to isolate the corresponding voltage and current harmonic components. It is finally noted from Fig. 8 that no explicit high frequency signal injection exists, contrary to active islanding detection methods reported in [12] and [39].

Since the proposed method is based on the high frequency impedance variation between island and grid-connected operating modes, a NDZ can occur when the difference between the microgrid and the grid high frequency impedance is small (e.g. below the limits established by the standards [7-9]) or the voltage difference between the inverter output and the PCC. It is noted however that these limitations are shared by all islanding detection methods based on the measurement of impedance variation. It is also noted that since the method is based on the microgrid/grid high frequency impedance variation, it will be sensitive to the length/impedance of the line between the inverter and the point of common coupling (PCC). An analysis of this issue, including remedial measurements, has already been presented in [33].

Finally, although the proposed method must be considered as passive, since no disturbing signal is being injected, its NDZ matches with that of active methods [10-18, 33 and 36]. The NDZ in passive methods is typically defined as a region of active and reactive fundamental power mismatch where the islanding condition cannot be detected [11], however this definition cannot be applied in this case, as the proposed method is not based on a power mismatch but on the high frequency impedance variation.

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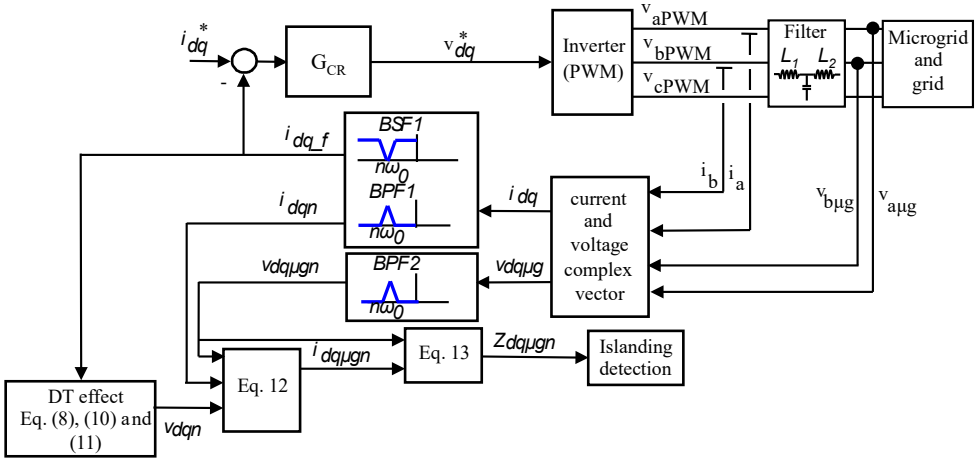

Fig. 8.- Signal processing for islanding detection using the high frequency impedance variation using an open-loop implementation.

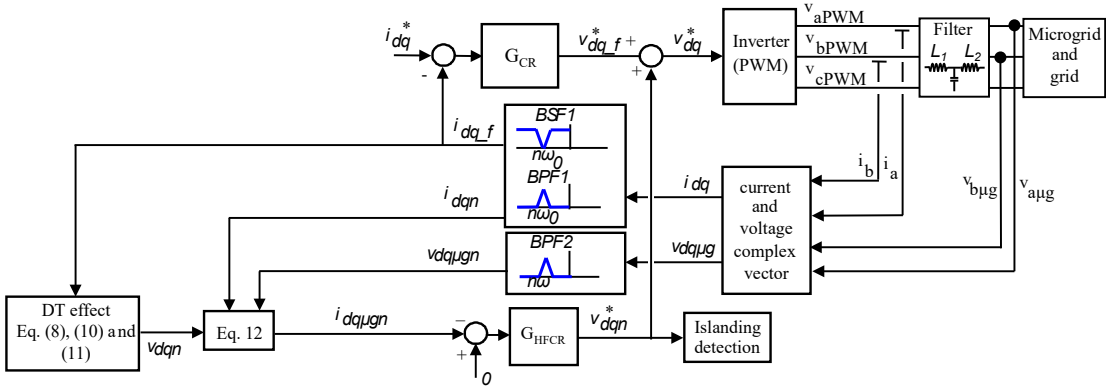

Fig. 9.- Signal processing for islanding detection for the current cancellation mode.

B. *Current cancellation mode*

An alternative implementation of the method named *Current cancellation mode* is shown in Fig. 9. In this strategy, a PI regulator (G_{HFCR} in Fig. 9) in a reference frame synchronous with the harmonic used for islanding detection, $n\omega_0$, is used to eliminate the harmonic from the inverter output current. The output of the harmonic current regulator (v^*_{dqn} in Fig. 9) corresponds to the harmonic voltage needed to cancel the harmonic current. The magnitude of this voltage can be used for islanding detection purposes [13]. As for the *open-loop mode*, the voltage control loop and higher-level control functionalities are not shown in Fig. 9, as they do not affect to the implementation of the method.

The threshold for islanding detection, both for open-loop and current-cancellation modes is highly influenced by the microgrid structure and parameters (LCL filters, transition lines, loads, inverters, nonlinear loads (NLLs)). There is therefore no limit for the number of potential configurations. It is noted that the same problem exists for all islanding detection methods based on the injection of a harmonic/high frequency signal. This issue has been not investigated in the literature by analytical procedures, being the object of ongoing research.

IV. Implementation Issues

There are five aspects that can be especially relevant for the implementation of the proposed method: 1) dead-time used in the inverter; 2) the risk of interference with non-linear-loads (NLLs); 3) grid voltage harmonics; 4) the effects of dead-time compensation strategies and 5) interference among inverters operating nearby. All these issues are discussed in this section.

A. *Dead-time used in the inverter*

The proposed method uses the variations of the high frequency impedance to detect changes between grid-connected and island modes. Consequently, its operation should be independent in principle, of the dead time used in the VSI. However, this is not totally true in practice. The selection of the dead-time will affect to the signal-to-noise ratio: the larger the dead-time is, the larger will be the magnitude of the induced voltage distortion and consequently the resulting harmonic currents, therefore improving the signal-to-noise ratio of the estimated impedance. For the case of small values of the dead-time, a low-pass filter can be used to eliminate noise from the estimated high frequency impedance.

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Fig. 10 shows the estimated high frequency impedance for values of the dead-time ranging from 3μs to 6μs respectively, which correspond to the minimum and maximum values that can be used in the experimental setup respectively (the details can be found in Table I and Fig. 11). As expected, the estimated high frequency impedance (magnitude and phase) is less oscillatory for the case of the larger dead-time. Since lower dead-times would be preferred from a power quality perspective, there is a compromise which is required in practice.

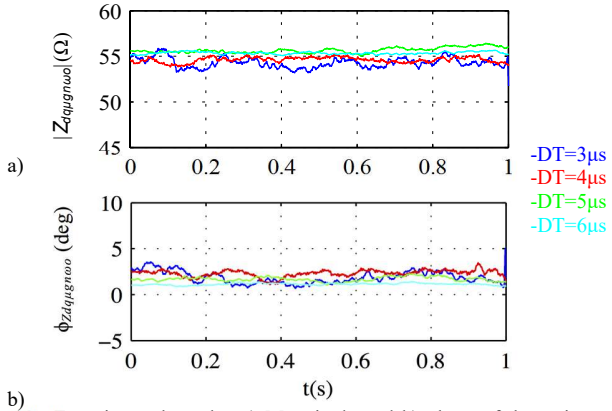

Fig. 10.- Experimental results. a) Magnitude and b) phase of the estimated high frequency impedance for different values of the dead-times.

B. *Risk of interference with NLLs*

Non-linear loads (NLLs) can potentially interfere with the proposed method, as they can produce harmonics at frequencies that coincide with those due to the non-ideal behavior of the inverter. The performance of the method in this case can strongly depend on the microgrid structure. To the best of authors' knowledge, detailed analysis of this issue has not been reported in the literature. Although its detailed analysis is beyond the scope of this paper, discussion of the key concepts involved are briefly presented following.

There are two major issues that will influence the performance of high frequency signal injection based islanding detection methods in the presence of NLLs:

- Frequency selection: it can coincide with a characteristic harmonic components of the fundamental frequency (-5, 7, 11, 13… i.e. those produced by non-linear loads) or not; the method proposed in this paper uses a characteristic frequency, as the harmonics due to the dead-time in the inverter are of these type.
- Presence of APFs in the microgrid implementing harmonic current compensation. It is noted that the presence of APFs implies a multi-inverter scenario.

Use of characteristic harmonics is expected to provide excellent performance when APFs operate in the microgrid. Since the APF supplies the harmonic current consumed by NLLs, the NLL will become *invisible* to the harmonics induced by the nonlinear behavior of the inverter (no current will flow from the inverter to the NLL), the inverter *seeing* an infinite impedance at its output. However, when the inverter is grid connected and the APF continues supplying the harmonic current consumed by the NLLs, the high frequency impedance that the inverter *sees* at its output will decrease due to the reduced grid impedance magnitude. Therefore, the method proposed in this paper is advantageous in this case as it uses characteristics harmonics. On the contrary, use of non-characteristic harmonics would be highly inadvisable when APF operate in the microgrid, as the reaction of the APF to such harmonics is highly unpredictable, depending on the frequency being used and the configuration of the APF. Both characteristic and non-characteristic harmonics can potentially provide similar performance when APFs are not used in the microgrid.

C. *Effects of grid voltage harmonics*

The presence of harmonic components in the grid voltage could decrease the method accuracy, eventually driving the method into the NDZ or even erroneously detecting the islanding condition. Nevertheless, this is not a particular limitation of this method, it is shared by all active islanding techniques based on the injection of a harmonic/high frequency signal.

The advantage of the proposed technique is that any of the high order harmonics due to the non-ideal behavior of the inverter could be potentially used for islanding detection purposes (i.e. not only -5th harmonic component). Therefore, harmonic component which are not expected to be present could be used instead of the -5th.

D. *Effects of dead-time compensation techniques*

Inverters commonly implement dead-time compensation techniques [20-26, 40-48]. The reliability of the proposed technique could be compromised in inverters implementing these techniques. The reliability of the proposed islanding detection technique has been evaluated for the dead-time compensation strategy presented in [40].

Fig. 11 shows the simulation results for the compensation technique presented in [40]. Fig. 11a) shows the magnitude of the current harmonics (-5th to 13th), $i_{dq\ gn}$ (11). while Fig. 11b shows the magnitude of the voltage harmonics at the filter output ($v_{dq\ \mu gn}$, see Fig. 7). The dead-time compensation strategy is activated at t=0.25s, the inverter is connected to the grid at t=0.5s and disconnected from the grid at t=1.5s. It is observed from Fig. 11a that the compensation technique compensates the current harmonics ≈100ms after the strategy is being activated. Finally, Fig. 11c shows the magnitude of the high frequency impedance (13) for the harmonic components shown in Figs. 11a and b. It is observed that islanding condition can be reliable detected even in inverters implementing dead-time compensation techniques.

It is finally noted that dead-time compensation techniques typically do not compensate for all harmonic components due to the non-ideal behavior of the inverter [40, 42-48]. Although in the paper it is proposed to use the -5th harmonic component, in principle, any of the high order harmonics due to the non-ideal

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behavior of the inverter that is not being compensated by the compensation technique could be used for islanding detection purposes. Therefore, as verified in simulation results, the method applicability is not compromised by the implementation of dead-time compensation techniques.

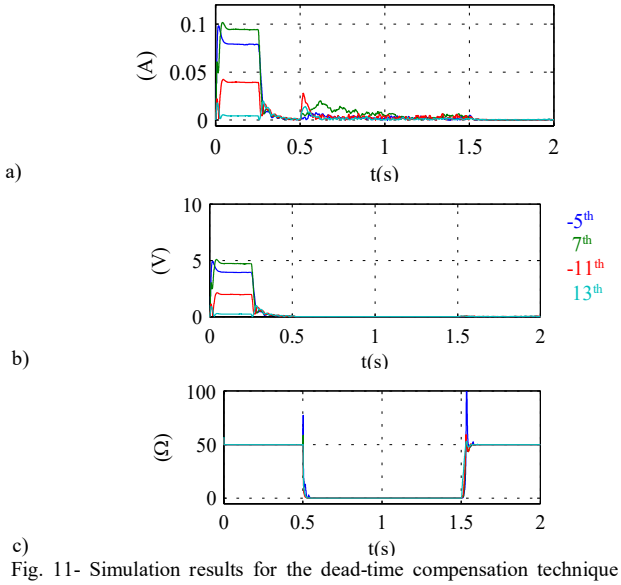


Fig. 11- Simulation results for the dead-time compensation technique shown in [40]. a) Magnitude of the -5th 7th, -11th and 13th current harmonics. b) Magnitude of the -5th 7th, -11th and 13th voltage harmonics c) Magnitude of the estimated high frequency impedance for the -5th, 7th, -11th and 13th harmonic components. Dead-time=5μs.

E. *Interference among inverters operating nearby*

When multiple inverters using high frequency signal for islanding detection operate nearby, synchronization of the high frequency signal for all the inverters is highly advisable [33]. Otherwise, the circulating currents among the inverters due to differential high frequency voltages can produce an unwanted interference among inverters. Since the effect of the dead-time is related to the zero crossing of the current, inverters operating with the same power angle will be self-synchronized. This would be the case when all the inverters operate with a unit power factor. If the power factor is different for inverters located nearby (e.g. if the inverters are commanded to compensate reactive power), then a differential high frequency voltage among inverters could occur. This would produce the circulation of high frequency currents among inverters, therefore reducing the accuracy estimating the high frequency impedance. Strategies to prevent from this to happen have already been analyzed in [13, 33], they are not therefore discussed in detail in this work. The strategy proposed in [13] can be adopted in this case, where one of the inverters would work in an "*open loop mode"* and the remaining inverters would work in a *"Current cancellation mode"*. Inverters using the combined "*Open loop mode"* and *"Current cancellation mode"* can be directly connected in parallel.

V. Simulation Results under IEEE-1547 Islanding Detection Test Conditions

The proposed strategy has been evaluated in a single inverter scenario using the IEEE-1547 islanding detection test conditions. The simulation scenario is shown in Fig. 12, the simulation parameters being given in Table I.

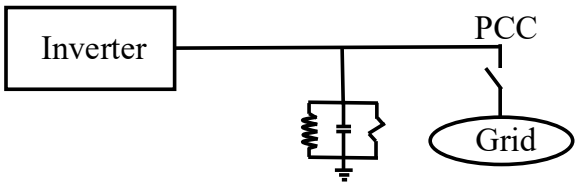


Fig. 12.- Simulation scenario for IEEE-1547 islanding detection test conditions.

Table I. Simulation parameters: single inverter operation.

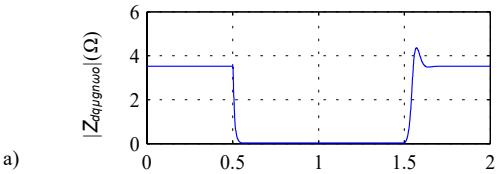
Grid	380 V, 50 Hz, S_{cc}=15 MVA
Inverter	380 V, 10 kHz.
RLC Load	R=43Ω , L= 136.9 mH C= 74 μF
RLC Load Quality factor [2]	1
Simulation step	1e-7 s
Dead-time	5μs
BPF1, BPF2 and *BSF1* bandwidth	25Hz
G_{CR}	K_p =10; K_i=95
G_{HFCR}	K_p=15; K_i =200
LCL filter resonance frequency	575 Hz

Fig. 13a and b show the magnitude and phase of the estimated high frequency impedance in a transition from island to grid connected (t=0.5s) and from grid connected to island (t=1.5s), using the *open-loop* mode (see Fig. 8). The -5th harmonic was used for the impedance estimation.

It is observed from Fig. 13 that both the magnitude and phase of the high frequency impedance could be potentially used for islanding detection. The change of the high frequency impedance is detected in a few *ms*, widely meeting the islanding detection requirements (e.g. 1 Ohm in 2 seconds for the German standard [7] and 0.5 Ohms in 5 seconds for the Swiss and Australian standards [8, 9]).

Fig. 14 shows the harmonic current regulator output voltage when the *current cancellation mode* shown in Fig 9 is used, for the same transition as in Fig. 13. Also in this case the change of the current regulator output voltage takes a few *ms*, therefore meeting the islanding detection standards [2-9].

To illustrate the differences between the *current cancellation* mode vs. the *open loop* mode, Fig. 15 shows the magnitude of the -5th, 7th, -11th and 13th harmonics of the current vector in both cases. The current cancellation mode is seen to significantly reduce the -5th harmonic of the current, therefore improving the THD.



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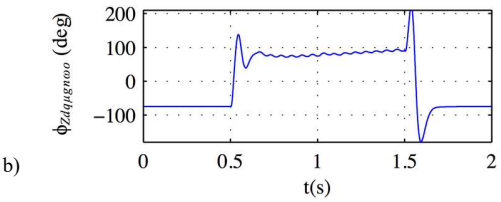


Fig. 13.- a) Magnitude and b) phase of the estimated high frequency impedance.

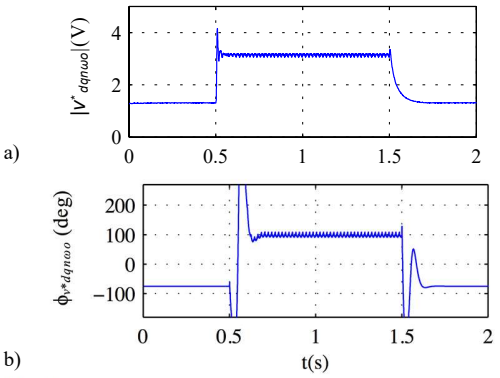


Fig. 14.- a) Magnitude and b) phase of the harmonic current regulator output voltage.

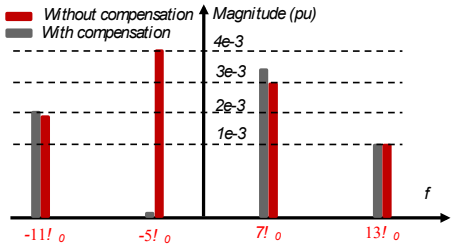


Fig. 15.- Harmonics of the current vector with and without compensation of the 5th harmonic implemented.

VI. Simulation Results for Parallel Inverter Operation

The proposed method has been evaluated for the multi-inverter scenario as shown in Fig. 16. The simulation parameters are shown in Table II. No load sharing strategy was implemented for the converters while the -5th harmonic was used for the impedance estimation.

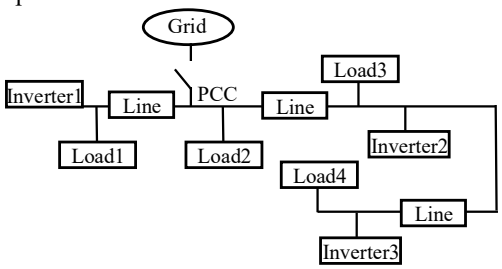


Fig. 16.- Multi-inverter simulation scenario.

Table II. Simulation parameters: parallel inverter operation.	
Grid	380V, 50Hz, Scc=15MVA
Inverter 1, 2 and 3	380V, 10kHz.
Load1,2,3 and 4	10kW
Line	11.7mOhm, 8.68e-4H
Simulation step	1e-7 s
Dead-time	5μs
BPF1, BPF2 and *BSF1* bandwidth	25Hz
G_{CR}	K_p=10; K_i=95
G_{HFCR}	K_p=15; K_i =200
LCL filter resonance frequency	575 Hz

Fig. 17a and 17b show the magnitude and phase of the estimated high frequency impedance in a transition from island to grid-connected (t=0.5s) and from grid-connected to island (t=1.5s) with the inverter operating in an *open-loop mode*, the high frequency impedance being used for islanding detection (see Fig. 8). Minor differences observed in Fig. 17a and 17b among inverters 1, 2 and 3 are due to the differences in the corresponding line impedances. It is observed however that in all the cases the transition between grid connected and island modes are readily observable.

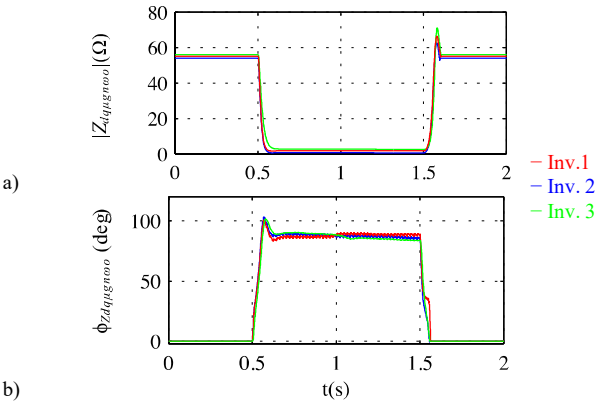
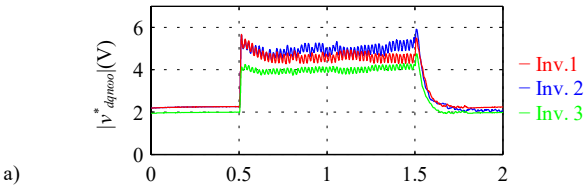


Fig. 17.- Simulation results when the inverters operated in the *open-loop mode*. a) magnitude and b) phase.

Fig. 18a and 18b show the response of the method using the *current cancellation mode*. Changes of the harmonic current regulator output voltage (see Fig. 9) reliably reflect the changes between the grid-connected and island modes.



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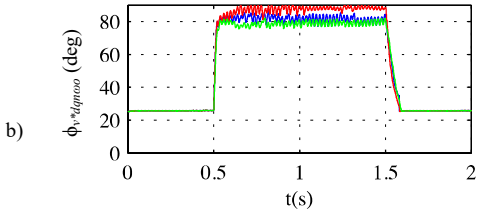


Fig. 18.- Simulation results when the inverters operated in the *Current cancellation mode*. a) Harmonic current regulator output voltage and b) phase.

VII. Experimental Results

Experimental results showing the performance of the proposed method are presented in this section. Only results for the multi inverter scenario will be provided, as this case is significantly more challenging compared to the single-inverter case. Fig. 19 shows the experimental setup, the main parameters being shown in Table III. The three-phase inverters use *Mitsubishi Electric* 1200V, 75A *IGBT* modules. The dead-time was set to 3µs, which is the minimum value allowed by the power modules. The switching frequency was set to10 kHz. The -5th harmonic was used for the impedance estimation.

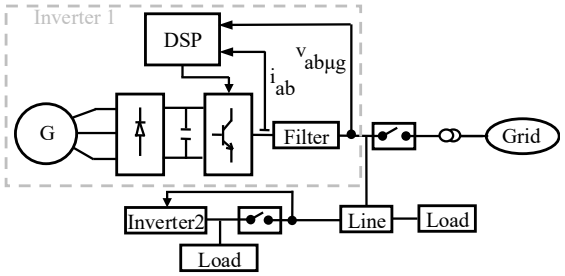


Fig. 19.- Experimental setup with two parallel-connected inverters.

Table III. Experimental setup parameters: parallel inverter operation.	
Grid ratings	380 V, 50 Hz, S_{cc}=2 MVA
Grid harmonic content	5th=0.195%, 7th=0.087%, 11th=0.033%.
Generator	380V, 10kHz, 100kVA.
Inverter 1 and 2 ratings	380V, 10 kHz, 30kVA.
Inverter 1 LCL filter parameters	L=2.4mH, C=30uF
Inverter 2 LCL filter parameters	L=1.56mH, C=30uF
Load 1 and 2	30 kW
Dead-time	3µs
BPF1, BPF2 and *BSF1* bandwidth	10Hz
G_{HFCR}	K_p=12.6; K_i=71.5
G_{CR}	K_p=8.4; K_i=60

Fig. 20 shows the estimated high frequency impedance magnitude and phase using the implementation shown in Fig. 8 (*open-loop mode*), during a transition from island to grid-connected (t=1s) and from grid connected to island (t=4s). The estimated high frequency impedance is available in ≈100ms: this was considered fast enough for island detection (according to [2]-[6]). The experimental results were repeated for many scenarios and in each case an identifiable change in impedance indicating a grid-island transition was identified, shown that the technique was repeatable and potentially reliable. The differences between the high frequency impedance *seen* by the inverters are related to the different LCL filters, the transmission lines and the loads connected to the PCC (Fig. 16).

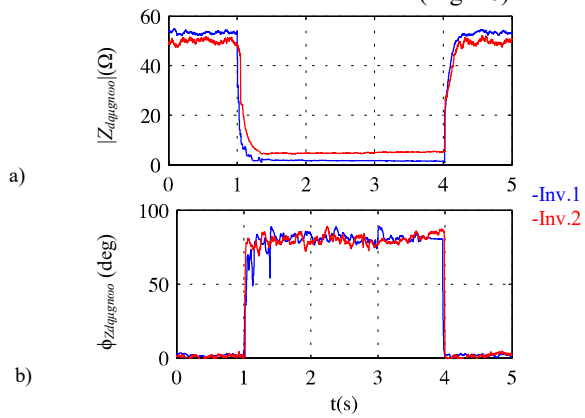
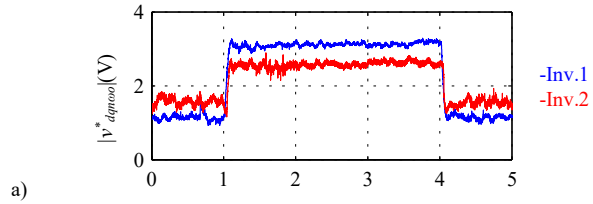


Fig. 20.- Experimental results when the inverters operate in the *open-loop mode*. a) magnitude and b) phase. Dead-time=3µs.

Fig. 21 shows the harmonic current regulator output voltage using the *current cancellation mode* (see Fig. 9) for the same transition shown in Fig. 20. Again, it is observed that the change on the current regulator output voltage occurs in a few *ms*, both the magnitude and phase being potentially useful for islanding detection purposes. The differences among the voltages required to compensate the high frequency current are due to the different lines impedances (i.e. lines between the inverters and the PCC). In this case, inverter 2 has a transmission line placed between its LCL output and the PCC (Fig. 19) that makes smaller the required voltage to compensate its input current. It is finally noted that although the variation of the current PI regulator output (see Fig. 21) between island and grid-connected modes is small, the signal is very clean, the transition being therefore reliably detected.

Finally, Fig. 22 shows the magnitude of the most relevant current harmonics due to the non-ideal behavior of the inverter for the *open-loop* and *current cancellation* modes respectively. As expected, the current cancellation mode eliminates the selected component of the harmonic current. It is noted that the current THD at the PCC is ≈2.13% in the *open-loop mode,* reducing to ≈1.6% in the *current cancellation mode*, i.e. when the -5th harmonic is compensated by the harmonic current regulator (see Fig. 9).



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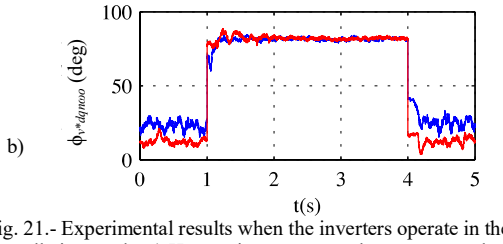

Fig. 21.- Experimental results when the inverters operate in the Current cancellation mode. a) Harmonic current regulator output voltage and b) phase. Dead-time=3µs.

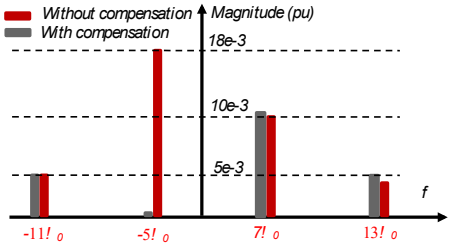

Fig. 22.- Experimentally measured harmonics of the current complex vector with and without compensation of the -5th harmonic implemented at the PCC. Dead-time=3µs.

VIII. Conclusions

An islanding detection method which uses harmonic components of the fundamental frequency caused by the non-ideal behavior of the inverter (mainly the dead-time) has been presented in this paper. The proposed method provides a reduced NDZ, similar to active islanding detection method. However, since these harmonic components occur naturally and no additional signal needs to be injected, it has no adverse effect on the system power quality. Consequently, it combines the reduced NDZ of active islanding detection methods with the grid-friendly properties of passive islanding detection methods.

Two different implementations, namely o*pen-loop mode* and c*urrent cancellation mode*, have been proposed, the second providing better performance in general, as it improves the current THD at PCC and can be used in scenarios with multiple inverters operating in parallel.

Simulations and experimental results have been provided to confirm the viability of the method. Changes between island and grid connected conditions can be detected in ≈100 *ms*, which is fast enough to meet the islanding detection standards [2-9]. Regardless of the relatively small value of the voltage harmonics due to the dead-time compared to the values reported in the literature for other high frequency signal injection based methods [12-13, 10-18, 35-38], implementation of the method has not required special voltage and current sensors in most of the applications. Finally, the computational requirements of the method are relatively small, meaning that it can be easily integrated into the type of digital signal processors that are currently being used in grid connected VSIs.

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