A New Method for Islanding Detection of Inverter-Based Distributed Generation Using DC-Link Voltage Control

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Abstract—This paper presents a new method for islanding detection of inverter-based distributed generation (DG). The main idea of this paper is to change the dc-link voltage considering the PCC voltage changes during islanding condition. A simple islanding detection scheme has been designed based on this idea. The proposed method has been studied under multiple-DG operation modes and the UL 1741 islanding tests. The simulations results, carried out by MATLAB/Simulink, show that the proposed method has a small nondetection zone. Also, this method is capable of detecting islanding accurately within the minimum standard time.

Index Terms—Distributed generation (DG), islanding, nondetection zone (NDZ), voltage-source inverter.

I. INTRODUCTION

DISTRIBUTED generation (DG) has been widely used in the power industry due to market deregulation and environmental concerns [1]. Islanding protection is one of the most important issues to address in DG applications. In [2] and [3], the islanding is defined as a condition in which a portion of an electric power system is solely energized and separated from the rest of the electric power system. The DG unit should detect the islanding and disconnect the islanded system in a timely manner to avoid damages [2]. Unintentional islanding of DG may result in power-quality (PQ) issues, interference with protection devices, and reliability reduction for customers. There are three main methods of islanding detection: 1) passive, 2) active, and 3) communication-based methods [4].

Passive methods continuously monitor the system parameters, such as voltage, frequency, harmonic distortion, etc. In this technique, one or more of these parameters has/have been considerably changed when the grid is islanded. Setting a proper threshold can help to differentiate between the islanding and grid-connected conditions. The over/underfrequency protection method uses upper and lower frequency thresholds, which are usually set at 60.5 and 59.3 Hz, respectively [3]–[5]. The over/undervoltage protection method uses upper and lower

voltage thresholds, which are set at 110% and 88% of the nominal voltage value , respectively [3]–[5]. Upper and lower thresholds have been used to avoid unwanted tripping of the DG due to other system disturbances [4]. Sometimes the load closely matches the DG capacity. In this case, the amount of frequency or voltage deviation will not be sufficient to trigger the islanding detection system [4]. Several passive islanding detection methods are available, such as undervoltage/overvoltage [6], [7]; underfrequency/overfrequency [6], [7]; rate of change of active power [8], [9]; rate of change of frequency (ROCOF) [7], [10]; and [11] rate of change of frequency over power [12], voltage and power factor changes [13], phase jump detection [14], and voltage unbalance and total harmonic distortion [15], [16]. Passive islanding detection methods suffer from large nondetection zones (NDZs) [3], [4]. NDZs are defined as a loading condition for which an islanding detection method would fail to operate in a timely manner.

Active techniques have been designed to force DG to be unstable in islanding mode [17] and interact with the operation of the power system directly [18]. The main advantage of active techniques over passive techniques is their small NDZ [7]–[19] and [20]. Active methods include slide-mode frequency shift [21], active frequency drift or frequency bias [22], Sandia frequency shift [23], and harmonic distortion base [19]. Active methods have a smaller NDZ and can degrade the PQ of the power system [24], [25]. Communication-based methods do not have any NDZ, but they are more expensive than the former methods [24].

This paper presents a new islanding detection method, which has the advantages of active and passive islanding methods, small NDZ, and good accuracy. The control strategy of the voltage-source inverter has been designed to operate at unity power factor. Also, the dc side has been modeled by a controllable dc voltage source. The main idea of this paper is to change the dc-link voltage considering the PCC voltage changes during the islanding condition. A simple and easy-to-implement method, such as the over/undervoltage protection (OVP/UVP), can be used to detect an islanding condition. Once the magnitude of voltage exceeds a determined threshold value, an islanding condition is detected and DG is disconnected.

In this paper, the system is modeled in Section II. The proposed islanding detection method is discussed in Section III. The performance of the proposed method is evaluated in Section IV. A comparison from the PQ point of view is presented in Section V. The last section consists of conclusions.

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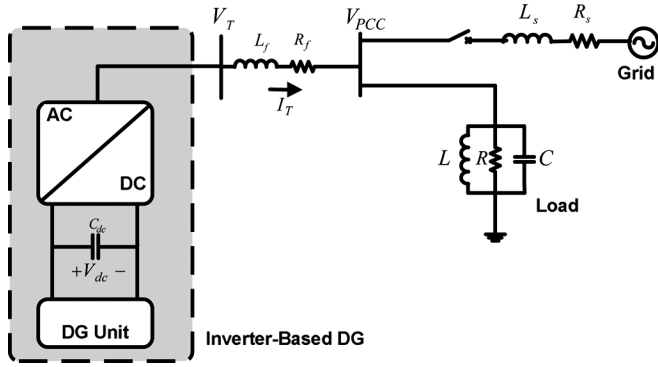
Fig. 1. Modeled system.

II. System Under Study

The system, which has been studied in this paper, is shown in Fig. 1. This system consists of a distribution network modeled by a three-phase voltage source behind impedance, a load modeled by a three-phase constant impedance, and a DG system. The DG is modeled by a controllable dc voltage source behind a three-phase inverter. The rating of this inverter is 100 kW. The other parameters have been given in [4], [5], and [17].

Fig. 2 shows the control scheme based on dq synchronous reference frame. In this system, the dc-link voltage controller and reactive-power controller determine d and q components, respectively. The input power extracted from the DG unit is fed into the dc link. Therefore, the voltage controller counteracts the voltage variation by specifying an adequate value of the d axis inverter current to balance the power flow of the dc link [26].

The reactive power controller, shown in Fig. 2, specifies the reference value for the q component of the converter current. The reactive power reference value (Q_{ref}) is set to zero in order to model a unity power factor DG operation. Also, Fig. 2 shows two proportional-integral (PI) controllers for the d- and q-axis current controls. The outputs of these controllers obtain the reference voltages for the PWM signal generator. The main features of the current control strategy are the limitation of the converter output current during a fault condition, providing over-current protection, and reducing the fault current contribution of the unit [26].

The instantaneous real and reactive power could be written in terms of the dq axis components, as follows [27], [28]:

$$P = \frac{3}{2} v_{dpcc} \cdot i_{dt} \tag{1}$$

$$Q = \frac{3}{2} v_{dpcc} \cdot i_{qt} \tag{2}$$

where v_{dpcc} is the phase peak value of the PCC voltage. i_{dt} and i_{qt} are orthogonal components of inverter currents. The dq components of the voltage and current are constant values in the steady-state condition. Therefore, the controller provides the independent regulation of d and q components [27], [28]. The instantaneous voltages of the three phases could be expressed by the following equation [27], [28]:

$$\frac{d}{dt} i_{t(abc)} = -\frac{R_f}{L_f} i_{t(abc)} + \frac{1}{L_f} [v_{t(abc)} - v_{pcc(abc)}] \tag{3}$$
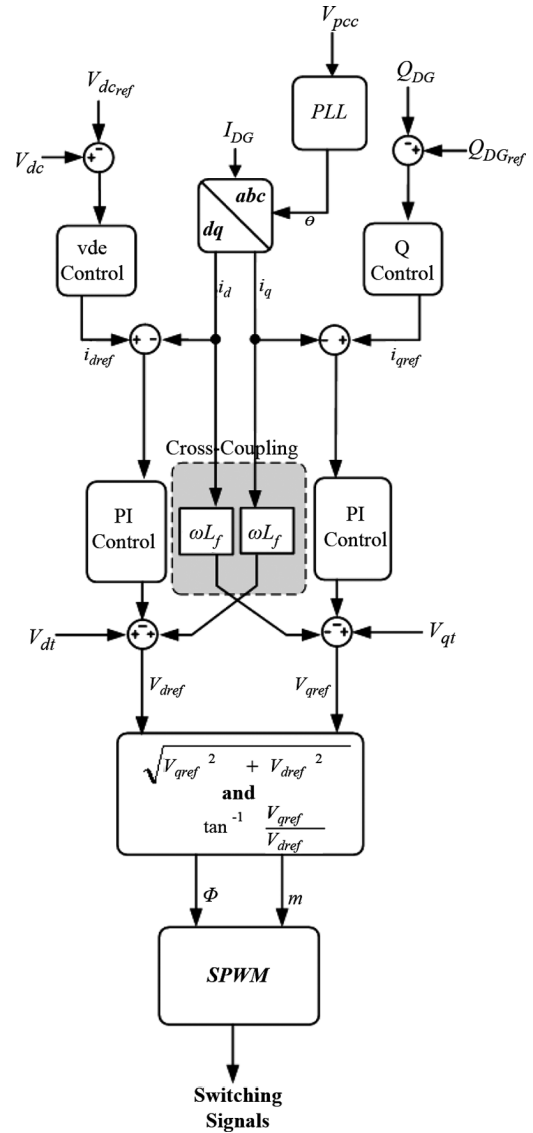

Fig. 2. Block diagram of the DG inverter controller.

where $i_{t(abc)}$ represents the DG current three-phase components. R_f and L_f are the filter resistance and inductance, respectively. $v_{t(abc)}$ and $v_{pcc(abc)}$ represent the DG terminal and PCC three phase voltages, respectively. By using Park's transformation [27], (3) can be transformed to the rotating synchronous reference frame, as follows [4], [27] and [28]:

$$\frac{d}{dt} \begin{bmatrix} i_{\text{dt}} \\ i_{qt} \end{bmatrix} = \begin{bmatrix} \frac{-R_f}{L_f} & \omega \\ -\omega & \frac{-R_f}{L_f} \end{bmatrix} \begin{bmatrix} i_{\text{dt}} \\ i_{\text{qt}} \end{bmatrix} + \frac{1}{L_f} \begin{bmatrix} v_{\text{dt}} - v_{dpcc} \\ v_{\text{qt}} - v_{qpcc} \end{bmatrix}. \tag{4}$$

Or

$$\frac{d}{dt} \begin{bmatrix} i_{\text{dt}} \\ i_{\text{qt}} \end{bmatrix} = \begin{bmatrix} \frac{-R_f}{L_f} & 0 \\ 0 & \frac{-R_f}{L_f} \end{bmatrix} \begin{bmatrix} i_{\text{dt}} \\ i_{\text{qt}} \end{bmatrix} + \frac{1}{L_f} \begin{bmatrix} u_d \\ u_q \end{bmatrix} \tag{5}$$

where

$$u_d = v_{dt} - v_{dpcc} + \omega L_f i_{\text{qt}} \tag{6}$$

$$u_q = v_{\text{qt}} - v_{qpcc} - \omega L_f i_{\text{dt}}. \tag{7}$$

The DG interface control is modified by using the set of equations shown in Fig. 2. The magnitude and angle of the modulating signal are calculated and then the switching pattern of the inverter has been determined.

PWM three-phase inverters should shape and control the three-phase output voltage in magnitude and frequency with the essentially constant input dc voltage [29]. In the linear region (i.e., $m_a \leq 1.0$), the fundamental frequency component in the output voltage ($(\hat{V}_{AN})_1$) determines the amplitude-modulation ratio (m_a), by the following equation [29]:

$$(\hat{V}_{AN})_1 = m_a \frac{v_{dc}}{2} \tag{8}$$

$$m_a = \frac{v_{control}}{v_{tri}} \tag{9}$$

where $v_{control}$ is the peak amplitude of the control signal and the v_{tri} is the amplitude of the triangular signal. Therefore, the line-to-line rms voltage at the fundamental frequency can be written, as follows [29]:

$$V_{L-L(line-line,rms)} = \frac{\sqrt{3}}{\sqrt{2}} (\hat{V}_{AN})_1 = \frac{\sqrt{3}}{2\sqrt{2}} m_a v_{dc}$$
$$\approx 0.612 m_a v_{dc} \quad (m_a \leq 1.0). \tag{10}$$

Now, the following equations can be written for v_{dt} and v_{qt}:

$$v_{dt} = 0.612 \cdot m_a v_{dc} \cos(\phi) \tag{11}$$

$$v_{qt} = 0.612 \cdot m_a v_{dc} \sin(\phi) \tag{12}$$

where ϕ is the angle by which the inverter voltage vector leads the line voltage vector. In a lossless inverter, the instantaneous power at the ac and dc terminals of the inverter is equal. This power balance can be written, as follows:

$$v_{dc} \cdot i_{dc} = \frac{3}{2} (v_{dt} i_{dt} + v_{qt} i_{qt}). \tag{13}$$

At the dc link, we have

$$i_{dc} = C_{dc} \cdot \frac{d}{dt} v_{dc}. \tag{14}$$

By using (4) and (11)–(14), the following state equations can be written [27]:

$$\frac{d}{dt} \begin{bmatrix} i_{dt} \\ i_{qt} \\ v_{dc} \end{bmatrix} = [A] \begin{bmatrix} i_{dt} \\ i_{qt} \\ v_{dc} \end{bmatrix} + \begin{bmatrix} \frac{-1}{L_f} & 0 \\ 0 & \frac{-1}{L_f} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} v_{dpcc} \\ v_{qpcc} \end{bmatrix}$$

$$[A] = \begin{bmatrix} \frac{-R_f}{L_f} & \omega & \frac{0.612 \cdot m_a}{L_f} \cos\phi \\ -\omega & \frac{-R_f}{L_f} & \frac{0.612 \cdot m_a}{L_f} \sin\phi \\ \frac{3 \times 0.612 m_a}{2C_{dc}} \cos\phi & \frac{3 \times 0.612 m_a}{2C_{dc}} \sin\phi & 0 \end{bmatrix}. \tag{15}$$

III. PROPOSED ISLANDING DETECTION METHOD

The acceptable voltage deviation is in the range of 88% to 110% of the nominal voltage [2], [3]. Any voltage deviation in this range should not be detected and the corresponding load condition would be considered within the NDZ. It is assumed that DG has been designed to operate at a constant dc voltage of 900 V. In this section, a new analytical formulation is derived by the linearization of system state equations. Then, a new $V_{dc} - V_{PCC}$ characteristic of DG will be explained, and the performance of this method will be evaluated.

A. Linearization of System State Equations

To measure the impact of deviation of m_a on dc-link voltage, ϕ has been kept constant and only m_a has been considered as a variable. As a result, (15) is a nonlinear equation. However, for a small perturbation around the equilibrium point m_a, the following linear set of equations can be obtained, where subscript 0 denotes steady-state values [27], as shown in (16) at the bottom of the page.

The inverter steady-state model can be obtained from the dynamic model by setting the derivative terms equal to zero. After transformation from abc to the dq reference frame, the voltages and the currents become dc quantities. Therefore, substituting

$$\frac{d}{dt} \begin{bmatrix} \Delta i_{dt} \\ \Delta i_{qt} \\ \Delta v_{dc} \end{bmatrix} = [\Delta A] \begin{bmatrix} \Delta i_{dt} \\ \Delta i_{qt} \\ \Delta v_{dc} \end{bmatrix} + [\Delta B] \begin{bmatrix} \Delta v_{dpcc} \\ \Delta v_{qpcc} \\ \Delta m_a \end{bmatrix}$$

$$[\Delta A] = \begin{bmatrix} \frac{-R_f}{L_f} & \omega_0 & \frac{0.612 m_{a0}}{L_f} \cos\phi \\ -\omega_0 & \frac{-R_f}{L_f} & \frac{0.612 m_{a0}}{L_f} \sin\phi \\ \frac{3 \times 0.612 m_{a0}}{2C_{dc}} \cos\phi & \frac{3 \times 0.612 m_{a0}}{2C_{dc}} \sin\phi & 0 \end{bmatrix}$$

$$[\Delta B] = \begin{bmatrix} -\frac{1}{L_f} & 0 & \frac{0.612 \cdot v_{dc0} \cdot \cos\phi}{L_f} \\ 0 & -\frac{1}{L_f} & \frac{0.612 \cdot v_{dc0} \cdot \sin\phi}{L_f} \\ 0 & 0 & \frac{3 \times 0.612}{2C_{dc}} (\cos\phi \cdot i_{dt0} + \sin\phi \cdot i_{qt0}) \end{bmatrix}. \tag{16}$$
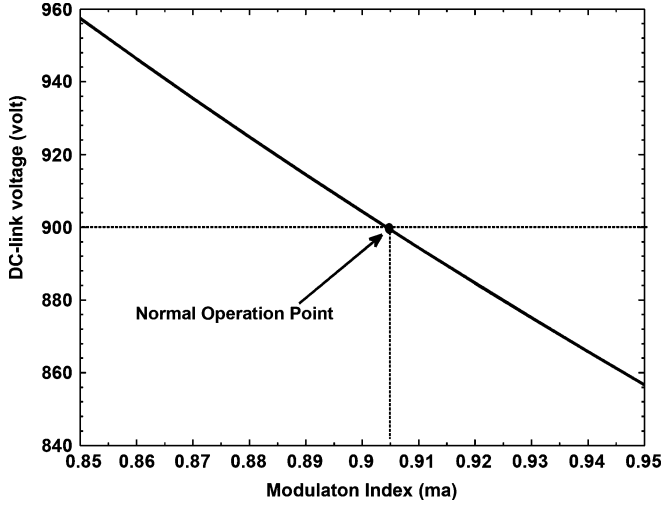
Fig. 3. Steady-state variations of V_{dc} versus m_a (with $L_f = 2.1$ mH, $\phi = 377$ rad/s, $R_f = 0.00145$ Ω, $\phi = 20°$ and $V_{\mathrm{pcc}} = 1$ p.u.).

Fig. 4. DC voltage versus PCC voltage characteristic (DG and $V_{\mathrm{dc-ref}}$ are set to 900 V).

$v_{\mathrm{dpcc}} = |v_{\mathrm{pcc}}|$, $v_{\mathrm{qpcc}} = 0$, $i_d = I_d$, and $i_q = I_q$ and simplification of the steady-state model resulted in the following equation:

$$\begin{bmatrix} -R_f & \omega L_f & 0.612 m_a \cos \phi \\ -\omega L_f & -R_f & 0.612 m_a \sin \phi \\ 0.612 m_a \cos \phi & 0.612 m_a \sin \phi & 0 \end{bmatrix} \begin{bmatrix} I_{\mathrm{dt}} \\ I_{\mathrm{qt}} \\ v_{\mathrm{dc}} \end{bmatrix} = \begin{bmatrix} |v_{\mathrm{pcc}}| \\ 0 \\ 0 \end{bmatrix}. \quad (17)$$

By solving (17) for i_{dt}, i_{qt} and v_{dc}, we have

$$I_{\mathrm{dt}} = \frac{\cos(2\phi) - 1}{2 R_f} \cdot |v_{\mathrm{pcc}}| \quad (18)$$

$$I_{\mathrm{qt}} = \frac{\sin(2\phi)}{2 R_f} \cdot |v_{\mathrm{pcc}}| \quad (19)$$

$$V_{\mathrm{dc}} = \frac{(1.634 \cdot R_f \cdot \cos \phi) - (1.634 \cdot \omega L_f \cdot \sin \phi)}{R_f \cdot m_a} \cdot |v_{\mathrm{pcc}}|. \quad (20)$$

Considering (18) and (19), it is obvious that I_{dt} and I_{qt} do not depend on the modulation index (m_a). For the given system, the variations of V_{dc} versus m_a can be determined by using (20). By considering it as a constant value, (20) becomes a hyperbolic equation. But the part $m_a < 0$ is not acceptable and just the part $0 < m_a < 1$ is the dominant. By scaling m_a between 0.8 and 1, it can be seen that the deviation of m_a versus V_{dc} is linear and usually the normal operating point of the inverter is in this range. The $V_{\mathrm{dc}} - m_a$ curve of this range has been shown in Fig. 3

Considering (10), we have

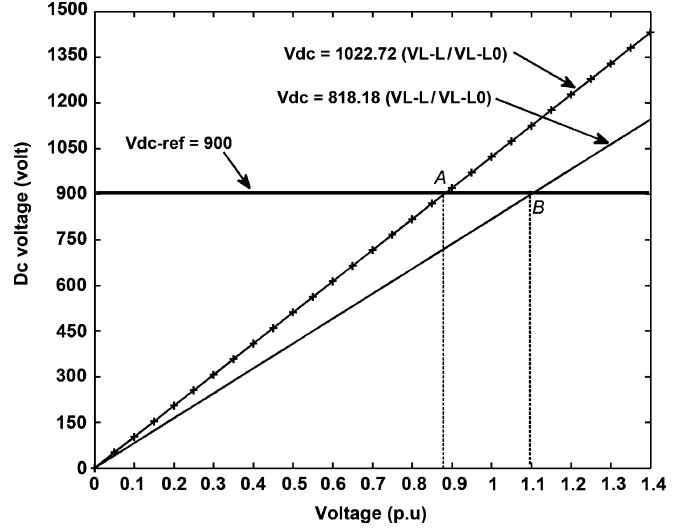$$V_{\mathrm{dc}} = \frac{V_{L-L}}{0.612 \cdot m_a}. \quad (21)$$

In steady-state condition, (10) can be written as follows:

$$V_{\mathrm{dc}_0} = \frac{V_{L-L_0}}{0.612 \cdot m_{a_0}}. \quad (22)$$

By combining (21) and (22), we have

$$V_{\mathrm{dc}} = V_{\mathrm{dc}_0} \cdot \left(\frac{V_{L-L}}{V_{L-L_0}} \right) \cdot \left(\frac{m_{a_0}}{m_a} \right). \quad (23)$$

Considering (20) and Fig. 3, it is obvious that the deviation of m_a around the operating point does not have any major impact on drifting of the dc-link voltage. Therefore, the modulation index can be assumed to be constant (i.e., $m_a = m_{a0}$). Then, (23) can be written as follows:

$$V_{\mathrm{dc}} = V_{\mathrm{dc}_0} \cdot \left(\frac{V_{L-L}}{V_{L-L_0}} \right). \quad (24)$$

B. $V_{\mathrm{dc}} - V_{\mathrm{PCC}}$ Characteristic

The $V_{\mathrm{dc}} - V_{\mathrm{PCC}}(V_{L-L})$ characteristic of DG and dc reference voltage have been shown in Fig. 4. In this figure, there are 2 lines which presenting the lower and upper dc voltage limits. Using (24) and assuming V_{L-L0} equal to 1 p.u, the slope of these lines $(V_{\mathrm{dc}0})$ can be determined for $V_{\mathrm{rmdc}} = 900$ V and the dc voltage limits. The intersect point of DG and dc-link reference voltage curves is called the islanding operating point. In this figure, points "A" and "B" represent the operating point of the lower and upper dc-link voltage limits, respectively. Each operating point between these two lines is in the NDZ. In addition, in any kind of loading condition, the dc-link voltage would be placed within or without these boundaries. If V_{dc} is accommodated within these limits, the voltage deviation will be in the allowable values, and the islanding can occur and will not be detected (NDZ).

In this paper, the DG reference dc voltage curve has been modified and expressed by the PCC voltage-dependent line.
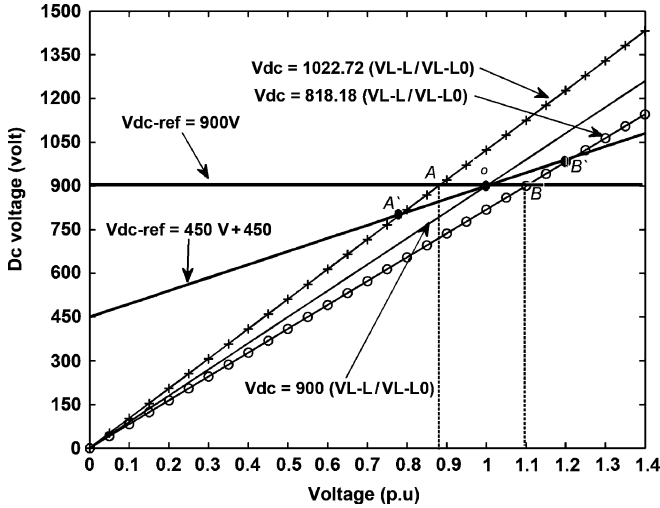
Fig. 5.   DC voltage versus the PCC voltage characteristic for DG and modified $V_{\mathrm{dc-ref}}$.

Fig. 6.   DC voltage versus the PCC voltage characteristic, effect of negative slope.

This line should cross the point which has the rated dc voltage at the rated PCC voltage. It can be expressed by the following equation:

$$V_{\mathrm{dc-ref}} = k_1 \cdot V_{\mathrm{PCC}} + k_2. \qquad (25)$$

Fig. 5 presents the dc voltage versus the PCC voltage lines for three (dc voltage) conditions. By changing "A" and "B" points to "A'" and "B'," the NDZ is smaller, because these new points are outside the allowable voltage limits (88% and 110% of nominal voltage), so this condition can be easily detected. As an example, the DG reference dc voltage can be rewritten, as follows:

$$V_{\mathrm{dc-ref}} = 450 \cdot V_{\mathrm{PCC}} + 450. \qquad (26)$$

The load condition, which intersects the DG voltage line at point "o," has an active power of 100 kW and the voltage of 1 p.u. Equation (26) intersects the lower and upper limits at points "A'" and "B'," respectively. These two points correspond to voltage levels that are beyond the allowable voltage levels. Thus, these loading conditions can be easily detected by using the over/undervoltage protection (OVP/UVP) methods. As a result, a reduction in the NDZ can be achieved.

The reference dc voltage can be expressed by a negative slope, as follows:

$$V_{\mathrm{dc-ref}} = -450 \cdot V_{PCC} + 1350. \qquad (27)$$

Fig. 6 presents the dc voltage versus PCC voltage lines for the same conditions, presented in Fig. 5. The lower and upper limits intersect the new DG line by (27) at points "A'" and "B'," respectively. The voltage levels of these two points are in the NDZ. Therefore, these loading conditions will not be detected by using OVP/UVP methods. Therefore, the negative slope in (27) will lead to an increase in the NDZ and the positive slope can reduce the NDZ. The values of parameters k_1 and k_2 have
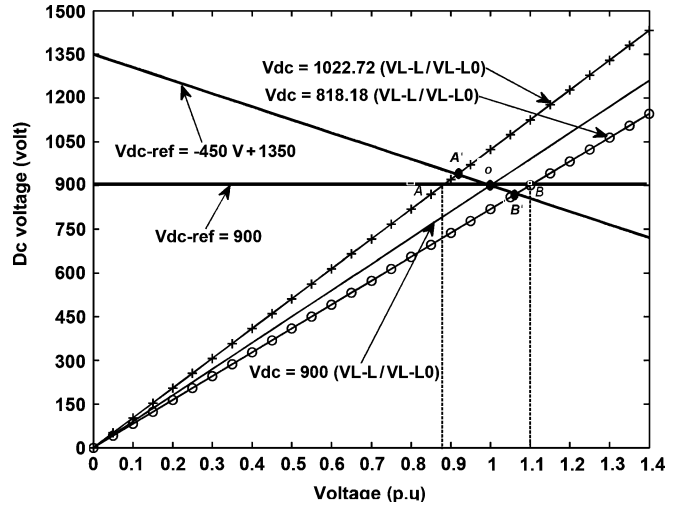

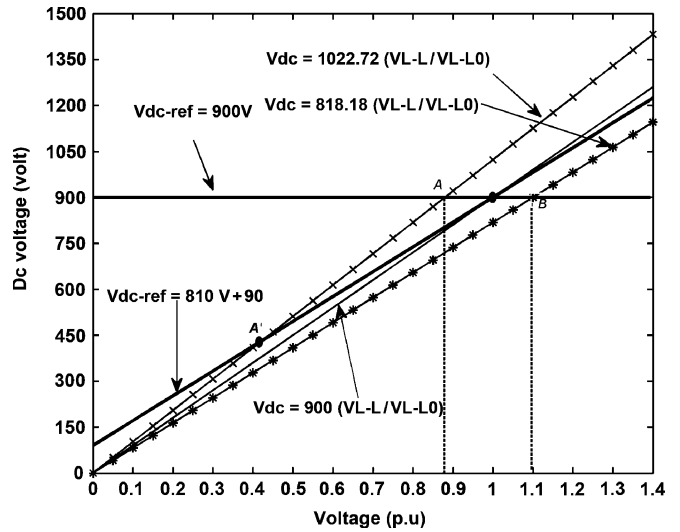
Fig. 7.   DC voltage versus the PCC voltage characteristic, with an effect of the selection of (31).

been chosen so that the DG $V_{\mathrm{dc}} - V_{\mathrm{PCC}}$ slope is placed higher than the slope of all possible load lines within the NDZ. Considering (24), the following equations have been used to tune k_1 and k_2

$$\frac{V_{\mathrm{dc}} - V_{dc0}}{V_{L-L} - V_{L-L_0}} = \frac{dV_{\mathrm{dc}}}{dv}\Big|_{V_{L-L}=V_{L-L_0}} \qquad (28)$$

$$\frac{V_{\mathrm{dc}} - V_{dc0}}{V_{L-L} - V_{L-L_0}} = \frac{V_{dc0}}{V_{L-L_0}} \qquad (29)$$

$$V_{\mathrm{dc}} = \frac{V_{dc0}}{V_{L-L_0}} V_{L-L}. \qquad (30)$$

Based on these equations, it can be stated that $k_1 = V_{dc0}/V_{L-L_0}$ ($V_{dc0} = 900$ volts, $V_{L-L_0} = 1$ p.u.) and $k_2 = 0$ are a suitable condition. But it must be mentioned that k_2 cannot be equal to zero. This is because if $k_1 = 900$ and $k_2 = 0$, then the system will be very sensitive to PCC voltage perturbations,
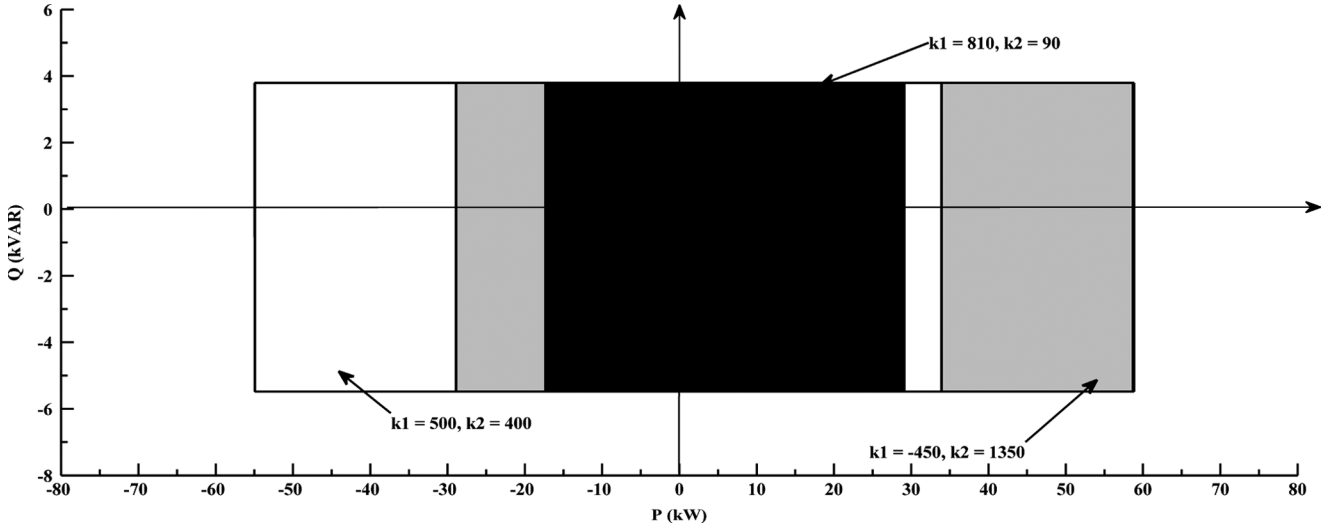
Fig. 8. NDZ of the $V_{\rm dc} - V_{\rm PCC}$ characteristic for a different amount of k_1 and k_2.

and it will lead to undesirable system tripping. To protect the system from this situation, based on the simulation results and IEEE 1547 Standard and other power system standards (the allowable voltage deviation for DGs below 500 kVA is 10% of the nominal voltage), it is supposed to have a good selection for k_2, when it is about 10% of the dc link voltage. As a result, (25) has been changed into the following form:

$$V_{\rm dc-ref} = 810 \cdot V_{\rm PCC} + 90. \qquad (31)$$

C. Performance Evaluation

The performance of the proposed islanding detection method as well as its NDZ depends on the $V_{\rm dc} - V_{\rm PCC}$ DG characteristic. A PCC voltage variation (ΔV) will result in a dc-link voltage variation $(\Delta V)_{\rm dc}$ which could be expressed, as follows:

$$V_{\rm dc-ref} = V_{\rm dc} \left(\frac{V_{L-L}}{V_{L-L_0}} \right) = k_1 \cdot V_{L-L} + k_2 \qquad (32)$$

$$(V_{\rm dc_0} + \Delta V_{\rm dc}) \left(\frac{V_{L-L_0}(1+\Delta V)}{V_{L-L_0}} \right)$$

$$= k_1 \times V_{L-L_0}(1+\Delta V) + k_2 \qquad (33)$$

$$(V_{\rm dc_0} + \Delta V_{\rm dc}) = \frac{k_1 \times V_{L-L_0}(1+\Delta V) + k2}{(1+\Delta V)}. \qquad (34)$$

Table I shows the calculated NDZs for different values of k_1 and k_2 presented in this paper. It can be seen that the selection of the $V_{\rm dc} - V_{\rm PCC}$ characteristic will have a great impact on NDZ. If the boundary between lower and upper limits of NDZ is a large number, it will lead to a wide NDZ. In some cases, NDZ has a large gap (e.g., case No. 2), while for other cases, it is relatively small (e.g., case No. 3). NDZ can either be represented in terms of power mismatch or in terms of the load R, L, and C. An accurate presentation of the NDZ can be found in [17]. The

TABLE I
NDZ UPPER AND LOWER LIMITS FOR DIFFERENT $V_{\rm dc} - V_{\rm PCC}$

Case Number	k_1	k_2	Lower limit of NDZ	Upper limit of NDZ
1	450	450	825	1092.9
2	-450	1350	675	1478.6
3	810	90	885	938.5

details have been presented in the Appendix. This paper examines the NDZ of an OVP/UVP and OFP/UVP islanding scheme in case of using the implemented $V_{\rm dc} - V_{\rm PCC}$ characteristic for different amounts of k_1 and k_2. The results have been plotted in Fig. 8.

IV. SIMULATION RESULTS

In this section, the test system shown in Fig. 1 has been simulated by MATLAB/Simulink. The system, DG, and load parameters are listed in Table II. The parameter $Q_{\rm ref}$ has been set to 0 MVAr. The Islanding detection method has been tested for load with a quality factor (Q_f) of 1.77. The proposed islanding detection method has been also tested for various loading conditions specified in the UL 1741 Standard [3].

A. UL 1741 Testing

Based on the UL 1741 Standard, the active load power is adjusted to set the inverter at 25%, 50%, 100%, and 125% of the rated output power of the inverter. The reactive power has been adjusted between 95% and 105% of the balanced condition (unity power factor loading) in 1% steps [3]. The islanding detection scheme is tested based on the procedure presented in [3]. But all results have not been presented in this section. The DG interface has been equipped with the $V_{\rm dc-ref}$ characteristic given in (31) and islanding has occurred at $t = 0.8$ s. The first simulation result using the proposed method is shown in Fig. 9. This figure shows the voltage at the PCC during an islanding condition, for the active load power adjusted at 50%, 100%, and 125% of its rated output power. The reactive power has been adjusted at 100% of the balanced condition. As can be seen in

TABLE II
SYSTEM, DG, AND LOAD PARAMETERS

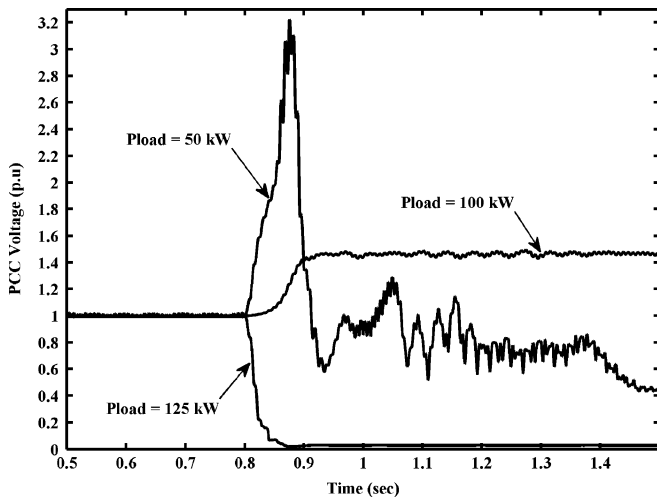| Grid and Inverter Parameters	
DG Output power	100 kW
Switching Frequency	8000 Hz
Input DC Voltage	900 V
Voltage (Line to Line)	480V
Frequency	60 Hz
Grid Resistance	0.02 Ω
Grid Inductance	0.3 mH
Filter Inductance	2.1 mH
DG Controller Parameters	
Q Control	$K_p = 0.1, K_i = 0.01$
V_{dc} Control	$K_p = 0.15, K_i = 9.78$
PI Control	$K_p = 1, K_i = 1250$
Load Parameters	
R	2.304 Ω
L	0.00345 H
C	2037 μF

Fig. 9.   PCC voltage using the proposed $V_{dc} - V_{PCC}$ characteristic for different loads.

Fig. 9, the PCC voltage exceeds the OVP/UVP thresholds in less than 100 ms (after the occurrence of islanding).

Fig. 10 shows the voltage at the PCC during an islanding condition, for the following cases [4]:

Case 1) The load has been adjusted to operate at 100% of rated active power with 101% reactive power in the balanced condition.

Case 2) The load has been adjusted at 100% of the rated active power with 100% reactive power.

Case 3) The load has been adjusted at 100% of its rated active power with 99% reactive power.

Table III lists the load parameters. It can be seen in Fig. 10 that the operation of the DG unit is stable as long as it is connected to the grid. After islanding instant ($t = 0.8$ s), the DG loses its stable operation, and the PCC voltage exceeds the OVP/UVP threshold values in less than 110 ms.
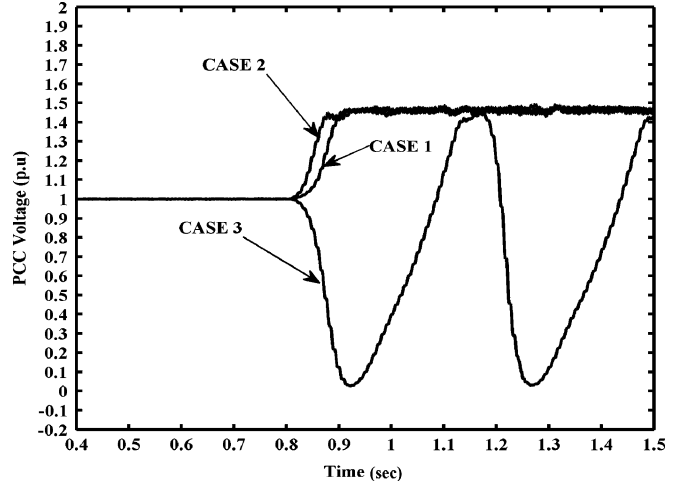

Fig. 10.   PCC voltage with proposed $V_{dc} - V_{PCC}$ characteristic for three cases.

TABLE III
LOAD PARAMETERS FOR UL 1741 TESTS

$P\%$	$Q\%$	R (Ω)	L (H)	C (μF)
50	100	4.603	0.00345	2037
125	100	1.841	0.00345	2037
100	99	2.304	0.003488	2037
100	100	2.304	0.00345	2037
100	101	2.304	0.003419	2037

B. Effect of Load Switching

The proposed islanding detection method has been tested for load switching in the grid-connected operation mode. In parallel with the old load, which has been presented in Fig. 1, the new load has been switched at $t = 0.5$ s and disconnected at $t = 1$ s. Three cases have been simulated in this test. In all cases, the load apparent power is equal to 100 kVA but the power factor is 0.8 lead, 1.0 and 0.8 lag. The simulation results that include the PCC voltage and frequency, and the DG active and reactive power outputs for three different loading conditions have been presented in Fig. 11. The voltage and frequency variations can be seen when the load is switched on and off. For simulated cases, the voltage and frequency variations are within the standard values. It is obvious that the proposed method does not interfere with the power system operation during normal conditions.

C. Effect of Load Quality Factor

The IEEE Standard 929 proposes the use of $Q_f \le 2.5$ for tests. Yet, recent standards (IEEE 1547.1) propose testing islanding with loads having a quality factor of 1 [30]. The UL 1741 test specifies that an islanding detection method must succeed in detecting the islanding phenomenon within 2 s for RLC loads with $Q_f \le 1.8$ [4]. For the system shown in Fig. 1, Q_f has changed in the range of 0.5 to 4.2 by adjusting the load inductance and capacitance according to Table IV.

Fig. 12 shows the PCC voltage for different values of Q_f. As can be seen in this figure, the voltage has exceeded the
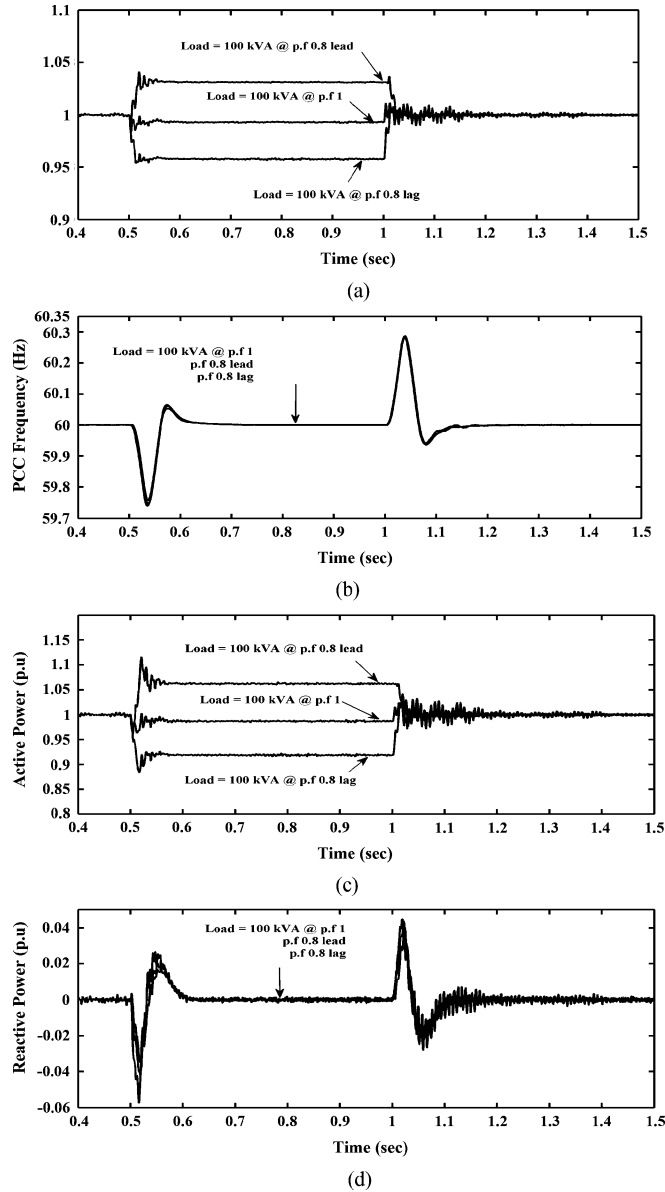
Fig. 11. System response during load switching. (a) PCC voltage. (b) PCC frequency. (c) Inverter active power. (d) Inverter reactive power.

TABLE IV
LOAD PARAMETERS FOR DIFFERENT Q_f

Q_f	R (Ω)	L (H)	C (μF)
0.5	2.304	0.0122	575.4
1	2.304	0.0061	1150
1.77	2.304	0.00345	2037
2.12	2.304	0.00288	2439
3	2.304	0.00203	3452
4.2	2.304	0.00145	4833.5

OVP/UVP thresholds in less than 110 ms for $Q_f = 0.5$ and 300 ms for $Q_f = 4.2$.

D. Multiple-DG Operation Mode

The proposed islanding detection method has been tested in a system with multiple DGs. For the simplification and demon-
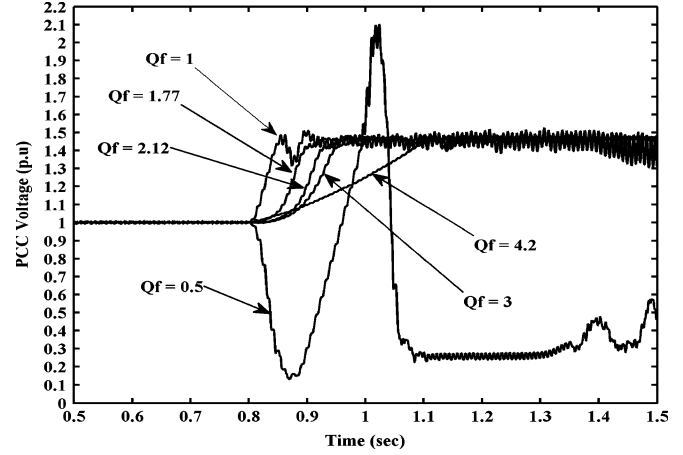

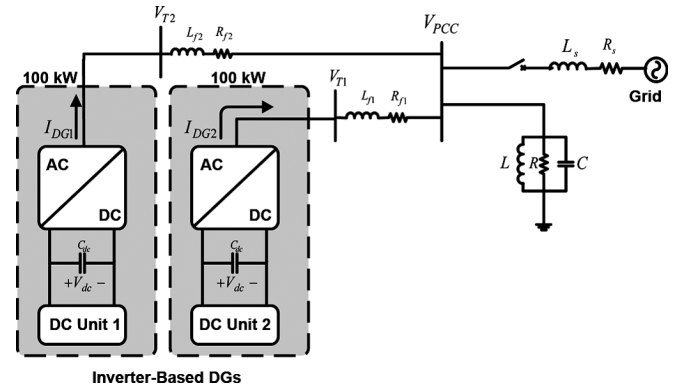Fig. 12. PCC voltage for different values of Q_f.

Fig. 13. Schematic diagram of the two-DG system.

stration of the interactions, two DG units are used in this study. Fig. 13 illustrates the operation of two DGs grid-connected inverters. Each DG is the same as the single DG system case and the rating of each of them is equal to 100 kW. They are connected to the PCC in parallel to supply the load with 200-kW active power. Each DG interface has been equipped with the proposed $V_{dc} - V_{PCC}$ characteristic presented in (31). Islanding has been simulated at $t = 0.8$ s and the load has a Q_f of 0.885. The simulation result has been presented in Fig. 14. It can be seen that DG loses its stable operation mode, and an islanding condition can be detected by using OVP/UVP methods in less than 50 ms.

V. PQ POINT OF VIEW

Compared with some useful active islanding detection methods, which, by nature, inject low-frequency distorted waveforms, the proposed method does not distort any waveforms. It simply manipulates the dc-link voltage by the continuous feedback signal of the PCC voltage. Therefore, this method does not have any considerable total harmonic distortion (THD). This is evident from the simulation results given in Table V. These results show that there is no THD degradation with and without using the proposed schemes in comparison with the GE method [31].

In this section, in order to have a comparison, SFS and the proposed methods have been simulated for a three-phase in-
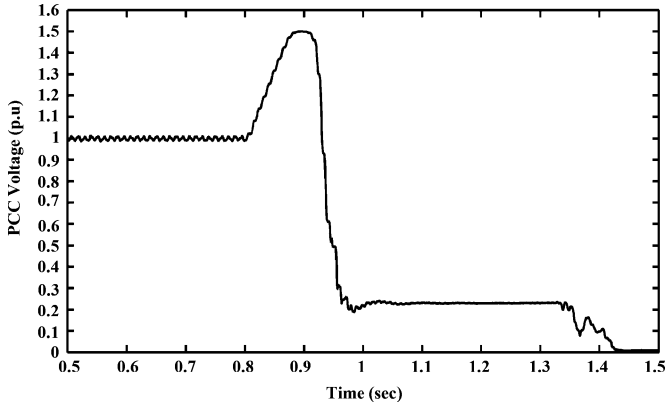
Fig. 14.　PCC voltage for the multiple-DG operation mode.

TABLE V
THD COMPARISON

Scheme status	Power (kW)	Proposed Method (in %)		GE Method (in %)	
		THD$_V$	THD$_i$	THD$_V$	THD$_i$
No-AI	100	0.0550	1.1408	0.096	1.769
AI-V	100	0.0685	1.1421	0.099	1.752
No-AI	66	0.1061	1.9120	0.117	2.918
AI-V	66	0.2038	1.9861	0.132	2.923
No-AI	33	0.1372	1.9673	0.367	5.809
AI-V	33	0.4297	2.1146	0.388	5.862

verter. The results have been shown in Fig. 15. It can be seen that the THD of the proposed method is much better than SFS. Also, there is a THD comparison between SFS and GE methods in [31] for the same test system and conditions. The inverter current THD of GE was equal to 0.13%. As a result, the THD of the proposed method is superior to SFS and GE.

VI. CONCLUSION

This paper proposes a new method for islanding detection of an inverter-based DG unit by using the $V_{dc} - V_{PCC}$ characteristic. The $V_{dc} - V_{PCC}$ characteristic has been chosen so that the DG maintains its stable operation in grid-connected and islanding condition modes. Applying the proposed $V_{dc} - V_{PCC}$ characteristic to the DG results in a simple islanding detection method, which can be similar to OVP/UVP protections. The suggested method has been studied for the inverter-based DG unit under the multiple-DG operation mode and the UL 1741 test conditions. The simulation results show the effectiveness of the new islanding detection method for different operating conditions. In addition, it has been shown that this method does not distort any voltage or current waveforms by injecting perturbations and, thus, it has high performance from a PQ point of view. This method is also capable of detecting islanding conditions accurately within the minimum standard time.

APPENDIX

In order to determine the amount of mismatch for which the OVP/UVP and OFP/UFP will fail to detect islanding, the load
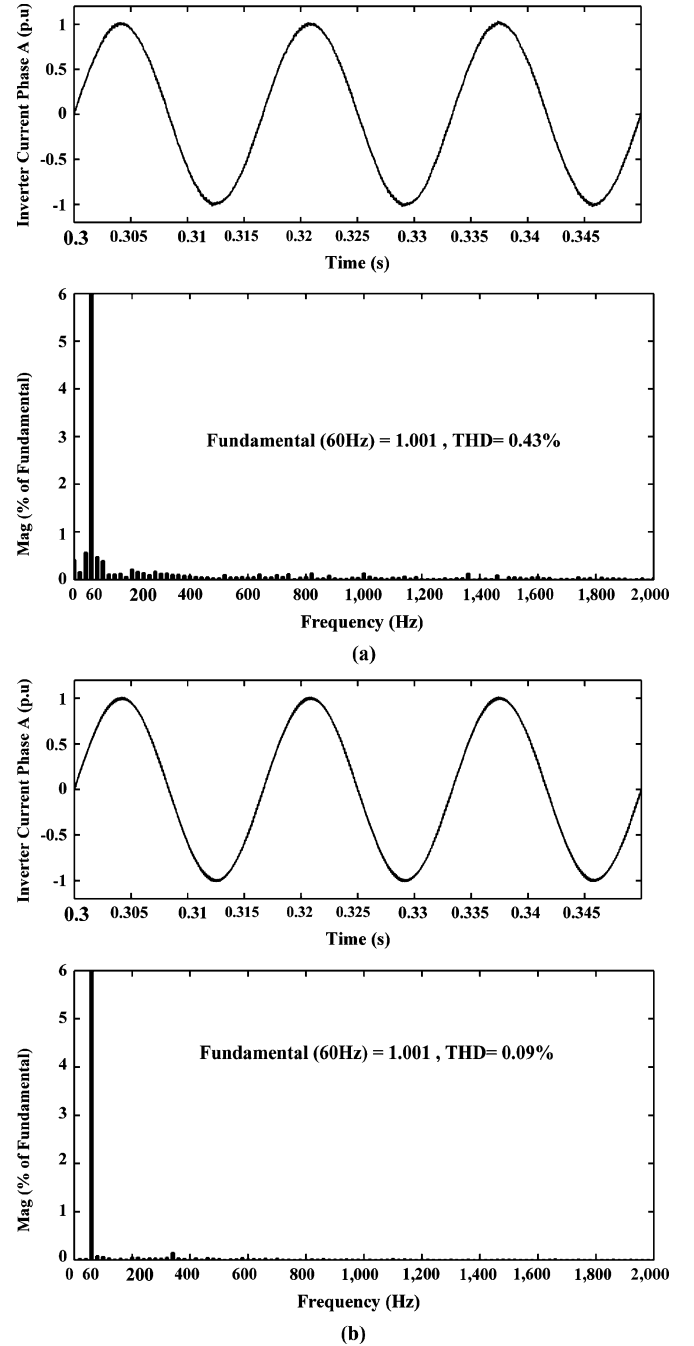

Fig. 15.　Inverter current THD comparison between the (a) SFS and (b) proposed methods.

reactive power can be expressed as follows [17]:

$$\Delta Q = \frac{3V^2}{\omega_n L}\left(1 - \frac{f_n^2}{(f_n \pm \Delta f)^2}\right) \qquad (35)$$

where ω_n is the nominal frequency and L is the load inductance. The values of reactive power mismatch (for a frequency threshold ranging from 59.3 Hz to 60.5 and load inductance of 0.00345 H) are 5.5 and 3.8 kVAR, respectively. Similarly, an equation for the active power mismatch has been derived in [17].

The active power mismatch in this case is related to voltage deviation on the dc-link bus and can be expressed by the following equation:

$$\Delta P = \frac{3V^2}{R}\left(1 - \frac{1}{(1 \pm \Delta V)^2}\right) \tag{36}$$

$$V = \frac{(V_{\text{dc}} - k1)}{k2}. \tag{37}$$

Combining (36) and (37), results in the following equation:

$$\Delta P = \frac{3\left(\frac{(V_{\text{dc}}-k1)}{k2}\right)^2}{R}\left(1 - \frac{1}{(1 \pm \Delta V)^2}\right). \tag{38}$$

For the voltage variation in the range of 88%–110%, the power mismatches calculated by using (38) for $k1 = 810$, $k2 = 90$ are equal to 29.3 kW and 17.3 kW, respectively. Also, the power mismatches for $k1 = 500$, $k2 = 400$ are equal to 35.95 kW and 55.85 kW, respectively. For the last case, the power mismatches of $k1 = -450$, $k2 = 1350$ are equal to 58.95 kW and 28.33 kW, respectively.

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