Study on A High Voltage Gain SEPIC-Based DC-DC Converter with Continuous Input Current for Sustainable Energy Applications

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***Abstract*— A high step-up DC-DC converter is proposed in this paper. The presented converter benefits from some advantages such as high voltage gain and continuous input current which makes it suitable for the renewable energy applications. The presented converter is based on the Sepic converter. However, the converter voltage gain is improved by employing a coupled inductor and two voltage multipliers. A passive clamp circuit is also added to the proposed converter which increases the voltage gain and reduces the voltage stress on the main switch. Thus, a switch with low $R_{DS(on)}$ will be needed which decreases the conduction loss. Besides, the voltage stress on the output diode in the proposed converter is reduced which alleviates reverse recovery problem. The steady state analysis of the proposed converter is discussed in this paper. The analysis is verified with experimental results under the output power of 245 W.**

***Index Terms*— DC-DC converter, High voltage gain, voltage multiplier.**

I. INTRODUCTION

NOWADAYS, DC/DC converters are widely employed in various fields of industries. The renewable energy deployment such as photovoltaic panels (PVs) or fuel cells (FCs), DC distribution networks in data centers or electric vehicle (EV) charging stations and battery storage systems in uninterruptable power supplies (UPS) are just some examples for DC/DC converters applications [1].

Renewable energy sources such as PV and F.C. have low DC output voltage. Thus, high step-up DC-DC converter should be used in these systems [2]. Moreover, in order to track the maximum power point in these systems, the input current of the converter should be continuous with low ripple. Thus, the continuous low ripple input current is very essential for proper input power regulation [3].

In renewable energy systems, when galvanic isolation is not required, the conventional boost converter appears as the first choice. However, extreme duty ratio and consequently low efficiency are the main drawbacks at high output voltage gain [4-6]. Recently, several DC/DC converters have been proposed to increase the output voltage gain.

Switched inductors and switched capacitors structures are common as well [7-9]. The current stress on the main power devices is high in switched inductor structures while the high voltage stress is the main problem in switched capacitor based circuits [10]. Coupled inductor based boost converters are proposed to solve the aforementioned problems [12-22]. The leakage current of the coupled inductor is restored via active or passive clamps. Single switch coupled inductor based converters are also proposed in the literature. Since the leakage inductor of coupled inductors is very low, the input current is pulsating with an undesirable current ripple. The peak current of the leakage inductor passes through the main power switch which deteriorates the overall efficiency. In addition, continuity of the input current causes the RMS value of the input inductor and the switch currents to be reduced which increases the efficiency [6], [10]. By cascading boost converters, high output voltage gain can be achieved. However, too many components will be used in the circuit structures which increase the complexity of the circuit and decrease the total efficiency. Some other Sepic based converters are also presented recently [3], [6], [10]. However, these converters have low voltage gain.

In this paper, a novel high step-up continuous input current DC/DC converter is proposed. The presented converter benefits from numerous advantages such as high output voltage gain, low ripple continuous input current and lower voltage stress. The presented converter consists of a coupled-inductor, an inductor and an improved voltage multiplier cell. The circuit configuration of the proposed converter is shown in Fig. 1. As shown in this picture, capacitors C_3 and C_4 are charged by both sides of the coupled inductor. In conventional voltage multipliers, the capacitors are charged with the secondary side of the coupled inductor. Besides, the voltage stress on the output diode in the proposed converter is less

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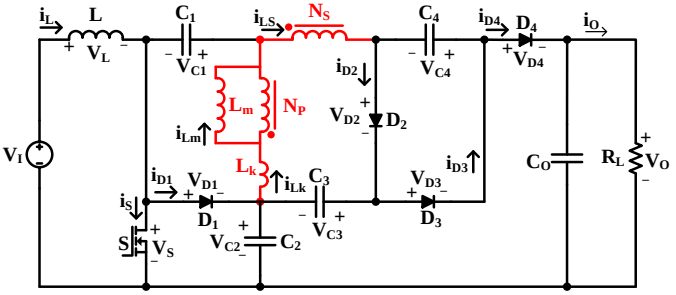

Fig. 1. The circuit prototype of the proposed converter

than other recently-proposed converters which helps solving reverse recovery problem. The voltage across the main switch is clamped by diode D_1 and capacitor C_1. This causes a switch with low on-resistance $R_{DS(on)}$ to be used in this converter which reduces the conduction loss. The operation principle of the proposed converter under steady state condition is discussed in the next section.

II. Operating Principle of the Proposed Converter

In order to simplify the operation principle analysis, it's assumed that: 1) all capacitors are large enough without any ripple in their voltages, all inductor L and L_m large enough without any ripple in their currents, 2) all components are ideal. The operation principle of the proposed converter in Continuous Conduction Mode (CCM) consists of five time intervals. The current flow path of the proposed converter in different modes and some waveforms of the components are depicted in Fig.2 and Fig. 3, respectively. The steady-state analysis of the presented converter is discussed as follows:

Mode I [t_0<t<t_1]: In this time interval, the switch is turned on. Diodes D_2 and D_4 are also on. The current of the leakage inductor is increased rapidly. The current equation of the leakage inductor is:

$$i_{Lk} = \frac{1}{L_K}\int_{t_0}^{t_1}\left(V_{C2} - V_{C1} + \frac{V_O - V_{C1} - V_{C4}}{n}\right)dt \qquad (1)$$

Where n is the turn ratio of the coupled inductor ($n=N_S/N_P$).

The voltage across the leakage inductor is high and also its inductance is very low. Thus, the slope of this current will be high. Therefore, this time interval is too small.

The secondary side current of the coupled inductor reaches zero when the currents of leakage and magnetizing inductor become equal. At this time, diodes D_2 and D_4 are turned off and this mode ends. By applying Kirchhoff Current Law (KCL), the switch current can be obtained as follow:

$$i_S = i_L + i_{Lk} - i_{Ls} \qquad (2)$$

Mode II [t_1<t<t_2]: In this time interval, the switch is on. As aforementioned, this mode begins when the currents of leakage and magnetizing inductor become equal. Thus, secondary side current of the coupled inductor reaches zero and diodes D_2 and D_4 are turned off. Once the current of the leakage inductor becomes more than the magnetizing inductor current, the direction of the secondary side current of the coupled inductor changes and turns diode D_3 on. Inductor L is charged by the input source. The magnetizing and leakage

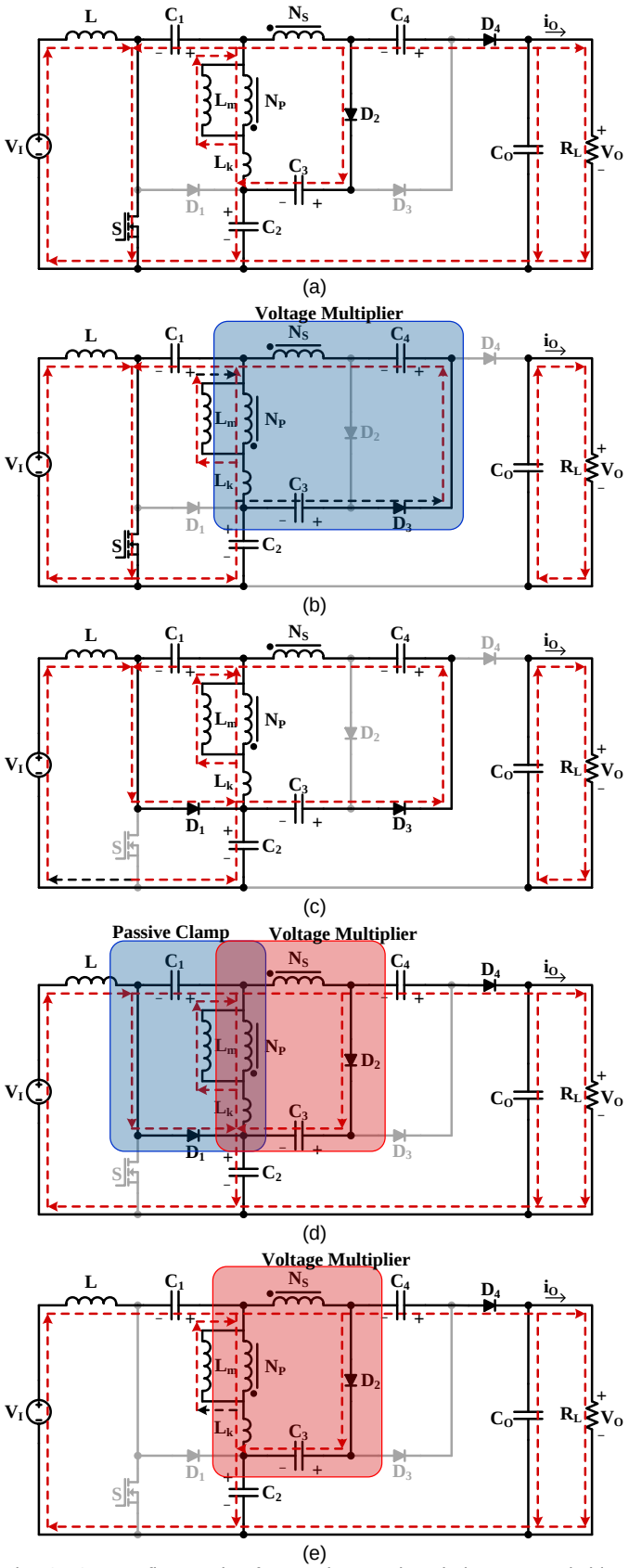

Fig. 2. Current-flow path of operating modes during one switching period at CCM operation. (a) Mode I. (b) Mode II. (c) Mode III. (d) Mode IV. (e) Mode V.

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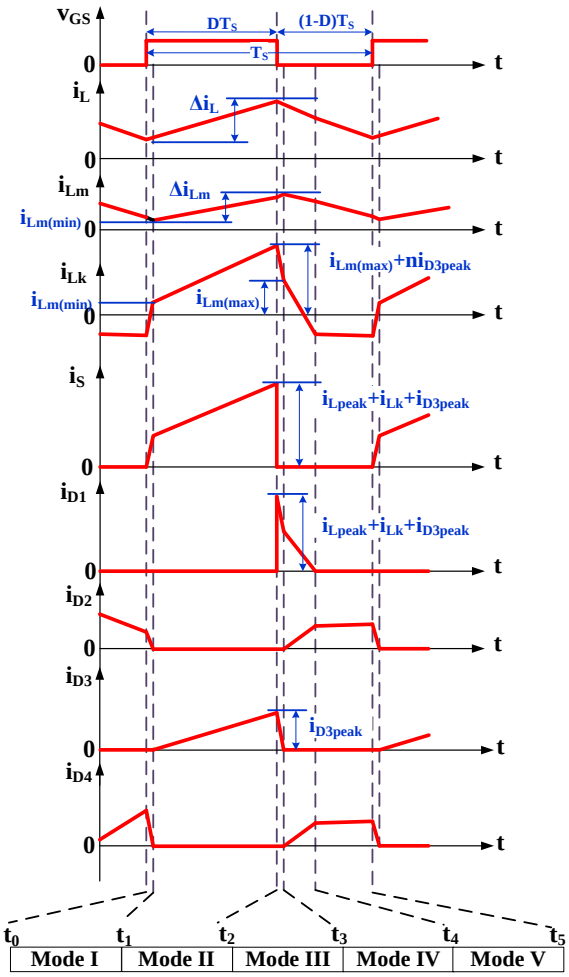

Fig. 3. Some typical waveforms of the proposed converter at CCM operation.

inductors and capacitor C_1 are charged by the energy stored in capacitor C_2. Capacitor C_3 and secondary side current of the coupled inductor charge capacitor C_4.

In this mode, the voltage of capacitor C_4 is equal to sum of capacitor voltage V_{C4} and both sides of the coupled inductor. The output capacitor provides energy to the load. This mode ends by turning the switch off. The following equation can be written for the capacitors currents.

$$\begin{cases} i_{C1} = -i_{C2} = (n+1)i_{D3} + i_{Lm} \\ i_{C4} = -i_{C3} = i_{D3} \end{cases} \quad (3)$$

By applying Kirchhoff Voltage Law (KVL) on the circuit, the following equations can be obtained.

$$V_L = V_I \quad (4)$$

$$V_{Lm} = V_{C2} - V_{C1} - V_{Lk2} \quad (5)$$

$$V_{C4} = V_{C3} + (n+1)(V_{C2} - V_{C1}) \quad (6)$$

Where, V_{Lk2} is the voltage across the leakage inductor L_k in mode II. The equation of the leakage inductor current can be written as follows:

$$V_{LK2} = \frac{\left(i_{Lk(t2)} - i_{Lk(t1)}\right)}{DT_S} L_K, \quad i_{Lk} = ni_{D3} + i_{Lm} \quad (7)$$

Mode III [t_2<t<t_3]: In this time interval, the switch is turned off. The current of inductor L flows through diode D_1 and charges capacitor C_2. The currents of diodes D_1 and D_3 can be written as follows:

$$i_{D1} = i_L + i_{Lk} - i_{Ls} \quad (8)$$

$$i_{D3} = -i_{Ls} \quad (9)$$

Where,

$$i_{Ls} = \frac{i_{Lm} - i_{Lk}}{n} \quad (10)$$

In this mode, the leakage inductor is demagnetized. Thus, the energy stored in the leakage inductor is recycled to capacitor C_1 through diode D_1. The following equation can be written for the leakage inductor:

$$i_{Lk} = \frac{1}{L_K} \int_{t_0}^{t_1} \left(\frac{V_{C3} - V_1 - V_{C4}}{n} - V_{C1} \right) dt \quad (11)$$

Because of high negative voltage across the inductor and low value of inductance, its current slope to be high and so causes this mode like mode I to be too small.

Mode IV [t_3<t<t_4]: In this time interval, diodes D_1, D_2 and D_4 are on. Recycling the energy of the leakage inductor is continued in this mode too. Once the leakage inductor current become smaller than the magnetizing inductor current, according to (9), the direction of the secondary side current of the coupled inductor is changed and turns diode D_2 and D_4 on. The capacitor currents in this mode can be found as follows:

$$\begin{cases} i_{C1} = -(I_L - i_{D1}) \\ i_{C4} = -i_{D4} = i_{C2} - I_L = -i_{Co} - I_O \\ i_{C3} = i_{D2} \end{cases} \quad (12)$$

Moreover, the following equation can be written for the currents of diodes D_1, D_2 and D_4 in this mode.

$$i_{D1} = i_L + i_{Lm} - (n+1)(i_{D2} + i_{D4}) \quad (13)$$

In conventional voltage multipliers, just the secondary side of the coupled inductors become in parallel with the capacitors. However, as seen in Fig. 2(d), in the proposed converter, both sides of the coupled inductor become in parallel with capacitor C_3. This makes the voltage across capacitor C_3 and as a result, the voltage gain to be increased. The voltage of capacitors in this mode can be found as follows:

$$V_L = V_I - V_{C2} \quad (14)$$

$$V_{Lm} = -V_{C1} - V_{Lk4} \quad (15)$$

$$V_O = V_{C2} + V_{C3} + V_{C4} \quad (16)$$

$$V_{C3} = (n+1)V_{C1} + nV_{Lk4} \quad (17)$$

Where V_{Lk4} is the voltage across the leakage inductor in mode IV which can be found as follow:

$$V_{LK4} = \frac{\left(i_{Lk(t4)} - i_{Lk(t3)}\right)}{d_4 T_S} L_K, \quad i_{Lk} = -ni_{D2} + i_{Lm} \quad (18)$$

Where, d_4T_S is time interval of mode IV.

Mode V [t_4<t<t_5]: This is the last time interval for a switching period. The energy of the leakage inductor has been

recycled to capacitor C_2 in modes III and IV. The energy of inductors and the input source charge the output capacitor and provide energy to the load through diode D_4. Diode D_2 is still on and capacitor C_3 is parallel with both sides of the coupled inductor. Applying KCL in this mode, yields:

$$i_{D2}=i_{D4}=i_{Ls}=\frac{i_{Lm}+i_L}{n+1},i_{Lk}=\frac{i_{Lm}-ni_L}{n+1} \tag{19}$$

It's worth noting that by neglecting current ripples of inductors L and L_m, the current slope of leakage inductor and diodes D_2 and D_4 are almost zero. Thus, the voltage across the leakage inductor in this mode is zero. It's worth noting that by assuming that the capacitors are large, the currents of diodes D_2 and D_4 are equal. The following equations can be achieved in this mod.

$$V_{Lm}=\frac{-V_{C3}}{n+1}=-V_{C1}-\frac{n}{n+1}V_{Lk4} \tag{20}$$

$$V_L=V_I-V_{C2}-\frac{n}{n+1}V_{Lk4} \tag{21}$$

By applying volt-second balance principle on the inductor voltages, the following equations can be obtained.

$$V_{C1}=\frac{DV_I}{1-D}-DV_{Lk2}-\left(\frac{n}{1+n}\right)\left(d_4+\frac{(1-D-d_4)}{(1-D)}\right)V_{Lk4} \tag{22}$$

$$V_{C2}=\frac{V_I}{1-D}-\frac{n(1-D-d_4)}{(n+1)(1-D)}V_{Lk4} \tag{23}$$

Neglecting modes I and III and by applying volt-second balance principle on the inductor L_K, the following equation is obtained.

$$DT_SV_{LK2}+d_4T_SV_{Lk4}+0=0\Rightarrow V_{Lk2}=-\frac{d_4}{D}V_{Lk4} \tag{24}$$

Using equations (6), (16), (17), (22), (23) and (24) the output voltage of the proposed converter can be obtained as follows:

$$V_O=MV_I+\left((n+1)(d_4+D)+\frac{n}{n+1}(Md_4-(1-D))\right)V_{Lk4} \tag{25}$$

Where M is the voltage gain of the proposed converter by neglecting the leakage inductor (L_k=0, V_{Lk4}=0). The value of M is:

$$M=\frac{n+2+D(n+1)}{1-D} \tag{26}$$

This equation can be found by using equations (6), (16), (17), (22) and (23) and also by considering the leakage inductor and its voltages to be zero. In order to find the voltage gain of the proposed converter without neglecting leakage inductance, the V_{Lk2} and V_{Lk4} should be found. By applying ampere-second balance principles on the capacitors, it can be proved that the average values of diode currents are equal to the output current. According to Fig. 3, the average values of diode D_3 can be achieved.

$$<i_{D3}>=I_O\Rightarrow Di_{D3peak}=2I_O\Rightarrow i_{D3peak}=\frac{2I_O}{D} \tag{27}$$

Neglecting the leakage inductor and power loss yields:

$$I_L=MI_O \tag{28}$$

Applying ampere-second balance principle on capacitor C_1, the average value of I_{Lm} can be found.

$$<i_{C1}>=DI_{Lm}+(n+1)I_O+I_O-DI_L=0\Rightarrow I_{Lm}=(n+1)I_O \tag{29}$$

The value of d_4 can be found as follows:

$$<i_{D1}>=I_O=\frac{(I_L+I_{Lm})d_4T_S}{2T_S}=\frac{(M+(n+1))d_4I_OT_S}{2T_S}\Rightarrow d_4=\frac{2(1-D)}{2n+3} \tag{30}$$

Substituting (27) into (7) and using equation (24), the value of V_{Lk4} can be obtained as follows:

$$V_{Lk4}=-\frac{n(2n+3)Q}{D(1-D)}V_O,Q=\frac{f_SL_K}{R_L} \tag{31}$$

The voltage of capacitors C_3 and C_4 and the voltage gain can be found as well.

$$V_{C3}=\frac{(n+1)D}{1-D}V_I+\left[n+\frac{2D+1-2n}{(2n+3)}\right]V_{Lk4} \tag{32}$$

$$V_{C4}=\frac{(n+1)}{1-D}V_I+\left[n+\frac{4D-1-2n}{(2n+3)}+\frac{2n(1-D)}{D(2n+3)}\right]V_{Lk4} \tag{33}$$

$$G_{CCM}=\frac{MD^2(1-D)}{D^2(1-D)-2[A]nQ} \tag{34}$$

$$A=D^2(2n^3+9n^2+10n+2)+nD(2n+6)-n$$

Where, G_{CCM} is the voltage gain of the proposed converter. According to equation (34), if L_K=0, the value of Q will be zero and the voltage gain will be equal to equation (26).

III. Converter design Consideration

In order to operate a converter properly, its components should be designed appropriately. Therefore, design of the components for the proposed converter is discussed here. Since operating in Discontinuous Conduction Mode (DCM) has some disadvantages such as slow dynamic response, dependence on frequency the output power and the value of inductors and also high current stress on the semiconductors, the proposed converter should be designed to operate under CCM condition. According to [9], [23], [24], if the average current value of the inductor is more than half of its ripple, the converter will operate in CCM. The current ripple of inductors L and L_m can be obtained using integral formula of inductors.

$$\Delta i_L=\frac{DV_I}{Lf_S} \tag{35}$$

$$\Delta i_{Lm}=\frac{DV_I}{L_mf_S} \tag{36}$$

Therefore, the minimum value of inductor L in order to operate in CCM can be achieved as follows:

$$L\geq\frac{DR_L}{2M^2f_S} \tag{37}$$

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In order to operate the proposed converter in CCM, the value of L_m is also should be calculated and designed properly. If the proposed converter operates in Boundary Conduction Mode (BCM), at the end of the switching period, the inductor currents i_L and i_{Lm} will be equal. Thus:

$$i_{L\min} = -i_{Lm\min} \Rightarrow I_{Lm} - \frac{\Delta i_{Lm}}{2} = \frac{\Delta i_L}{2} - I_L \tag{38}$$

Therefore, if the following inequality is valid, the proposed converter will operate in CCM.

$$i_{L\min} = -i_{Lm\min} \Rightarrow I_{Lm} - \frac{\Delta i_{Lm}}{2} \geq \frac{\Delta i_L}{2} - I_L \tag{39}$$

Using equations (28), (29), (35), (36) and (39), the minimum value of inductor L_m can also be calculated using the following equation:

$$L_m \geq \frac{2L(1-D)R_L}{2D(1-D)R_L - 4(2n+3)f_S ML} \tag{40}$$

Ignoring the ESR of capacitors, the voltage ripple of the output capacitor can be found as follows:

$$\begin{aligned} V_{Co}(DT_S) &= V_{Co}(0) + \frac{1}{C_O}\int_0^{DT_S} i_{Co}(t)dt \\ \Rightarrow \Delta V_{Co} &= \frac{DV_O}{f_S R_L C_O} \end{aligned} \tag{41}$$

Using this equation and considering certain voltage ripple, the output capacitor value can be found.

According to Fig. 2, the voltage stress on the semiconductors can be written as follows:

$$V_{D1} = V_S = V_{C2} = \frac{V_I}{1-D} \tag{42}$$

$$V_{D2} = V_{D3} = V_{D4} = V_{C4} = \frac{(n+1)V_I}{1-D} \tag{43}$$

The current stress on diode D_3 is calculated in equation (27). The current stress on the switch and diodes can be achieved as follows:

$$i_{Speak} = i_{D1peak} = i_L + i_{Lk} + i_{D3} = \left(\frac{2(n+1)}{D} + \frac{2n+3}{1-D}\right)I_O \tag{44}$$

$$I_O = \frac{(2(1-D)-d_4)i_{D2,4peak}}{2} \Rightarrow i_{D2,4peak} = \frac{(2n+3)I_O}{2(n+1)(1-D)} \tag{45}$$

IV. Comparison Study

In this session, some comparisons between the suggested converter and other recently-proposed converters are presented. The specifications of the converters are compared in Table I. The voltage gain and voltage stress on the main switch are compared in Fig. 4 and Fig. 5, respectively. The proposed converter has continuous and low-ripple input current. Thus it will be more suitable for renewable energy applications.

For instance, in some applications such as fuel cell (F.C.) which has slow dynamic response, the converters which have high input current ripple cannot operate properly. In order to solve this problem, an input filter is required which increase the number of components. The voltage gain of the proposed converter and some other recently-proposed converters are compared in Fig. 4. As shown in this figure, the voltage gain of the presented converter is higher than other converters. Besides, the voltage stress on the main switch in the proposed converter is lower than other converters. Comparing Fig. 4 and Fig. 5 yields that the voltage stress on the switch for the converter with higher voltage gain is less that the others.

V. Experimental Results

In order to validate the theoretical analysis and justify the feasibility of the proposed converter, the experimental results of implemented circuit of the proposed converter are analyzed in this session. The specifications of the implemented prototype are given in Table II. The proposed converter increases the input voltage of 20V to output voltage of 300V at the output power of 245W. The voltage of capacitors and semiconductors and the currents of inductor and semiconductors are shown in Fig. 6. The time per division in the figures is 10μs. Under this condition and according to equations (37) and (40), the minimum values of inductors can be calculated to operate the converter in CCM.

Table I. The comparison between the proposed converter and some other converters.

	Number of Components				Voltage Stress on Switch	Voltage Gain	Current Stress on Switch	$\sum V_D$
Reference	diode	switch	capacitor	core				
Proposed Converter	4	1	4	2	$\frac{M+n+1}{2n+1}V_I$	$\frac{n+2+(n+1)D}{1-D}$	$\left(\frac{2(n+1)}{D}+\frac{2n+3}{1-D}\right)I_O$	$\frac{(3n+5)(M+n+1)}{2n+1}V_I$
Converter in [10]	3	1	3	2	$\frac{M}{n+2}V_I$	$\frac{n+2}{1-D}$	$MI_O+\left(\frac{2(n+1)}{D}\right)I_O$	$\frac{M(2n+3)}{n+2}V_I$
Converter in [3]	3	1	3	2	$\frac{M}{n+1}V_I$	$\frac{n+1}{1-D}$	$\left(\frac{2nM}{M-n-1}+M\right)I_O$	$\frac{M(2n+1)}{n+1}V_I$
Converter in [11]	4	1	3	1	$\frac{M-n}{n+1}V_I$	$\frac{n+1+nD}{1-D}$	$\left(\frac{(2n+1)(M-n)}{1+n}+\frac{2n(M-n)}{M-2n-1}\right)I_O$	$\frac{(M-n)(3n+1)}{n+1}V_I$
Converter in [9]	4	1	3	1	$\frac{M+n}{2(n+1)}V_I$	$\frac{n+2+nD}{1-D}$	$\frac{M(M+n)}{M-n-2}I_O$	$\frac{3}{2}(M+n)V_I$

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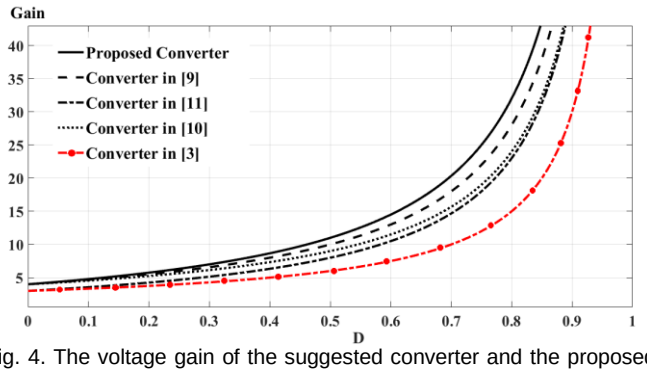

Fig. 4. The voltage gain of the suggested converter and the proposed converters in [3], [9], [10] and [11] (n=2)

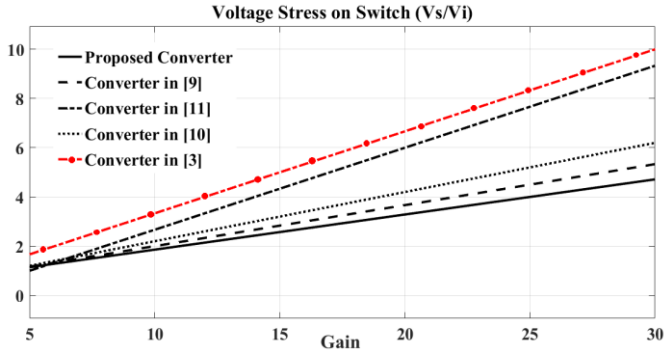

Fig. 5. The voltage stress on the main switch for the suggested converter and the proposed converters in [3], [9], [10] and [11] (n=2).

However, in this condition, the converter will operate near DCM which is caused the current ripples and stresses to be high. Thus, in order to design the inductors properly, the current ripples are considered to be less than 10% of their average. According to equations (35) and (36), the value of inductor L is chosen 320μH. The value of L_m can also be chosen as well.

For the voltage gain calculation, some assumptions are considered to simplify the analysis. For instance, the voltage forward of the diodes and resistances of components are neglected. Thus the calculated voltage gain of the proposed converter will be different from the measured voltage gain. However, considering them does not increase the duty ratio very much. According to equation (34), the duty ratio of the proposed converter for the input and output voltage of 20V and 300V is about 62%. However, according to Fig. 6, the duty ratio of the power switch is about 65%.

As shown in Fig. 6, the input current is about 13.1 A. The output power is 245 W. Therefore, the efficiency of the proposed converter under the output power of 245 W is about 93.5%. The efficiency curve of the proposed converter versus the output power is depicted in Fig. 7.

Table II. The circuit parameters of the implemented prototype.

Specifications	Values
Input Voltage	20V
Output Voltage	300V
Capacitors	C_1, C_2, C_3, C_4=47 μF, C_O=180 μF
Inductor (L)	320 μH
Coupled-inductor	L_m=100 μH, n=2
Switching frequency	50kHz
Power Switches	IRFP260
Diodes	MUR1560

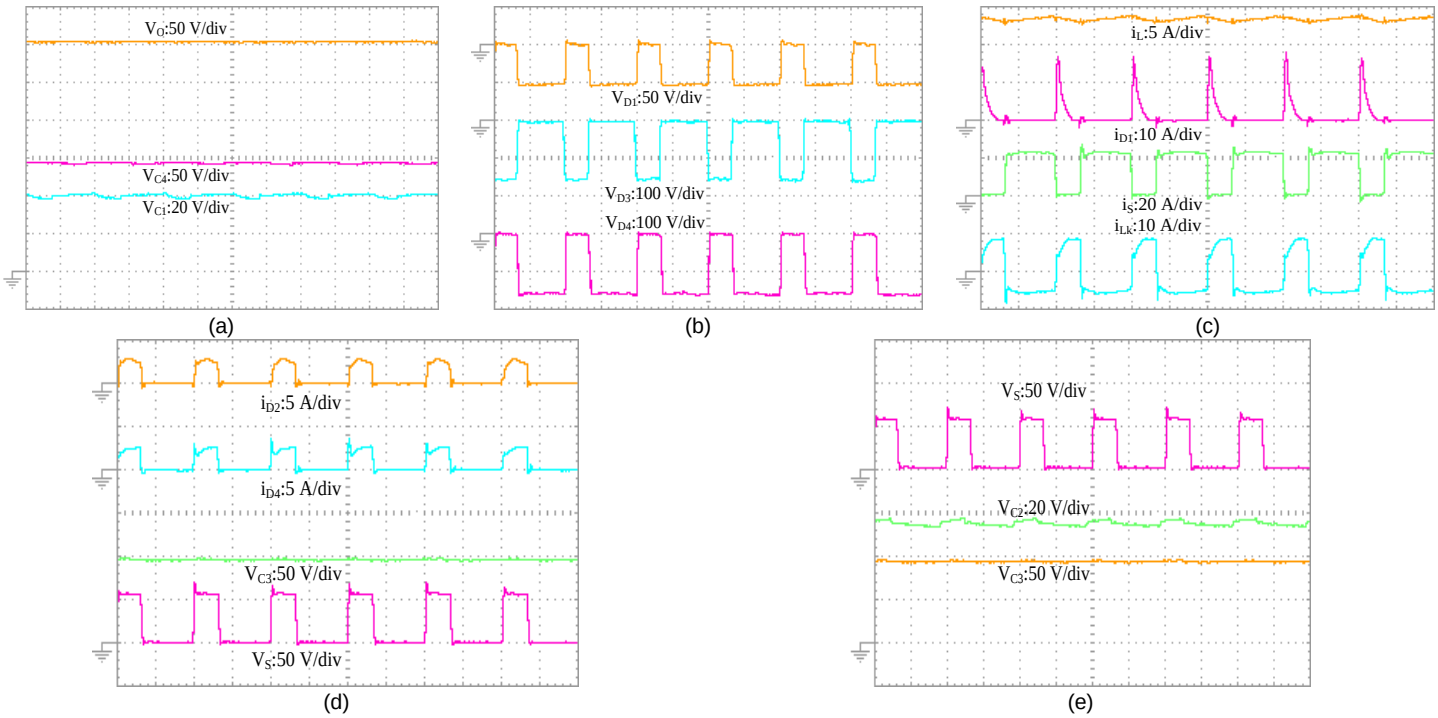

Fig. 6. Experimental results of the proposed converter.

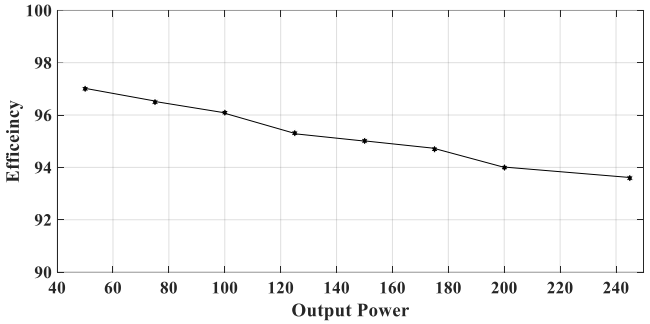

Fig. 7. Efficiency curve of the proposed converter versus various output power.

VI. Conclusion

A high step-up DC-DC converter is studied in this paper. The proposed converter has high voltage gain and continuous and low-ripple input current. A passive voltage clamp and two voltage multipliers are added to the converter to achieve high voltage gain. This cause the number of components to be high. Besides, the power is transferred to the load with some steps from input to output. These causes high conductions in the proposed converter. Since both sides of the coupled inductor charge the capacitors of voltage multipliers, the voltage gain of the proposed converter in comparison other converters with same number of components to be higher. Thus, higher voltage gain can be achieved with low duty ratio. The steady state analysis of the proposed converter is discussed in this paper. The voltage gain, voltage stress on the main switch and also sum of voltage stress on diodes and the current stress on the main switch are compared between the proposed converter and other converters. According to the presented results, the voltage stress on main switch in suggested converter is less than other converters. Finally, the presented topology is implemented experimentally under the output power of 245W in order to justify the theoretical analysis.

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