4

POWER CONVERTERS IN WIND ENERGY CONVERSION SYSTEMS

4.1 INTRODUCTION

Power converters are widely used in wind energy conversion systems (WECS). In fixed-speed WECS, the converters are used to reduce inrush current and torque oscillations during the system start-up, whereas in variable-speed WECS they are employed to control the speed/torque of the generator and also the active/reactive power to the grid [1]. According to the system power ratings and type of wind turbines, a variety of power converter configurations are available for the optimal control of wind energy systems.

Figure 4-1 illustrates three practical wind energy conversion systems using different power converter configurations. Figure 4-1a shows the fixed-speed, induction-generator-based WECS, in which a soft starter is employed to reduce inrush current caused by electromagnetic transients that take place at the moment the generator is connected to the grid. The soft starter is essentially an AC voltage controller using SCR devices, whose output voltage is adjusted such that it increases slowly with time during the system start-up. Figure 4-1b shows a variable-speed WECS using squirrel cage induction generators (SCIGs) or synchronous generators (SGs), where a back-to-back converter configuration with two identical PWM converters is used. The converters can be either voltage source converters (VSCs) or current source converters (CSCs). Figure 4-1c is also a variable-speed wind energy system only for synchronous

Power Conversion and Control of Wind Energy Systems. By B. Wu, Y. Lang, N. Zargari, and S. Kouro

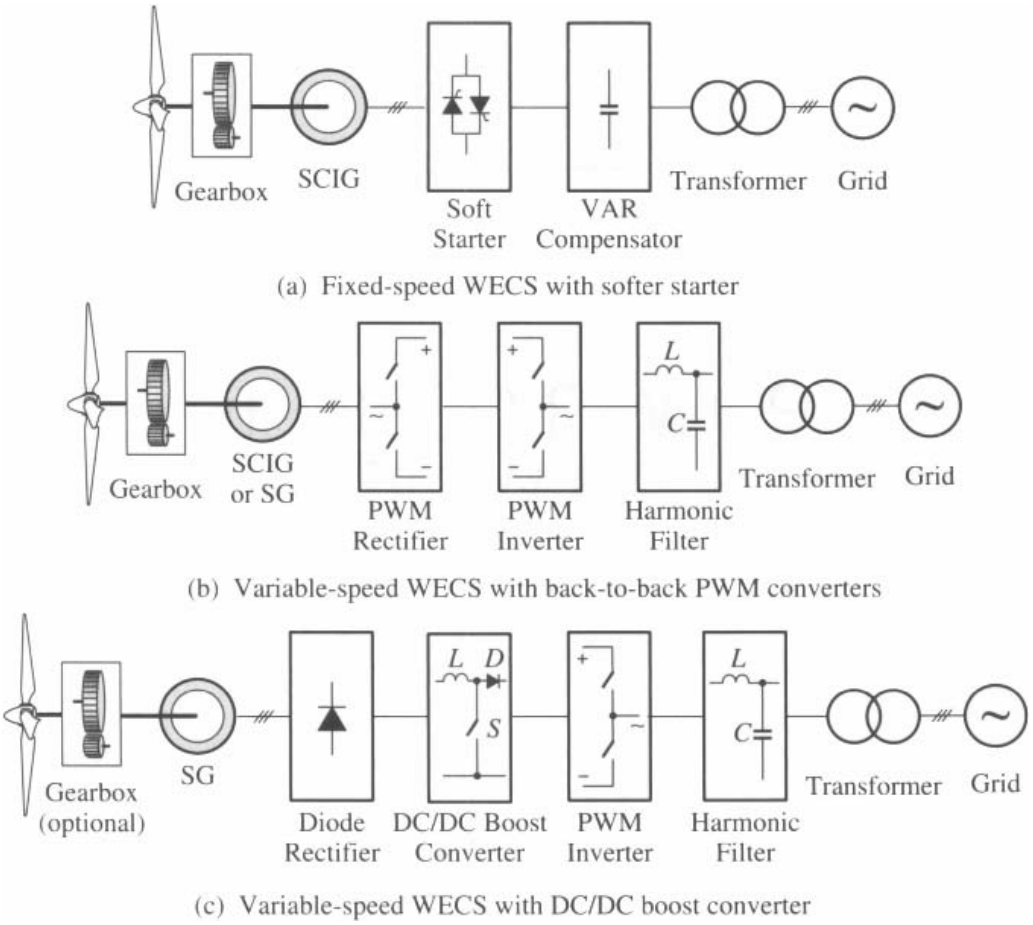


Figure 4-1. Three typical WECS using different power converter topologies.

generators, where a low-cost diode rectifier with a DC/DC boost converter can be used instead of the PWM rectifier.

In this chapter, different power converter topologies for wind energy systems are introduced, their operating principles are discussed, and switching schemes are elaborated. These converters include AC voltage controllers, DC/DC boost converters, two-level voltage source converters, three-level neutral point clamped (NPC) converters, and PWM current source converters [2]. Finally, the control of grid-connected converters is presented. The equations and tables derived in this chapter will be used to assist in the analysis of wind energy systems in the subsequent chapters.

4.2 AC VOLTAGE CONTROLLERS (SOFT STARTERS)

The AC voltage controller is often referred to as soft starter in WECS since its main function is to help the wind turbine to start smoothly with reduced inrush current and mechanical stress. After the system is started, the AC voltage controller is usually bypassed (short circuited) by a bypass switch, which eliminates the power losses of the controller. The AC voltage controllers in WECS normally use a SCR (thyristor) as

switching device. Through the delay (firing) angle control for the SCRs, the output voltage of the controller can be adjusted from zero all the way up to its supply voltage, which effectively reduces the starting current of the system. This section starts with an introduction to the single-phase AC voltage controller, followed by detailed studies for three-phase AC voltage controllers.

4.2.1 Single-Phase AC Voltage Controller

The simplified circuit for a single-phase AC voltage controller is shown in Figure 4-2. It is composed of a pair of SCR thyristors, connected in antiparallel between the power supply and the load. The operating principle of the voltage controller, the gating arrangement for the thyristors, and the resultant output voltage and current waveforms are illustrated in Figure 4-3.

Assuming a resistive load, the waveforms for the gate signals i_{g1} and i_{g2}, output current i_o, and output voltage v_o of the controller with a delay angle of $\alpha = \pi/3$ are given in Figure 4-3a. During the positive half-cycle of the power supply, thyristor T_1 is turned on at $\omega t = \alpha = \pi/3$ by i_{g1} and is turned off at π when its current falls to zero. During the negative half-cycle, thyristor T_2 is triggered on at $\omega t = (\alpha + \pi) = 4\pi/3$ and is switched off at 2π.

With a resistive load, the rms value of the output voltage V_o can be found from

$$V_o = \left(\frac{1}{\pi}\int_{\alpha}^{\pi}(\sqrt{2}V_s \sin\omega t)^2 d(\omega t)\right)^{1/2} = V_s\left(1 - \frac{\alpha}{\pi} + \frac{\sin 2\alpha}{2\pi}\right)^{1/2} \tag{4.1}$$

Figure 4-3b illustrates the operation of the voltage controller with an RL load and $\alpha = \pi/3$. Thyristor T_1 is turned on at $\omega t = \pi/3$, but will not be turned off when the supply voltage v_s falls to zero at $\omega t = \pi$. This is due to the lagging inductive load current flowing through T_1, which is not yet zero at $\omega t = \pi$. Thyristor T_1 remains on until its current becomes zero, at which the energy stored in the load inductance is fully released and, thus, T_1 is turned off.

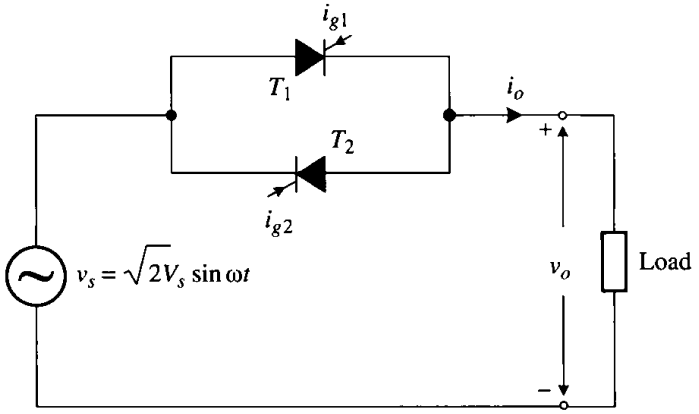


Figure 4-2. Single-phase AC voltage controller.

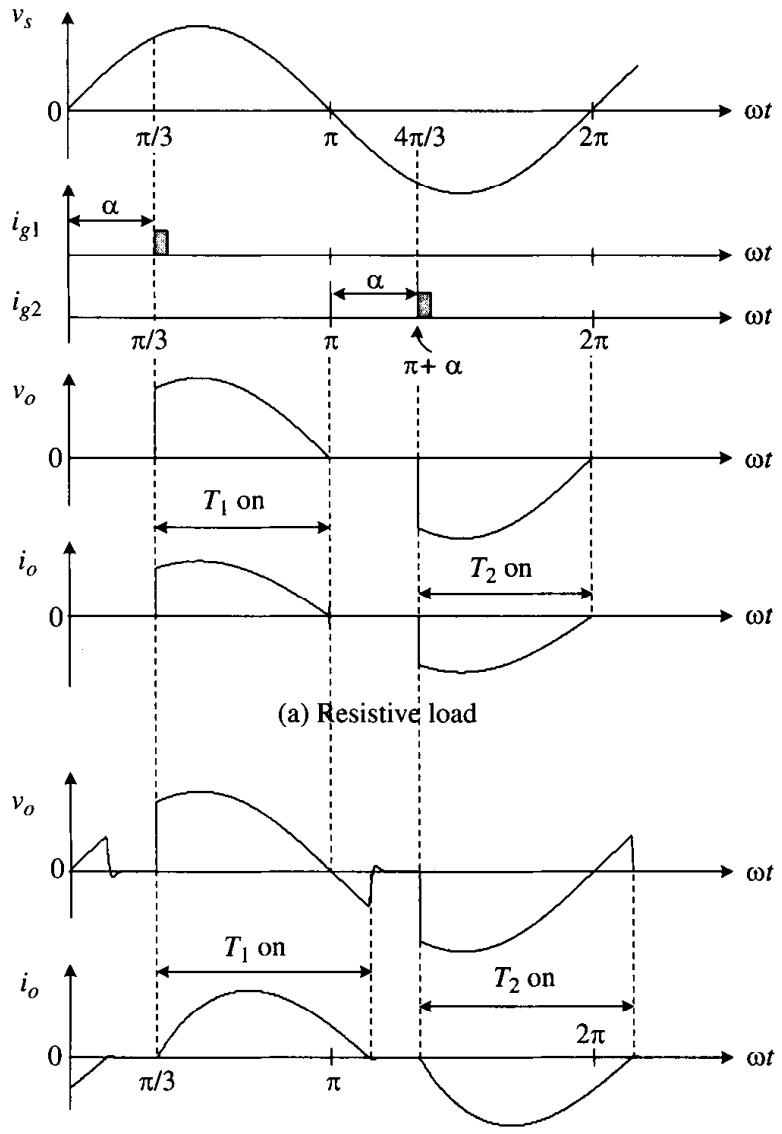


Figure 4-3. Waveforms for the single-phase AC voltage controller.

It is noted that when the delay angle α is smaller than the load power factor angle φ, defined by $\varphi = \tan^{-1}(\omega L/R)$, the output voltage v_o of the controller will be equal to its input supply voltage v_s and, thus, v_o is no longer adjustable. Take Figure 4-4 as an example, where the load power factor angle φ is $\pi/3$ and delay angle a is $\pi/6$. During the positive half-cycle of the supply voltage, thyristor T_1 conducts for a certain period of time. When the gate signal for T_2 arrives at $\omega t = \pi + \alpha$, T_2 will not be turned on since the load current i_o is still positive due to the inductive load and, thus, T_1 continues to conduct. T_2 will be turned on only when i_o falls to zero and becomes negative, provided that the gate current i_{g2} for T_2 is still there. When T_2 is turned on, T_1 is reverse biased and, thus, turned off. Both T_1 and T_2 conduct 180° alternatively per the fundamental-frequency cycle and, thus, the output voltage v_o is equal to the supply voltage v_s.

It is also noted that with an inductive load, continuous gating with extended duration, such as i_{g1} and i_{g2} in Figure 4-4, should be used. If the gate signals are of short duration, the controller will not operate properly. For instance, with a short gating pulse i_{g2}, like the one shown with a solid block in the figure, T_2 will not be turned on during the negative cycle of the supply voltage.

Assuming a pure inductive load, the rms value of the output voltage v_o of the controller can be calculated by

$$V_o = \begin{cases} V_s & \text{for } 0 \le \alpha < \pi/2 \\ V_s\left(2 - \dfrac{2\alpha}{\pi} + \dfrac{\sin 2\alpha}{\pi}\right)^{1/2} & \text{for } \pi/2 \le \alpha \le \pi \end{cases} \tag{4.2}$$

where V_o is equal to V_s for $0 \le \alpha < \pi/2$ due to the reasons discussed earlier.

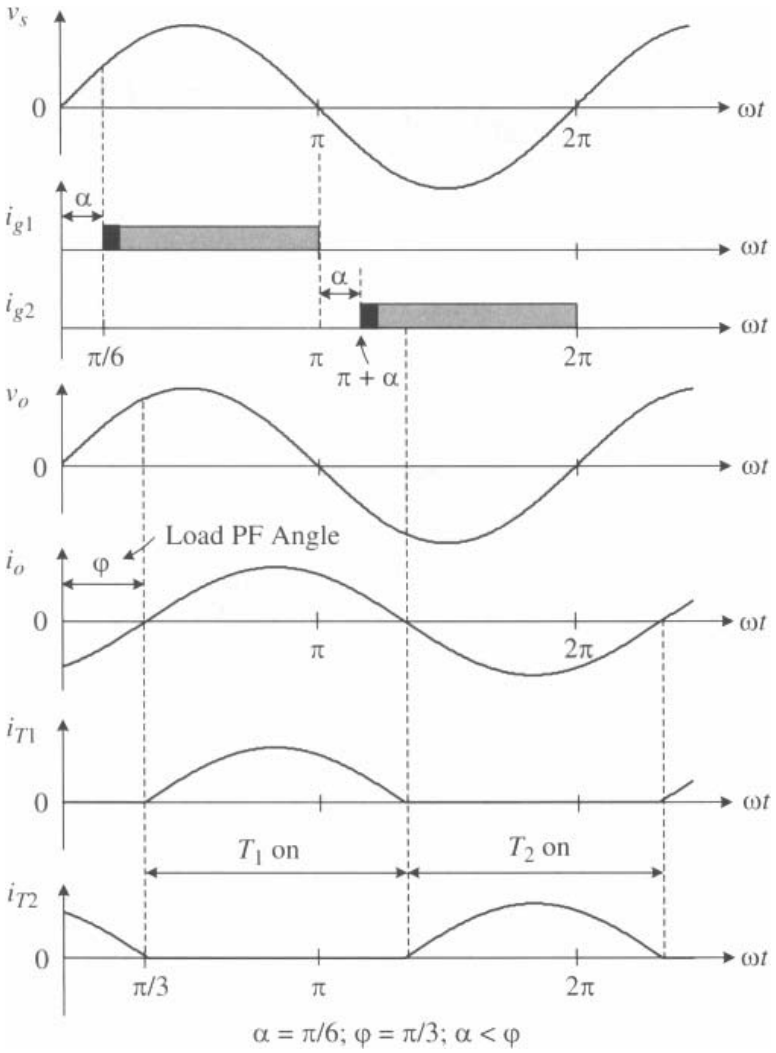


Figure 4-4. Waveforms for single-phase AC voltage controller with an RL load.

Based on Equations (4.1) and (4.2), the relationship between the voltage ratio V_o/V_s and delay angle α with a pure resistive ($\varphi = 0$) and pure inductive ($\varphi = 90°$) load is drawn in Figure 4-5. The other curves in the figure for load power factor angle of φ 45°, 60°, and 75° are obtained by computer simulation.

4.2.2 Three-Phase AC Voltage Controller

The configuration of a three-phase AC voltage controller with a three-phase Y-connected load is shown in Figure 4-6. It is composed of three pairs of SCR thyristors connected between the three-phase power supply and the load. The operating principle of the controller is illustrated in Figure 4-7, where the waveforms for the supply voltages, thyristor gating currents, and phase-*a* load voltage v_{an} are illustrated.

Consider a three-phase, balanced, Y-connected resistive load for the controller. During period I, thyristors T_6 and T_1 are turned on, and the line-to-line supply voltage v_{AB} is applied to the phase-*a* and *b* load resistors. Since T_5 and T_2 in phase-*c* are both off, the phase-*a* load voltage v_{an} is equal to $v_{AB}/2$ as shown in Figure 4-7. For period II, thyristors T_1 and T_2 conduct, leading to $v_{an} = v_{AC}/2$. During period III, thyristors T_2 and T_3 are turned on, but none of the phase-*a* thyristors is on, resulting in $v_{an} = 0$. Following the same procedure, the load voltage v_{an} during the negative half-cycle can be drawn. Similarly, the load voltage waveforms for the other two phases, v_{bn} and v_{cn}, can be determined.

The waveforms for the load line-to-line voltages can be obtained by $v_{ab} = v_{an} - v_{bn}$, $v_{bc} = v_{bn} - v_{cn}$, and $v_{ca} = v_{cn} - v_{an}$, respectively. Figure 4-8 shows the waveforms for v_{an} and v_{ab} with the delay angle changes from $2\pi/3$ to zero in steps. It can be observed that

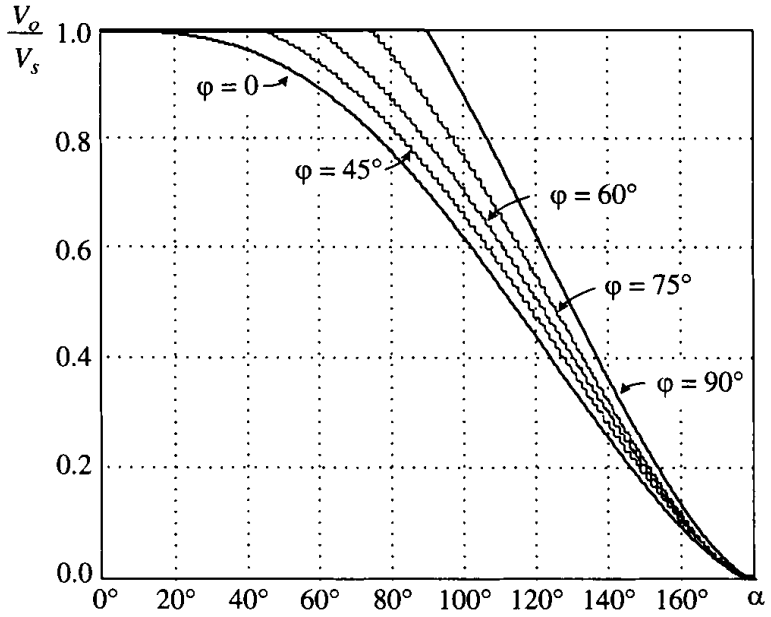


Figure 4-5. Output voltage to supply voltage ratio V_o/V_s versus delay angle α for single-phase AC voltage controller.

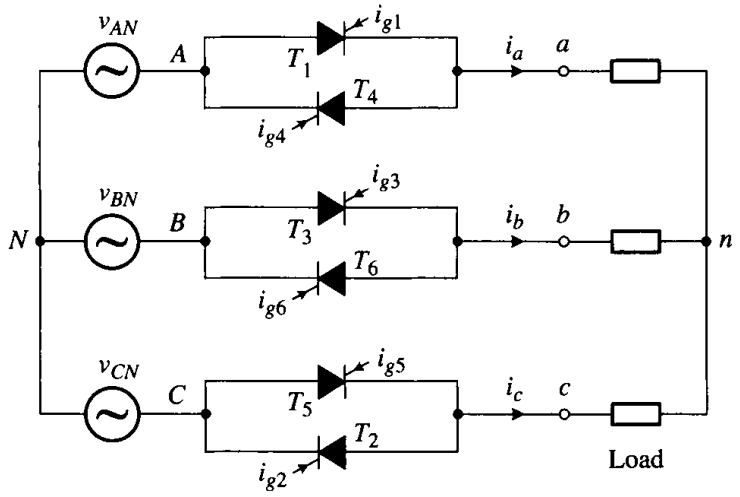


Figure 4-6. Three-phase AC voltage controller with Y-connected load.

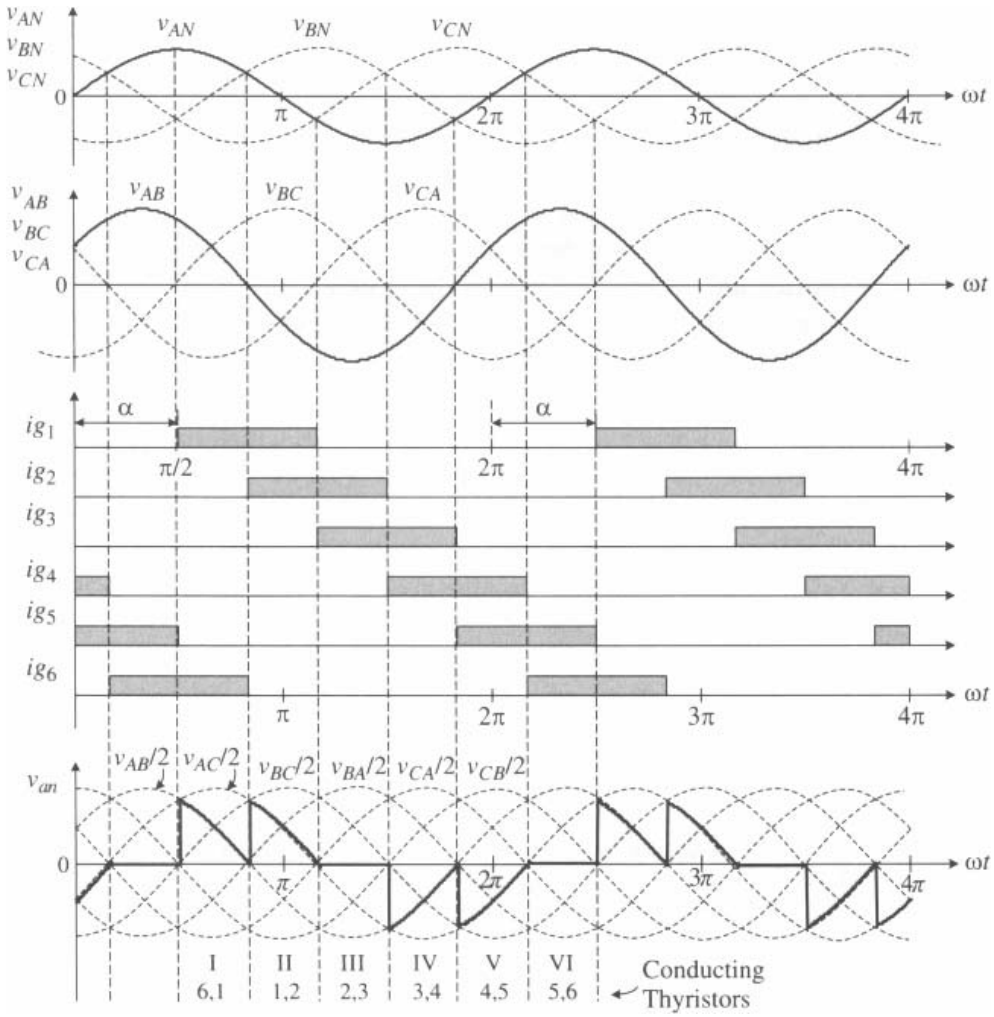


Figure 4-7. Waveforms of three-phase AC voltage controller with a Y-connected resistive load.

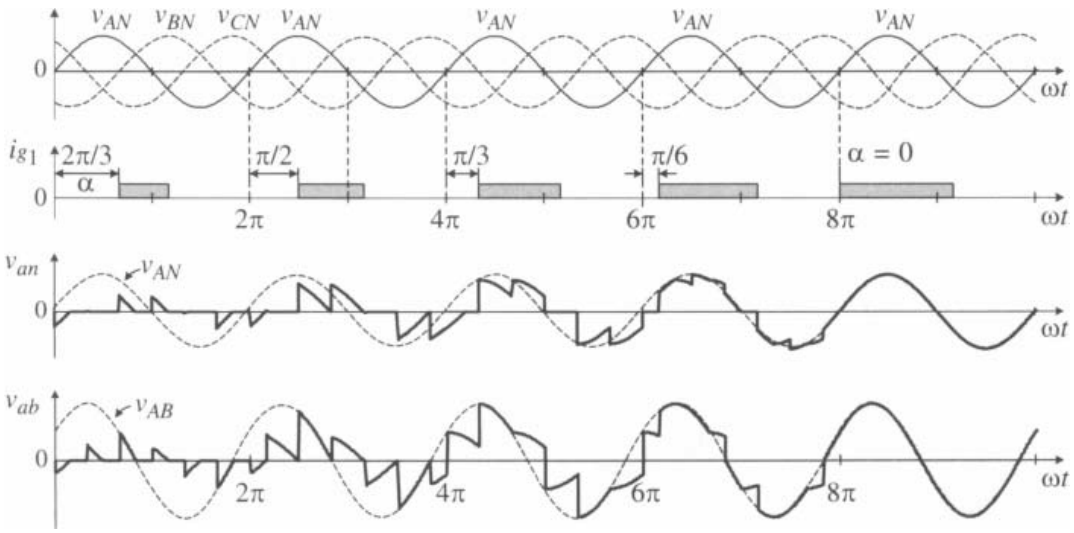


Figure 4-8. Waveforms of three-phase AC voltage controller with a resistive load and various delay angles. Delay angle: $\alpha = 2\pi/3$ (first cycle), $\pi/2$ (second cycle), $\pi/3$ (3rd cycle), $\pi/6$ (fourth cycle) and 0 (fifth cycle).

with the decreasing of delay angle, the load phase voltage v_{an} and line-to-line voltage v_{ab} increase accordingly, and, finally, are equal to the phase voltage v_{AN} and line-to-line voltage v_{AB} of the power supply at $\alpha = 0$, respectively.

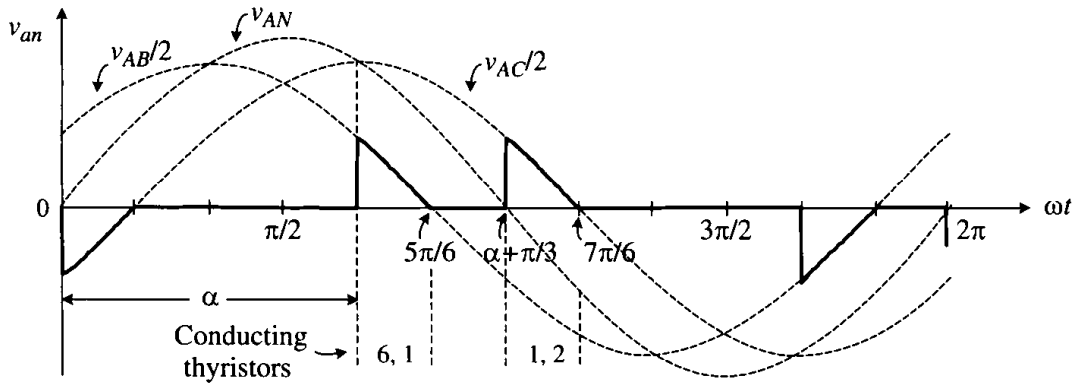
Depending on the delay angle α, the operation of the three-phase AC voltage controller can be classified into three operating modes: Mode I for $\pi/2 \leq \alpha < 5\pi/6$, during which there are periods when none or two thyristors in each phase conduct; Mode II for $\pi/3 \leq \alpha < \pi/2$, during which two thyristors in each phase are turned on; and Mode III for $0 \leq \alpha < \pi/3$, during which three thyristors or two thyristors conduct simultaneously [4]. Unlike the single-phase AC voltage controller, in which the delay angle α is in the range of zero to π, the range of the three-phase AC voltage controller is from zero to $5\pi/6$ (150°), beyond which ($5\pi/6 < \alpha \leq \pi$) the output voltage of the controller is kept to zero. Therefore, there is no need to extend the delay angle beyond $5\pi/6$.

The typical waveforms of v_{an} for the voltage controller operating in the these three modes are shown in Figure 4-9, where the delay angle α is $2\pi/3$ (120°) in Mode I, $5\pi/12$ (75°) in Mode II, and $\pi/6$ (30°) in Mode III, respectively.

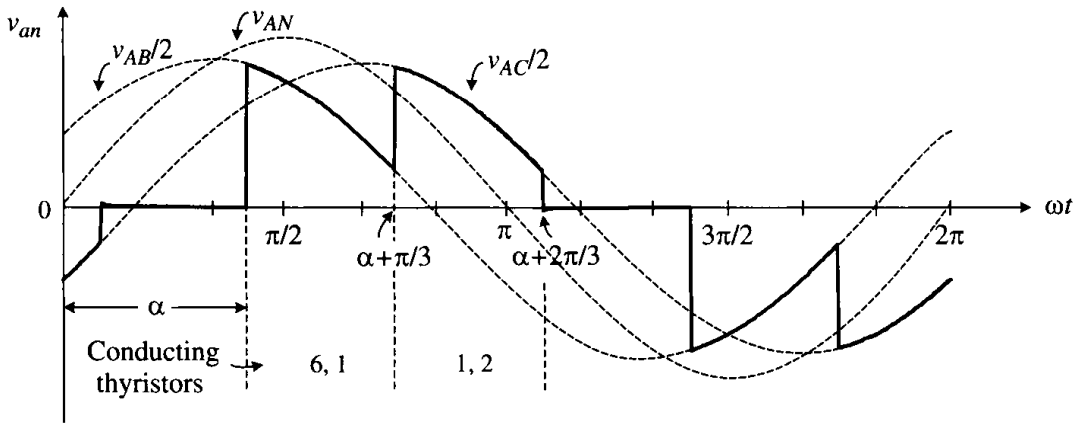
Based on the waveforms given in Figure 4-9, the rms value of the load phase voltage can be calculated by

$$V_{an} = \left(\frac{1}{\pi} \left(\int_{\alpha}^{5\pi/6} \left(\frac{\sqrt{6}}{2} V_s \sin(\omega t + \pi/6) \right)^2 d(\omega t) + \int_{\alpha+\pi/3}^{7\pi/6} \left(\frac{\sqrt{6}}{2} V_s \sin(\omega t - \pi/6) \right)^2 d(\omega t) \right) \right)^{1/2}$$

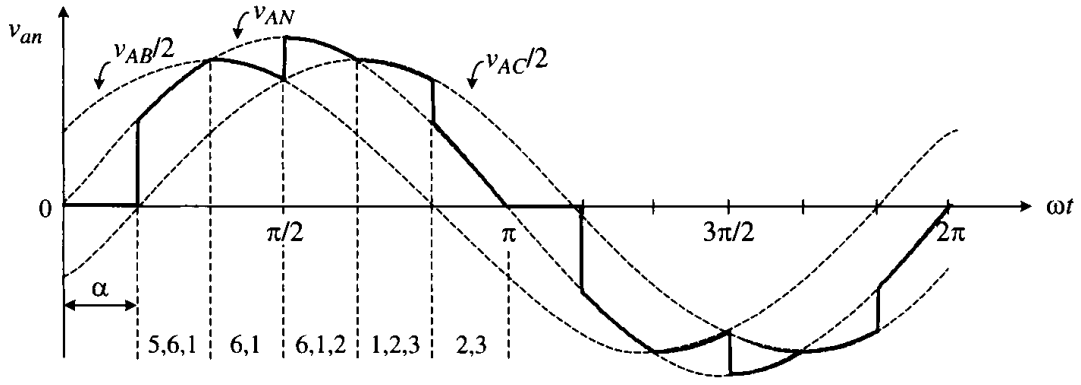
$$= V_s \left(\frac{5}{4} - \frac{3\alpha}{2\pi} + \frac{3\sin(2\alpha + \pi/3)}{4\pi} \right)^{1/2} \qquad \text{for Mode I } (\pi/2 \leq \alpha < 5\pi/6) \tag{4.3}$$



(a) α = 2π/3(120°, Mode I)



(b) α = 5π/12 (75°, Mode II)



(c) α = π/6(30°, Mode III)

Figure 4-9. Typical waveforms of v_{an} when the three-phase controller operates in three different modes with a resistive load.

$$V_{an} = \left(\frac{1}{\pi} \left(\int_{\alpha}^{\alpha+\pi/3} \left(\frac{\sqrt{6}}{2} V_s \sin(\omega t + \pi/6) \right)^2 d(\omega t) + \int_{\alpha+\pi/3}^{\alpha+2\pi/3} \left(\frac{\sqrt{6}}{2} V_s \sin(\omega t - \pi/6) \right)^2 d(\omega t) \right) \right)^{1/2}$$

$$= V_s \left(\frac{1}{2} + \frac{3\sqrt{3}}{4\pi} \sin(2\alpha + \pi/6) \right)^{1/2} \qquad \text{for Mod e II } (\pi/3 \le \alpha < \pi/2) \tag{4.4}$$

and

$$V_{an} = \left(\frac{1}{\pi} \left(\int_{\alpha}^{\pi/3} (\sqrt{2} V_s \sin \omega t)^2 d(\omega t) + \int_{\pi/3}^{\alpha+\pi/3} \left(\frac{\sqrt{6}}{2} V_s \sin(\omega t + \pi/6) \right)^2 d(\omega t) \right. \right.$$

$$+ \int_{\alpha+\pi/3}^{2\pi/3} (\sqrt{2} V_s \sin \omega t)^2 d(\omega t) +$$

$$\left. \left. \int_{2\pi/3}^{\alpha+2\pi/3} \left(\frac{\sqrt{6}}{2} V_s \sin(\omega t - \pi/6) \right)^2 d(\omega t) + \int_{\alpha+2\pi/3}^{\pi} (\sqrt{2} V_s \sin \omega t)^2 d(\omega t) \right) \right)^{1/2}$$

$$= V_s \left(1 - \frac{3\alpha}{2\pi} + \frac{3 \sin 2\alpha}{4\pi} \right)^{1/2} \qquad \text{for Mode III } (0 \le \alpha < \pi/3) \tag{4.5}$$

where V_s is the rms value of the phase voltage of the power supply given by

$$v_{AN} = \sqrt{2} V_s \sin \omega t; \quad v_{BN} = \sqrt{2} V_s \sin(\omega t - 2\pi/3); \text{ and } v_{CN} = \sqrt{2} V_s \sin(\omega t + 2\pi/3) \tag{4.6}$$

The analysis of the three-phase AC voltage controller with inductive load is quite complex since the thyristors do not cease conducting when the supply voltage falls down to zero and becomes negative, the same phenomenon as discussed in the single-phase AC voltage controller. Computer simulation provides an effective means of obtaining the load voltage and current waveforms. Figure 4-10 shows simulated waveforms for phase-a load voltage v_{an}, line-to-line voltage v_{ab}, and load current i_a when the voltage controller operates with a three-phase, Y-connected RL load having a power factor of 0.9 at different delay angles. The waveform for the phase-a load current i_a is much smoother than its phase voltage v_{an} due to the filtering effect of the load inductance. The load power factor angle φ is equal to 25.8° as indicated in the figure.

With the pure inductive load ($\varphi = \pi/2$) the rms value of the load voltage v_{an} of the three-phase AC voltage controller is given by [4]

$$V_{an} = \begin{cases} V_s & \text{for } 0 \le \alpha < \pi/2 \\ V_s \left(\frac{5}{2} - \frac{3\alpha}{\pi} + \frac{3 \sin(2\alpha)}{2\pi} \right)^{1/2} & \text{for } \pi/2 \le \alpha < 2\pi/3 \\ V_s \left(\frac{5}{2} - \frac{3\alpha}{\pi} + \frac{3 \sin(2\alpha + \pi/3)}{2\pi} \right)^{1/2} & \text{for } 2\pi/3 \le \alpha < 5\pi/6 \end{cases} \tag{4.7}$$

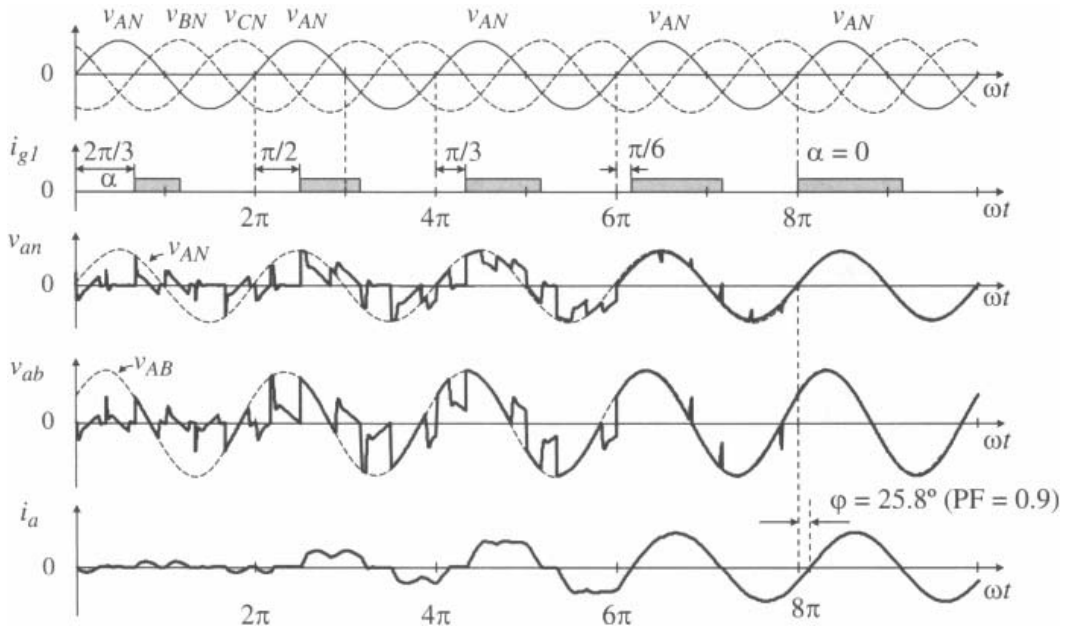


Figure 4-10. Waveforms of three-phase AC voltage controller with an RL load (cos $\varphi = 0.9$) and various delay angles. $\alpha = 2\pi/3$ (first cycle), $\pi/2$ (second cycle), $\pi/3$ (third cycle), $\pi/6$ (fourth cycle), and 0 (fifth cycle).

Based on Equations (4.3) to (4.7), the relationship between V_{an}/V_s and α is given in Figure 4-11 with the load power factor angle φ as a parameter. The other curves for $\varphi = 45°$, 60°, and 75° are obtained by computer simulations. It is noted that when the delay angle α is smaller than the load power factor angle φ, the load voltage V_{an} is equal to the supply voltage V_s and, therefore, is no longer adjustable, the same phenomenon as discussed in the single-phase AC voltage controller.

4.3 INTERLEAVED BOOST CONVERTERS

The DC/DC boost converter is one of the converter topologies often used in synchronous generator (SG) based wind energy conversion systems. As shown in Figure 4-1c, the converter is placed between the diode rectifier and the inverter of the power conversion system. The boost converter serves two main functions: tracking maximum power from the wind and boosting DC voltage to an appropriate value for the inverter. The second function facilitates the capture of maximum power from the wind at all wind speeds. For low- and medium-power wind energy systems of a few kilowatts to hundreds of kilowatts, a single-channel boost converter is often used.

In high-power megawatt wind energy systems, the current and voltage ratings can easily go beyond the range that one switching device can handle. Multiple switching devices connected in parallel or series can be a solution. However, extra measures

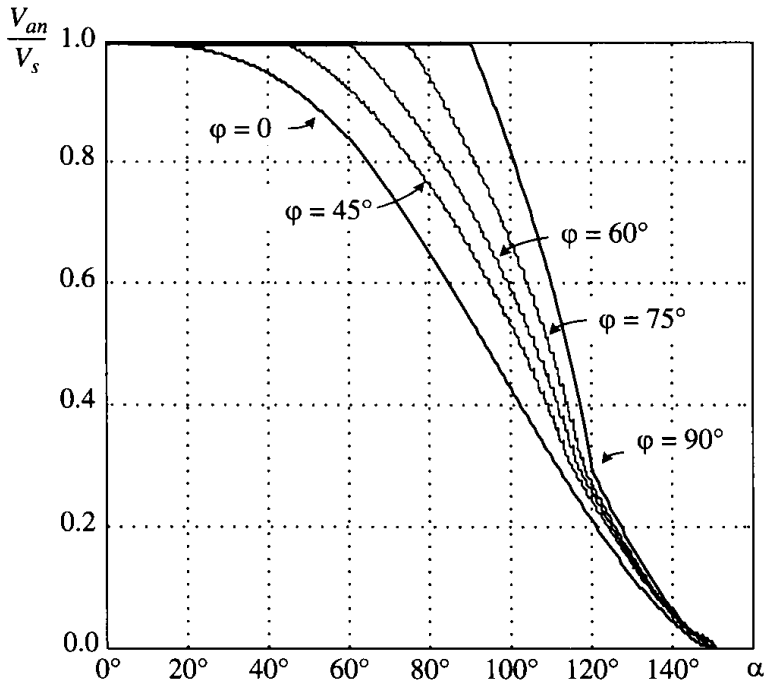


Figure 4-11. Load voltage to supply voltage ratio V_{an}/V_s versus delay angle α for three-phase AC voltage controller.

should be taken for equal sharing of the current or voltage among the parallel or series devices. Instead of connecting the switching devices in parallel or series, paralleling or cascading power converters is another valid solution.

In the low-voltage (e.g., 690 V) megawatt wind energy systems, multichannel interleaved boost converters are often used to handle high currents in the system. An interleaved boost converter can be realized by interleaving (phase shifting) the gating signals for each of the parallel converters. One of the main benefits of the interleaved converter over the single converter is that the equivalent switching frequency of converter is increased. The equivalent switching frequency of the converter can be twice of the device switching frequency for a two-channel converter, or three times for a three-channel converter. The increase in the equivalent switching frequency in the interleaved converter offers a number of advantages over the single-channel converter, such as lower input current ripple and output voltage ripple, faster dynamic response, and better power handling capability.

The interleaved boost converter in the WECS normally employs an IGBT as a switching device instead of the MOSFET that is often used in low-power switch-mode power supplies. To reduce the switching losses, the IGBT operates at low switching frequencies of a few hundred hertz to a few kilohertz, whereas the MOSFET often operates at much higher switching frequencies.

In this section, the single-channel and multichannel interleaved boost converters are introduced. The operating principles of these converters are discussed, and their input current and output voltage ripples are analyzed.

4.3.1 Single-Channel Boost Converter

A boost converter is a power converter with an output DC voltage greater than its input DC voltage. A typical circuit diagram for the single-channel boost converter is shown in Figure 4-12. It is composed of a switch S_1, a diode D_1, a DC inductor L_1, and a filter capacitor C. It is assumed in the following analysis that (1) all the components in the converter are ideal (no power or voltage losses) and (2) the output filter capacitor C is very large and the output voltage of the converter is ripple free.

When switch S_1 is turned on, diode D_1 is reverse biased, and the output is isolated from the input. The input supplies energy to the inductor L_1. When the switch is turned off, diode D_1 is forward biased, and the energy stored in L_1 is released to the load through the diode. In this case, the output voltage v_o is the sum of the input voltage v_i and the inductor voltage v_{L1}, making the converter output voltage v_o higher than its input voltage v_i.

Depending on the continuity of the DC inductor current i_{L1}, the operation of the converter can be divided into two operating modes: continuous-current mode (CCM) and discontinuous-current mode (DCM). When a boost converter operates in CCM, the inductor current i_{L1} never falls to zero. Figure 4-13 shows the typical waveforms of currents and voltages in the boost converter operating in this mode.

In steady-state operation of the converter, the integral of the inductor voltage v_{L1} over time period T_s must be zero. This implies that the average voltage across the inductor L_1 over T_s is zero. Its graphical interpretation is that the area A_1 in Figure 4-13 must equal area A_2, that is,

$$V_i t_{on} = (V_o - V_i) t_{off} \tag{4.8}$$

from which

$$\frac{V_o}{V_i} = \frac{1}{1-D} \quad \text{for } 0 \le D < 1 \tag{4.9}$$

where D is duty cycle of the converter, defined by $D = t_{on}/T_s$; T_s is the switching period; and t_{on} and t_{off} are the turn-on and turn-off times of the switch S, respectively. The

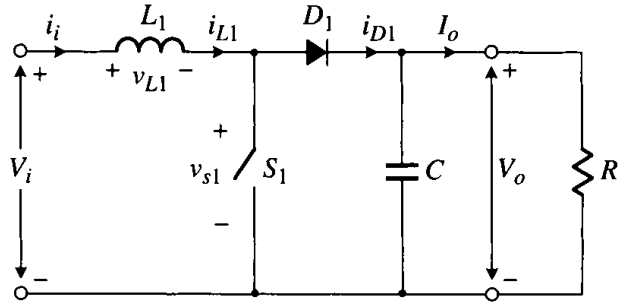


Figure 4-12. A simplified circuit for single-channel boost converter.

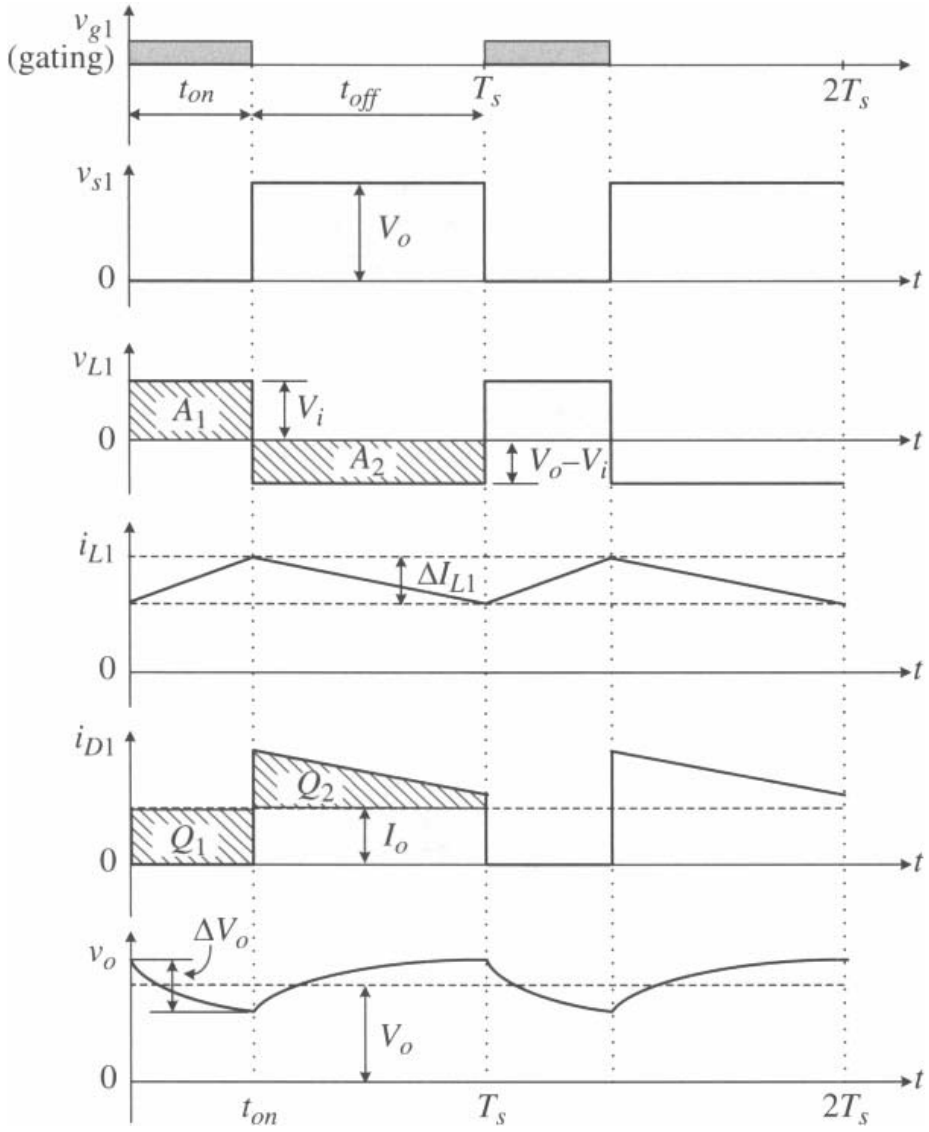


Figure 4-13. Waveforms of single-boost converter operating in a continuous current mode.

above expression indicates that the output voltage of the converter is always higher than its input voltage.

The relationship between the converter input current I_i and output current I_o can be derived from $V_i I_i = V_o I_o$, from which

$$\frac{I_o}{I_i} = 1 - D \quad \text{for} \quad 0 \le D < 1 \tag{4.10}$$

To calculate the ripple current in the inductor, differential equation $v_{L1} = L_1(di_{L1}/dt)$ can be replaced by a difference equation $\Delta v_{L1} = L_1(\Delta i_{L1}/\Delta t)$ since the inductor current

changes linearly with time. For the t_{off} period in Figure 4-13, the inductor ripple current can be expressed by

$$\Delta i_{L1} = \frac{\Delta v_{L1}}{L_1}\Delta t = \frac{(V_o - V_i)}{L_1} t_{off} = D(1-D)\frac{V_o T_s}{L_1} \tag{4.11}$$

The maximum current ripple $\Delta I_{L1,max}$ for the single-channel boost converter occurs when the duty cycle D is 0.5, at which

$$\Delta I_{L1,max} = \frac{V_o T_s}{4L_1} \tag{4.12}$$

When the converter operates under light load conditions, the load current is low, and so is the current in the inductor L_1. The energy stored in the inductor during the t_{on} period may not be sufficient to maintain its current during the t_{off} period. Consequently, the inductor current i_{L1} reaches zero before the end of the t_{off} period and, therefore, becomes discontinuous. The converter thus operates in the discontinuous current mode. The inductor current at the boundary between the CCM and DCM is given by [5]

$$I_{LB} = D(1-D)\frac{V_o T_s}{2L_1} = \frac{\Delta i_{L1}}{2} \tag{4.13}$$

The maximum inductor boundary current occurs at $D = 0.5$, which can be calculated by

$$I_{LB,max} = \frac{V_o T_s}{8L_1} \tag{4.14}$$

The boundary output current can be found from

$$I_{oB} = D(1-D)^2 \frac{V_o T_s}{2L_1} = (1-D)\frac{\Delta i_{L1}}{2} \tag{4.15}$$

and its maximum value occurs at $D = 1/3$, and can be determined by [5]

$$I_{oB,max} = \frac{2}{27}\frac{V_o T_s}{L_1} \tag{4.16}$$

To calculate the output voltage ripple in the single-channel boost converter, we can look into the waveform of the current i_{D1} in the diode D_1 as shown in Figure 4-13. Assuming that all the ripple current component in D_1 is absorbed by the large output capacitor C, the capacitor C is discharged to the load during the t_{on} period when the diode is turned off, and charged during the t_{off} period when D_1 is on. The amount of charges, Q_1 during t_{on} and Q_2 during t_{off}, represented by the shaded areas should be equal. The peak-to-peak ripple voltage can then be calculated by

$$\Delta V_o = \frac{Q_1}{C} = \frac{I_o t_{on}}{C} = \frac{V_o D T_s}{RC} \tag{4.17}$$

from which

$$\frac{\Delta V_o}{V_o} = \frac{DT_s}{RC} \tag{4.18}$$

For a given load resistance R and filter capacitor C, the ripple voltage ΔV_o increases with the duty cycle D.

Typical waveforms of the converter operating in a discontinuous current mode are shown in Figure 4-14.

During the t_{on} period, the operation of the converter in the DCM is the same as that in the CCM. The current i_{L1} increases over time and energy is stored in L_1. During the t_{off} period, the inductor current i_{L1} falls to zero at the end of $K_1 T_s$ period, at which all the energy stored in L_1 during the t_{on} period is completely released. Since the average voltage across the inductor over switching period T_s is equal to zero, area A_1 in Figure 4-14 must equal A_2, that is,

$$V_i t_{on} = (V_o - V_i) K_1 T_s \tag{4.19}$$

from which

$$\frac{V_o}{V_i} = \frac{K_1 + D}{K_1} \qquad \text{for} \quad 0 \le D < 1 \tag{4.20}$$

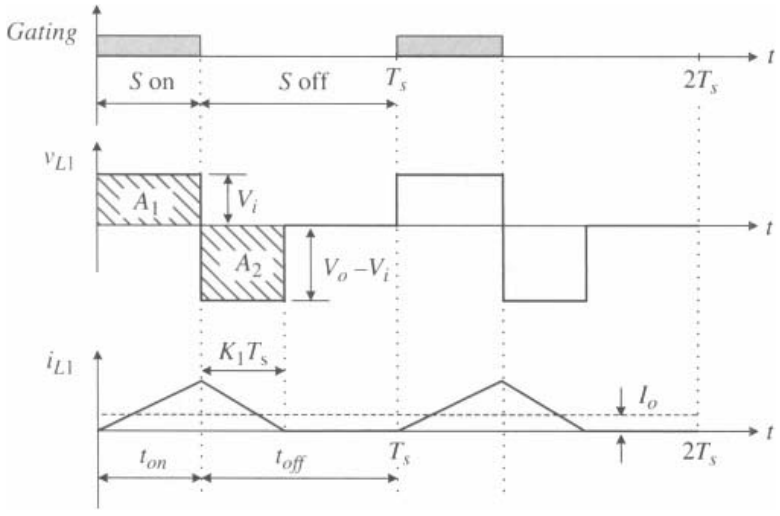


Figure 4-14. Waveforms of single-channel boost converter operating in a discontinuous current mode.

where K_1 can be calculated by [5]

$$K_1 = \frac{2L_1}{K_1 T_s D} I_o \tag{4.21}$$

4.3.2 Two-Channel Interleaved Boost Converter

The converter topology for a two-channel interleaved boost converter is shown in Figure 4-15 [6]. There are two parallel converter channels in the circuit. The first channel is composed of inductor L_1, switch S_1, and diode D_1, whereas the second channel consists of L_2, S_2, and D_2. The two converter channels are essentially connected in parallel but operate in an interleaved mode. They share the same filter capacitor C at the output. It is assumed that the parameters of the two channels are identical.

The gating arrangement and the inductor current waveforms of the converter are shown in Figure 4-16. With the interleaving design, the gating signals v_{g1} and v_{g2} for S_1 and S_2 are identical but shifted by $360°/N = 180°$, where N is the number of parallel converter channels. The operation and waveforms of individual converter channels are the same as those for the single-channel converter and, therefore, are not repeated here. Attention should be paid to the total input current i_i, which is the sum of the two inductor currents i_{L1} and i_{L2}. The input current i_i has the following characteristics:

- The average DC component of the input current (I_i) is twice that of the individual inductor ($I_i = I_{L1} + I_{L2}$). Since the input and output voltages for the parallel converters are the same, each channel handles only half of the total power of the load.
- The peak-to-peak input current ripple ΔI_i is smaller than that in the individual channels due to the use of the interleaved technique. This helps to reduce the volume of the input filter (not shown in the figure).
- The frequency of the input ripple current is twice that of the individual channels. In other words, the equivalent switching frequency of the interleaved converter is twice of that of each channel. For a given output voltage ripple, the capacitance of the output capacitor C can be reduced.

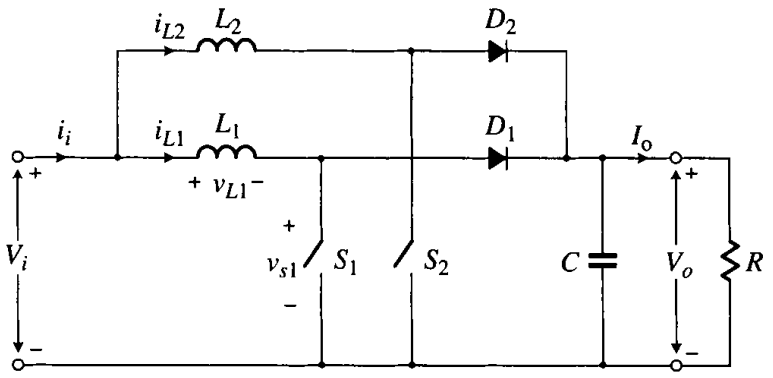


Figure 4-15. Two-channel interleaved boost converter.

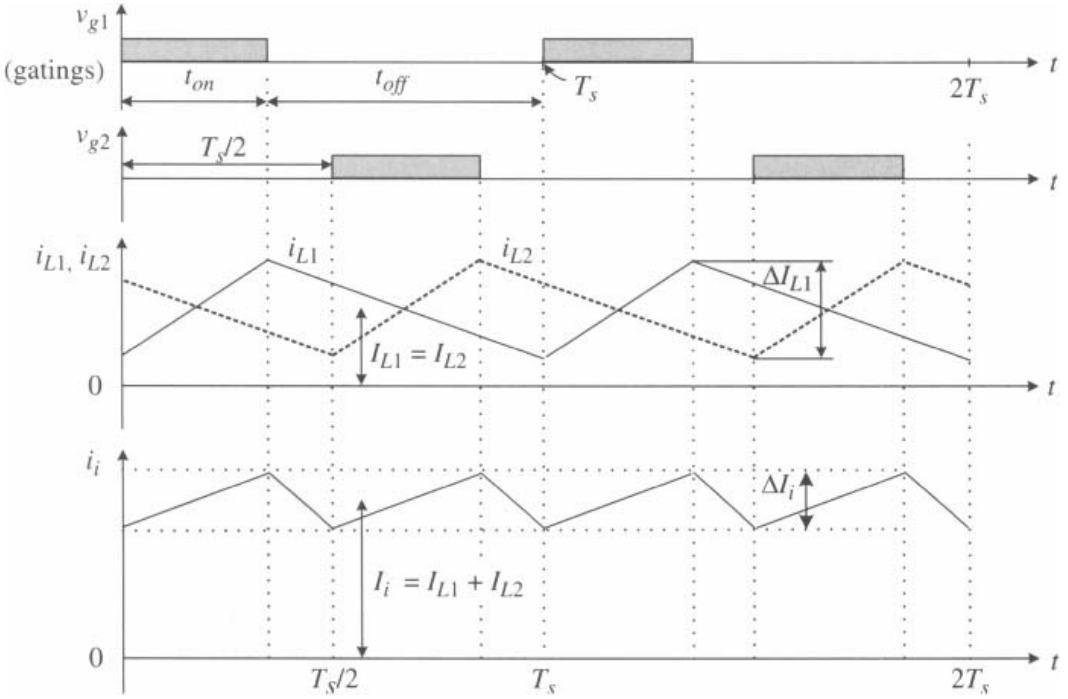


Figure 4-16. Waveforms for the analysis of input current ripple in a two-channel interleaved converter ($D < 0.5$).

Input Current Ripple. It is interesting to note that when the duty cycle D increases from about 0.35 in Figure 4-16 to 0.5, the ripples in the two inductor currents i_{L1} and i_{L2} cancel each other and do not appear in i_i, that is, $\Delta I_i = 0$. The ripple current starts to increase when $D > 0.5$. Therefore, the analysis for the input current ripple can be carried out for the following two cases.

CASE 1: $0 < D \leq 0.5$. The waveforms in Figure 4-16 can be utilized to analyze the input current ripple ΔI_i in the two-channel converter. It is more convenient to perform the analysis for the t_{on} period, during which the total input current i_i increases monotonously. The input current ripple of the converter can be calculated by

$$\Delta I_i = (K_1 - K_2)t_{on} = (K_1 - K_2)DT_s \tag{4.22}$$

where $K_1 = di_{L1}/dt$ and $K_2 = di_{L2}/dt$, which are the slopes of the inductor currents i_{L1} and i_{L2} during charging and discharging process, respectively. Thus,

$$\Delta I_i = \left(\frac{V_i}{L} - \frac{V_o - V_i}{L}\right)\left(1 - \frac{V_i}{V_o}\right)T_s = (1 - 2D)D\frac{V_o T_s}{L} \tag{4.23}$$

where L is the inductance of the each converter channel, that is, $L = L_1 = L_2$.

The maximum input current ripple $\Delta I_{i,\max}$ can be determined by differentiating the above equation with respect to V_i:

$$\frac{\partial \Delta I_i}{\partial V_i} = \left(\frac{2V_i - V_o}{L}\right)\left(1 - \frac{V_i}{V_o}\right)T_s = 0 \tag{4.24}$$

from which

$$V_i = \frac{3}{4}V_o \text{ and } D = 0.25 \quad \text{for } \Delta I_i = \Delta I_{i,\max} \tag{4.25}$$

The maximum current ripple can be found by substituting Equation (4.25) into Equation (4.24):

$$\Delta I_{i,\max} = \frac{V_o T_s}{8L} \tag{4.26}$$

Compare the above equation with Equation (4.12), where the maximum current ripple in the two-channel boost converter is half of the single-channel converter for $D \leq 0.5$.

CASE 2: $0.5 < D < 1$. The waveforms for the analysis of the input current ripple in the two-channel converter are shown in Figure 4-17, where the duty cycle D is 0.65. It

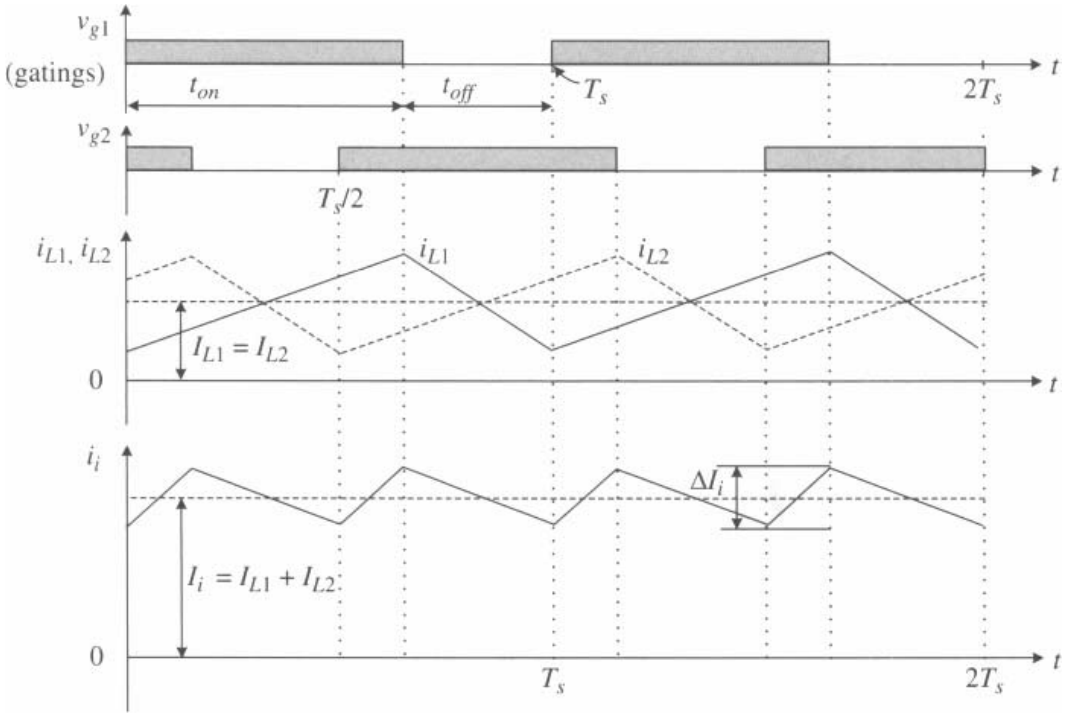


Figure 4-17. Waveforms for analysis of input ripple current in a two-channel interleaved converter ($D > 0.5$).

is more convenient to perform the analysis for the t_{off} period, during which the input current i_i decreases monotonously. The input current ripple can be determined by

$$\Delta I_i = (K_2 - K_1)t_{off} = (K_2 - K_1)(1-D)T_s$$
$$= \left(\frac{V_o - V_i}{L} - \frac{V_i}{L}\right)\left(\frac{V_i}{V_o}\right)T_s = (2D-1)(1-D)\frac{V_o T_s}{L} \tag{4.27}$$

Following the same procedure, the maximum input current ripple $\Delta I_{L1,max}$ can be determined, which is the same as that given in Equation (4.26) for the t_{off} period.

Based on Equations (4.10), (4.24), and (4.27), the input current ripple ΔI_i for the single-channel ($N = 1$) and two-channel ($N = 2$) converters versus duty cycle D is given in Figure 4-18 [6]. ΔI_i is normalized according to the maximum ripple current $\Delta I_{L1,max}$ in the single-channel converter given by Equation (4.11). It is shown that the magnitude of input ripple current for the two-channel converter is much lower than that in the single-channel converter. In particular, the ripple current for the two-channel converter becomes zero at $D = 0.5$, whereas it reaches its maximum value for the single-channel converter. Figure 4-19 shows the ratio of the input ripple current ΔI_i to the channel ripple current ΔI_L versus duty cycle D for the N-channel boost converters.

Output Voltage Ripple. As mentioned earlier, one of the benefits of the interleaved converters is the reduction of the output ripple. In the two-channel converter,

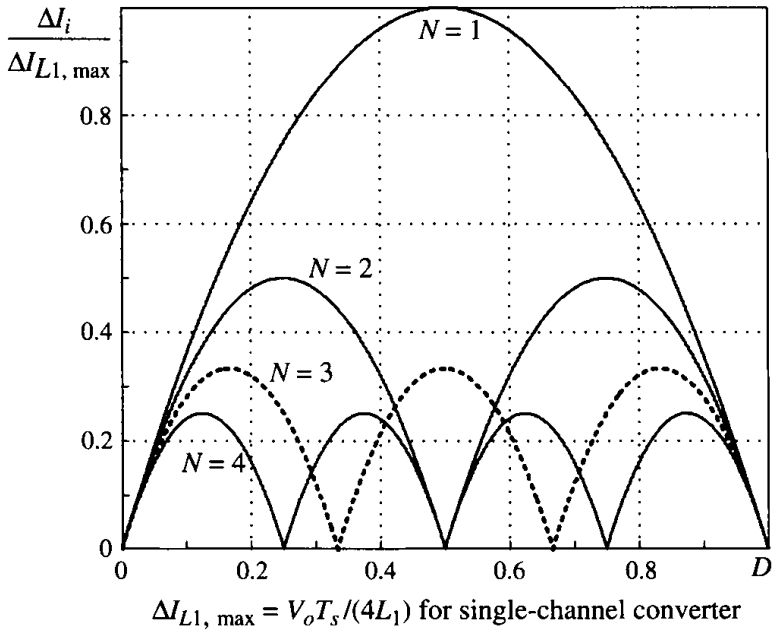


Figure 4-18. Normalized input ripple current versus duty cycle D for N-channel interleaved boost converters.

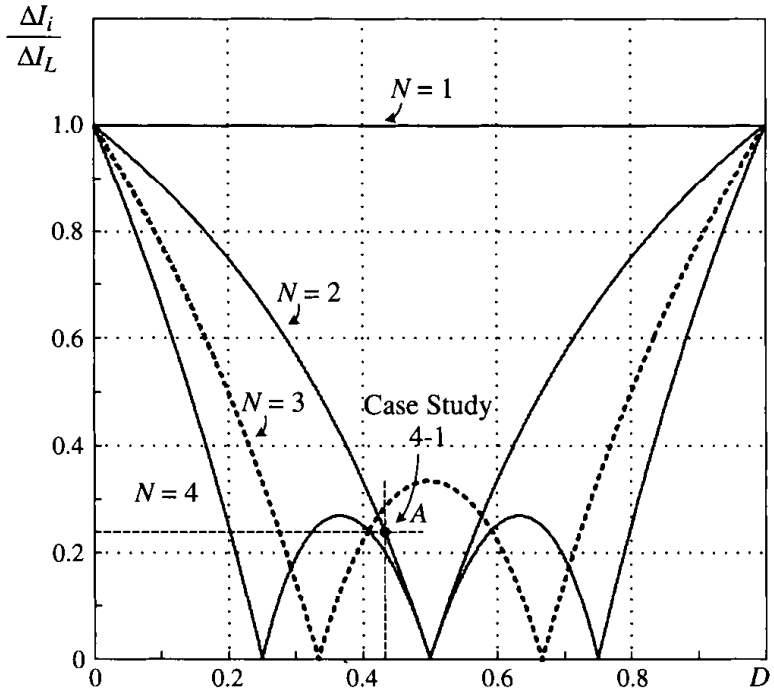


Figure 4-19. Ratio of the input ripple current ΔI_i to the channel ripple current ΔI_L versus duty cycle D for N-channel boost converters.

the two parallel converters share the same output capacitor C, which makes the analysis a little tedious. Computer simulation techniques can be used to determine the output voltage ripples. Figure 4-20 shows the results for the relative output ripple voltage for the two-channel converter under the assumption that the converter operates in a continuous-current mode [6]. The relative output ripple voltage for the single-stage converter is also given in the figure, which is calculated according to Equation (4.13). The two-channel converter produces much lower voltage ripple in comparison to the single-channel converter.

4.3.3 Multichannel Interleaved Boost Converters

Figure 4-21a shows the converter topology for a three-channel ($N = 3$) boost converter interleaved by $360°/N = 120°$. It is essentially composed of three single-channel converters connected in parallel and operating in the interleaving manner. The gate signals for the converters are identical except for a time delay of $T_s/3$ among the converters. The waveforms for the inductor currents, i_{L1}, i_{L2}, and i_{L3}, and the total input current i_L, are shown in Figure 4-21b. It can be observed that the frequency of the converter input current i_i is three times that of the individual converters.

Following the same procedure presented for the two-channel converters, the input current ripple in the three-channel converter can be derived and given by

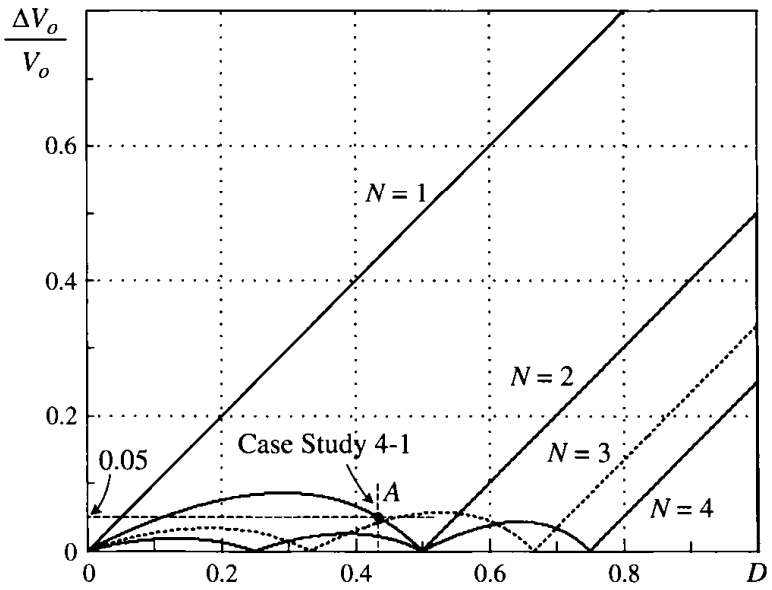


Figure 4-20. Relative output ripple voltages [$\times T_s/(RC)$] versus duty cycle D for N-channel boost converters.

$$\Delta I_i = \begin{cases} (1-3D)D\dfrac{V_o T_s}{L} & \text{for } 0 \le D < \dfrac{1}{3} \\ \left(3D(1-D)-\dfrac{2}{3}\right)\dfrac{V_o T_s}{L} & \text{for } \dfrac{1}{3} \le D < \dfrac{2}{3} \\ (3D-2)(1-D)\dfrac{V_o T_s}{L} & \text{for } \dfrac{2}{3} \le D < 1 \end{cases} \tag{4.28}$$

where L is the inductance of the each converter channel, that is, $L = L_1 = L_2 = L_3$.

The input current ripple ΔI_i and output voltage ripple ΔV_o for the three- and four-channel interleaved converters are illustrated in Figures 4-18 and 4-20, respectively. These current and voltage ripples are further reduced in comparison to those in the single- and two-channel converters. As a result, the size and cost of the input and output filters can be further reduced.

In practical wind energy conversion systems, the maximum power rating for each converter channel is around 500 kW to 600 kW. For a 1.5 MW WECS, three interleaved converters are required.

Case Study 4-1—PMSG Wind Energy System with a Two-Channel Interleaved Boost Converter. A 1.2 MW/690 V permanent magnet synchronous-generator (PMSG) based wind energy conversion system is shown in Figure 4-22, where a two-channel interleaved boost converter and a PWM voltage source inverter are employed. The boost converter provides two main functions: (1) to boost its input DC voltage V_i to a higher DC voltage V_o at its output, and (2) to perform maximum

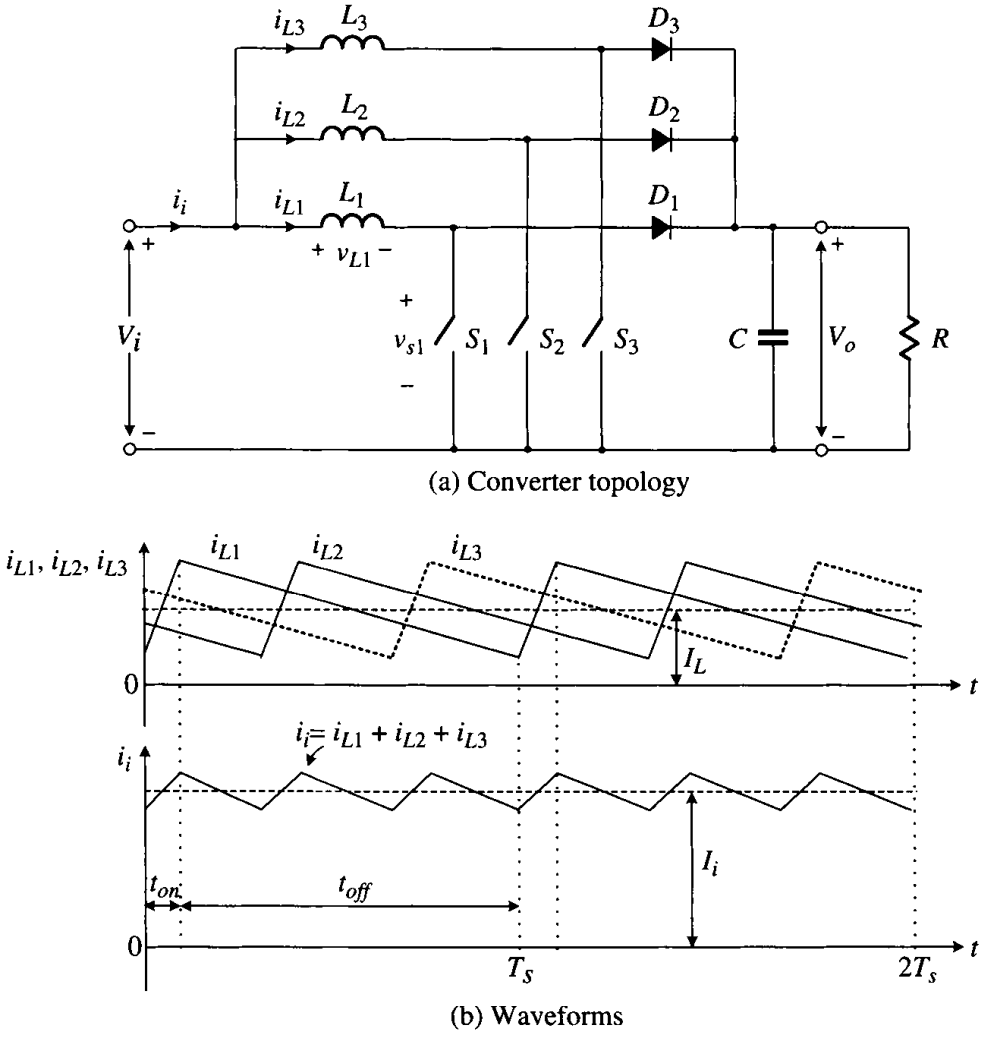


Figure 4-21. Converter topology and waveforms of three-channel interleaved boost converter.

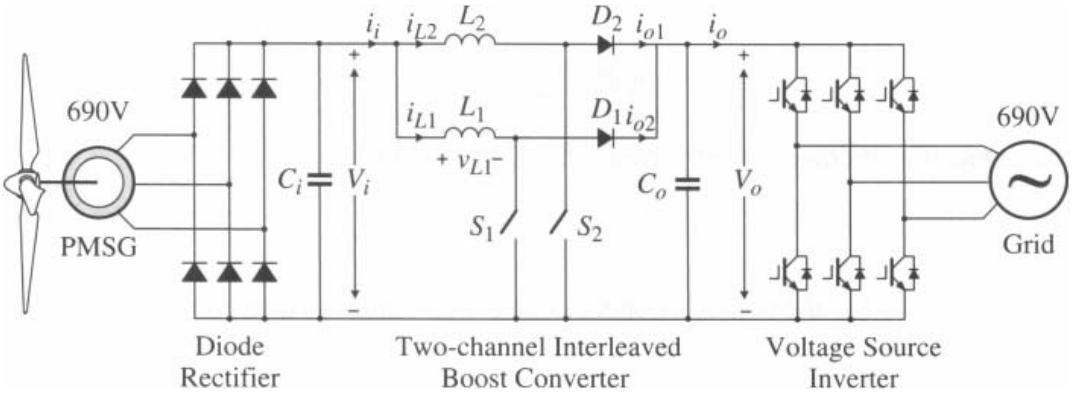


Figure 4-22. A wind energy conversion system with a two-channel interleaved boost converter.

power point tracking (MPPT) such that the system can deliver its maximum possible power captured by the turbine to the grid at any wind speed. The main function of the inverter is to keep its input DC voltage, which is the output of the boost converter, at a fixed value and also to control the reactive power to the grid.

At a given wind speed, the generator operates at a speed of 0.7 pu and delivers 412 kW (0.7^3 pu) power to the grid. The input voltage of the boost converter V_i is 680 V. The output voltage of the boost converter V_o is kept at a constant value of 1200 V by the inverter, which is the voltage required to deliver power to the grid of 690 V (refer to Section 4.7 for details). The inductance of the two-channel converter is $L = L_1 = L_2$ = 270 μH and capacitance of the output filter capacitor C_o is 300 μF. The boost converter operates at a switching frequency of 2 kHz. Assuming that all the converters are ideal without power losses, investigate the input current ripple and output voltage ripple of the boost converter.

Assuming that the boost converter operates in the continuous-current mode, the duty cycle of the each converter channel is

$$D = D_1 = D_2 = 1 - \frac{V_i}{V_o} = 1 - \frac{680}{1200} = 0.4333 \tag{4.29}$$

The ripple current in the two inductors can be calculated by

$$\Delta I_L = \Delta I_{L1} = \Delta I_{L2} = D(1-D)\frac{V_o T_s}{L} = 545.6 \text{ A} \tag{4.30}$$

The boundary inductor current relates the inductor ripple current by

$$I_{LB} = I_{LB1} = I_{LB2} = \Delta I_L / 2 = 272.8 \text{ A} \tag{4.31}$$

The boundary output current for each channel

$$I_{oB} = I_{oB1} = I_{oB2} = (1-D) I_{LB} = 154.6 \text{ A} \tag{4.32}$$

The total average output current of the interleaved converter is

$$I_o = P_o / V_o = 343.3 \text{ A} \tag{4.33}$$

from which the average output current of each channel is

$$I_{o1} = I_{o2} = I_o / 2 = 171.7 \text{ A} \tag{4.34}$$

Since $I_{o1} = I_{o2} > I_{oB}$, the converter operates in the continuous current mode.

The total input current of the boost converter is given by

$$I_i = \begin{cases} P_i / V_i = P_o / V_i = 412 \times 10^3 / 680 = 605.8 \text{ A} \\ I_o / (1-D) = 343.4 / (1-0.4333) = 605.8 \text{ A} \end{cases} \tag{4.35}$$

The percentage inductor ripple current in each channel can be found from

$$\frac{\Delta I_{L1}}{I_{L1}} = \frac{\Delta I_{L2}}{I_{L2}} = \frac{\Delta I_L}{I_i/2} = \frac{545.6}{605.8/2} = 180.1\% \tag{4.36}$$

The total input current ripple

$$\Delta I_i = (1-2D)D\frac{V_o T_s}{L} = 128.4 \text{ A} \tag{4.37}$$

The total input current ripple can be found from

$$\frac{\Delta I_i}{I_i} = \frac{128.4}{606} = 21.2\% \tag{4.38}$$

which is much lower than the inductor ripple current of 180.1% in each of the channels.

The ratio of the total input ripple current ΔI_i to the inductor ripple current ΔI_L of each channel is

$$\frac{\Delta I_i}{\Delta I_L} = \frac{128.4}{545.6} = 23.5\% \tag{4.39}$$

which is verified by Point *A* in Figure 4-19.

To determine the output ripple voltage of the interleaved boost converter, it is assumed that the effect of the inverter operation on the DC voltage ripple is neglected. The load of the boost converter, which is the inverter, can be modeled by an equivalent resistance given by

$$R_{eq} = \frac{V_o}{I_o} = 3.495\ \Omega \tag{4.40}$$

Making use of Figure 4-20, the percentage output ripple voltage can be obtained by

$$\frac{\Delta V_o}{V_o} \simeq 0.05 \times \left(\frac{T_s}{R_{eq}C_o}\right) = 0.05 \times \frac{1/2000}{3.495 \times 300 \times 10^{-6}} = 2.38\% \tag{4.41}$$

If the operation of the two-channel converters were not interleaved, switches S_1 and S_2 would be turned on and off simultaneously. The output ripple voltage would then be

$$\frac{\Delta V_o}{V_o} = D\left(\frac{T_s}{R_{eq}C_o}\right) = 0.433 \times \frac{1/2000}{3.495 \times 300 \times 10^{-6}} = 20.6\% \tag{4.42}$$

which is around 8.6 times higher than that for the interleaved boost converter.

In summary, the multichannel interleaved converter produces much lower input current ripple and output voltage ripple in comparison to the single-channel boost converter.

4.4 TWO-LEVEL VOLTAGE SOURCE CONVERTERS

Figure 4-23a shows the simplified circuit diagram for a three-phase, two-level voltage source converter. The converter is composed of six switches, S_1 to S_6, with an antiparallel free-wheeling diode for each switch. The switches can be IGBT or IGCT devices, depending on the power and voltage ratings of the converter.

The converter has been widely used in industry for many different applications. When the converter transforms a fixed DC voltage to a three-phase AC voltage with variable magnitude and frequency for an AC load, as shown in Figure 4-23b, it is often called an inverter. When the converter transforms an AC grid voltage with fixed magnitude and frequency to an adjustable DC voltage for a DC load, it is normally known as an active rectifier or PWM rectifier. Whether it serves as an inverter or a rectifier, the power flow in the converter circuit is bidirectional: the power can flow from its DC side to the AC side, and vice versa.

In wind energy conversion systems, the converter is often connected to an electric grid, and delivers the power generated from the generator to the grid as shown in Figure 4-23d. The converter in this application is referred to as a grid-connected or grid-tied converter. It is also called an inverter since the converter normally delivers power from its DC side to the AC side.

This section focuses on pulse-width modulation (PWM) schemes for two-level voltage source converters. Since the modulation schemes are applicable to the converter that may operate as an inverter or a rectifier, the inverter is used as an example for the discussion. The section starts with an introduction to carrier-based sinusoidal PWM (SPWM) schemes, followed by a detailed analysis of space vector modulation (SVM) algorithms.

4.4.1 Sinusoidal PWM

The principle of the sinusoidal PWM scheme for the two-level converter is illustrated in Figure 4-24, where v_{ma}, v_{mb}, and v_{mc} are the three-phase sinusoidal modulating waveforms and v_{cr} is the triangular carrier signal. The fundamental-frequency component in the inverter output voltage can be controlled by the amplitude-modulation index:

$$m_a = \frac{\hat{V}_m}{\hat{V}_{cr}} \tag{4.43}$$

where $\hat{V}_m$ and $\hat{V}_{cr}$ are the peak values of the modulating and carrier waves, respectively. The amplitude-modulation index m_a is usually adjusted by varying $\hat{V}_m$ while keeping $\hat{V}_{cr}$ fixed. The frequency-modulation index is defined by

$$m_f = \frac{f_{cr}}{f_m} \tag{4.44}$$

where f_m and f_{cr} are the frequencies of the modulating and carrier waves, respectively.

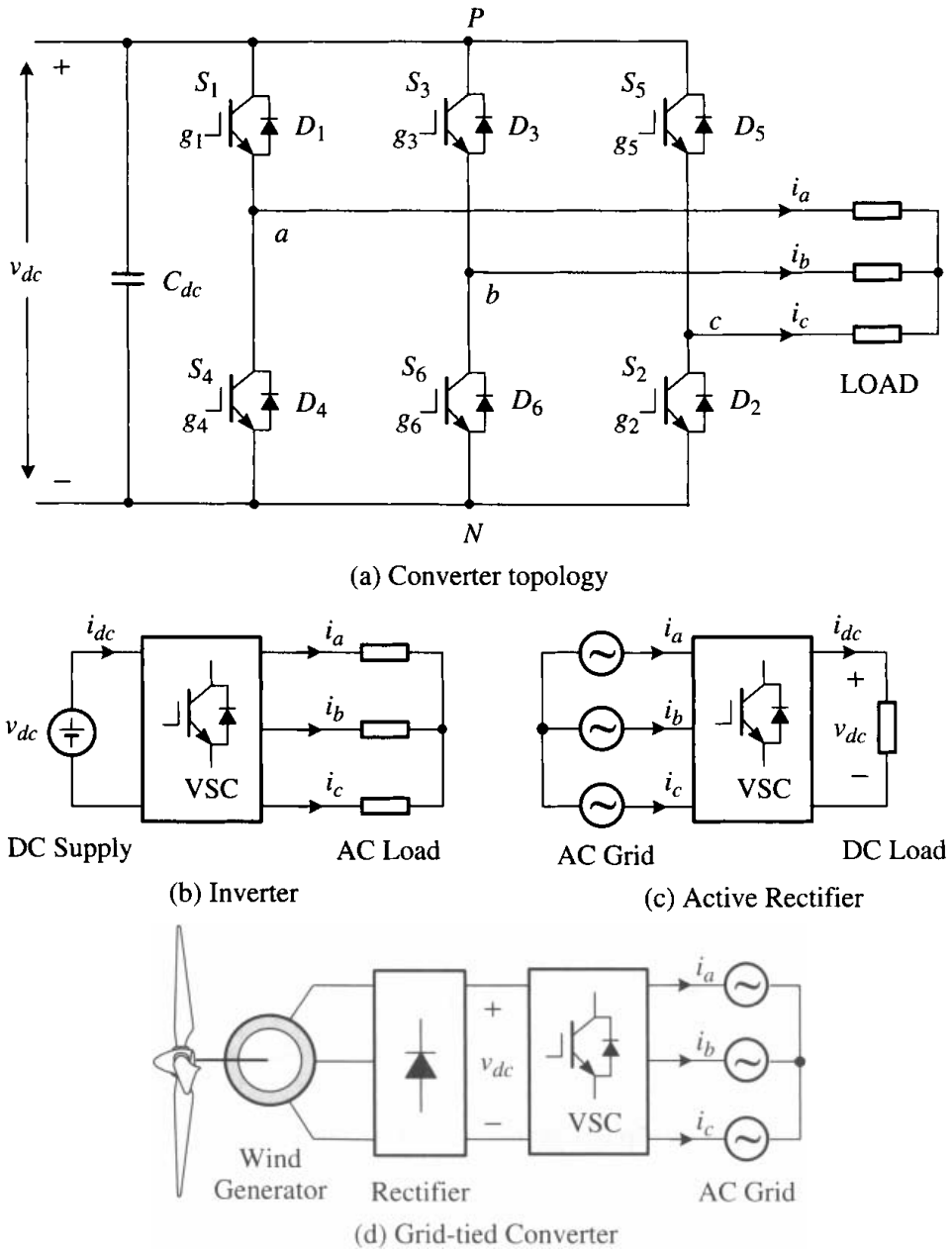


Figure 4-23. Simplified two-level voltage-source converter (VSC).

The operation of switches S_1 to S_6 is determined by comparing the modulating waves with the carrier wave. When $v_{ma} > v_{cr}$, the upper switch S_1 in inverter leg a is turned on. The lower switch S_4 operates in a complementary manner and thus is switched off. The resultant inverter terminal voltage v_{aN}, which is the voltage at the phase-a terminal with respect to the negative DC bus N, is equal to the DC voltage V_{dc}. When $v_{ma} < v_{cr}$, S_4 is on and S_1 is off, leading to $v_{aN} = 0$ as shown in Figure 4-24. Since the waveform of v_{aN} has only two levels, V_{dc} and 0, the inverter is often referred to as a two-level inverter. It is noted that to avoid possible short-circuiting during switching

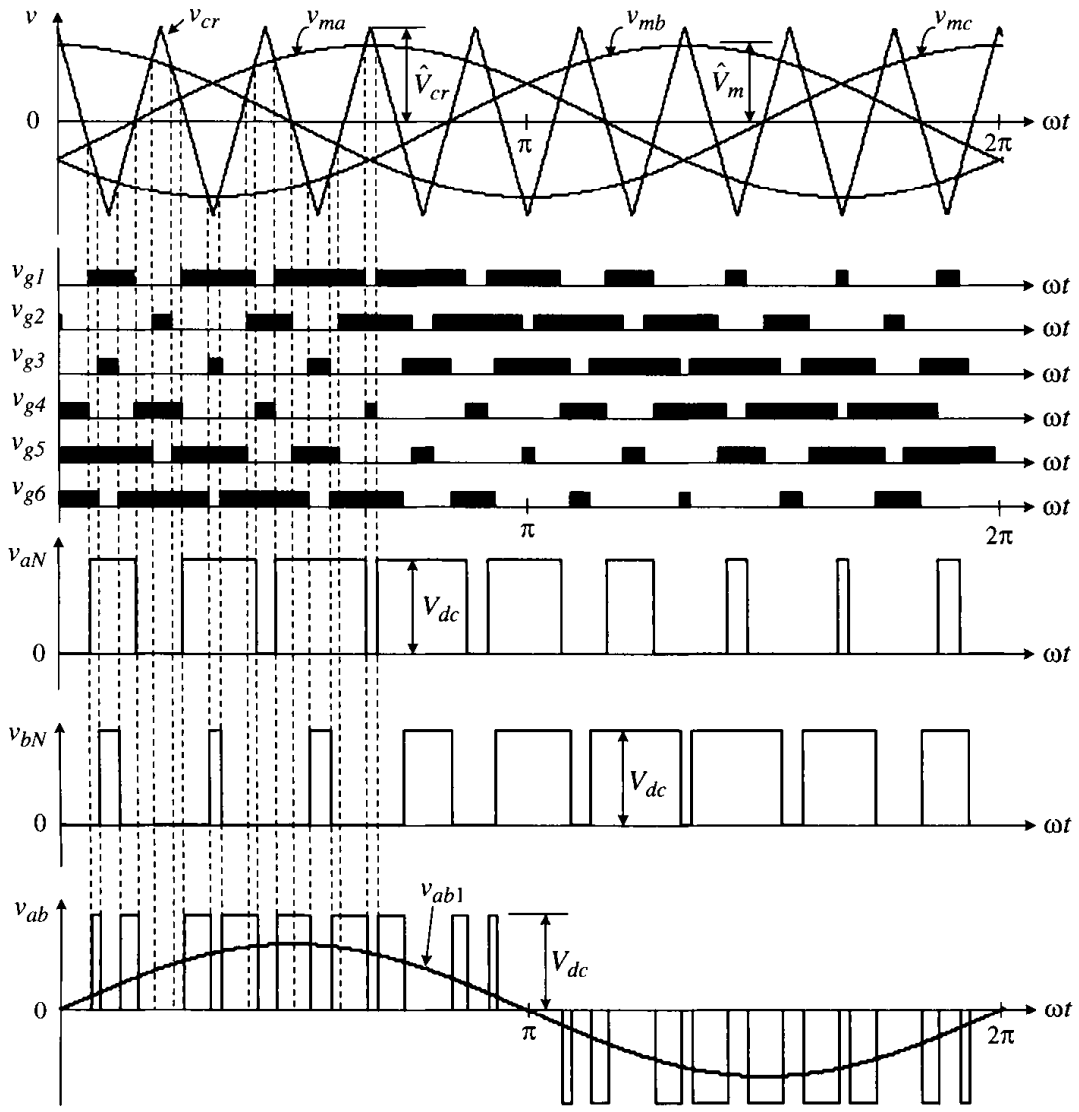


Figure 4-24. Sinusoidal pulse-width modulation (SPWM).

transients of the upper and lower devices in an inverter leg, a blanking time (or dead time) should be implemented, during which both switches are turned off.

The inverter line-to-line voltage v_{ab} can be determined by $v_{ab} = v_{aN} - v_{bN}$. The waveform of its fundamental-frequency component v_{ab1} is also given in the figure. The magnitude and frequency of v_{ab1} can be independently controlled by m_a and f_m, respectively.

The switching frequency of the active switches in the two-level inverter can be found from $f_{sw} = f_{cr} = f_m \times m_f$. For instance, v_{aN} in Figure 4-24 contains nine pulses per cycle of the fundamental frequency. Each pulse is produced by turning S_1 on and off once. With the fundamental frequency of 60 Hz, the resultant switching frequency for S_1 is $f_{sw} = 60 \times 9 = 540$ Hz, which is also the carrier frequency f_{cr}. It is worth noting that the device switching frequency may not always be equal to the carrier frequency in multilevel inverters. This issue will be addressed in the later sections.

When the carrier wave is synchronized with the modulating wave (m_f is an integer), the modulation scheme is known as synchronous PWM, in contrast to asynchronous PWM, whose carrier frequency f_{cr} is usually fixed and independent of f_m. The asynchronous PWM features a fixed switching frequency and easy implementation with analog circuits. However, it may generate noncharacteristic harmonics, whose frequency is not a multiple of the fundamental frequency. The synchronous PWM scheme is more suitable for implementation with a digital processor.

Case Study 4-2—Harmonic Analysis of Two-Level VSI with Carrier-Based Sinusoidal Modulation. The purpose of this case study is to investigate the harmonic characteristics of the two-level voltage source inverter with carrier-based sinusoidal modulation. Figure 4-25 shows a set of simulated waveforms for the two-level inverter, where v_{ab} is the inverter line-to-line voltage, v_a is the phase-a load voltage, and i_a is the phase-a load current. The inverter operates under the condition of m_a =

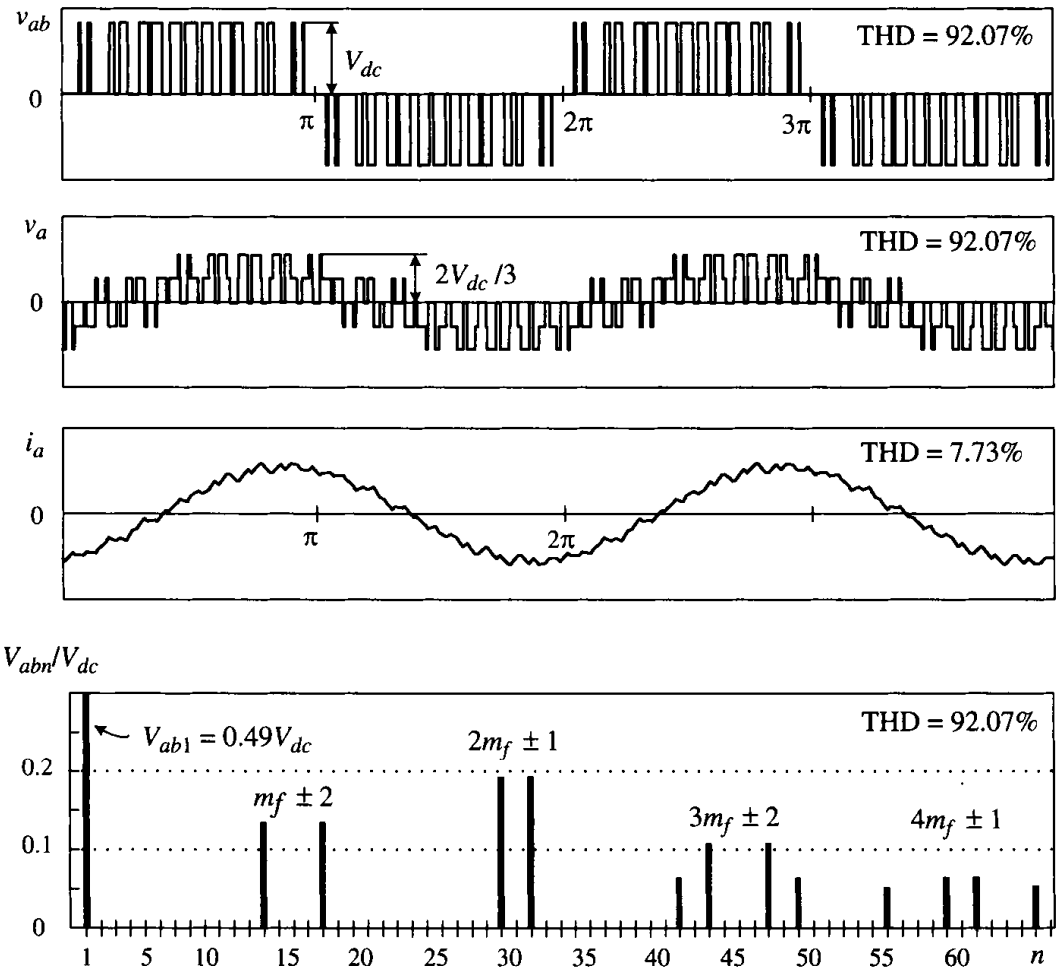


Figure 4-25. Simulated waveforms for the two-level inverter operating at m_a = 0.8 and m_f = 15, and f_m = 60 Hz and f_{sw} = 900 Hz.

0.8, $m_f = 15$, $f_m = 60$ Hz, and $f_{sw} = 900$ Hz with a rated three-phase inductive load. The load power factor is 0.9 per phase. It can be observed that

- All the harmonics in v_{ab} with order lower than $(m_f - 2)$ are eliminated.
- The harmonics are centered around m_f and its multiples, such as $2m_f$ and $3m_f$.

The above statements are valid for $m_f \geq 9$ with a m_f multiple of 3.

The waveform of the load current i_a is close to sinusoidal with a total harmonic distortion (THD) of 7.73%. The low amount of harmonic distortion is due to the elimination of low-order harmonics by the modulation scheme and the filtering effect of the load inductance.

Figure 4-26 shows the harmonic content of the inverter line-to-line voltage v_{ab} normalized to its DC voltage V_{dc} as a function of m_a, where V_{abn} is the nth-order harmonic voltage (rms). The fundamental-frequency component V_{ab1} increases linearly with m_a, whose maximum value can be found from

$$V_{ab1,\max} = 0.612\, V_d \qquad \text{for } m_a = 1 \tag{4.45}$$

The THD curve for v_{ab} is also given in the figure.

4.4.2 Space Vector Modulation

Space vector modulation (SVM) is one of the real-time modulation techniques and is widely used for digital control of voltage source inverters. This section presents the principle and implementation of the space vector modulation for the two-level inverter.

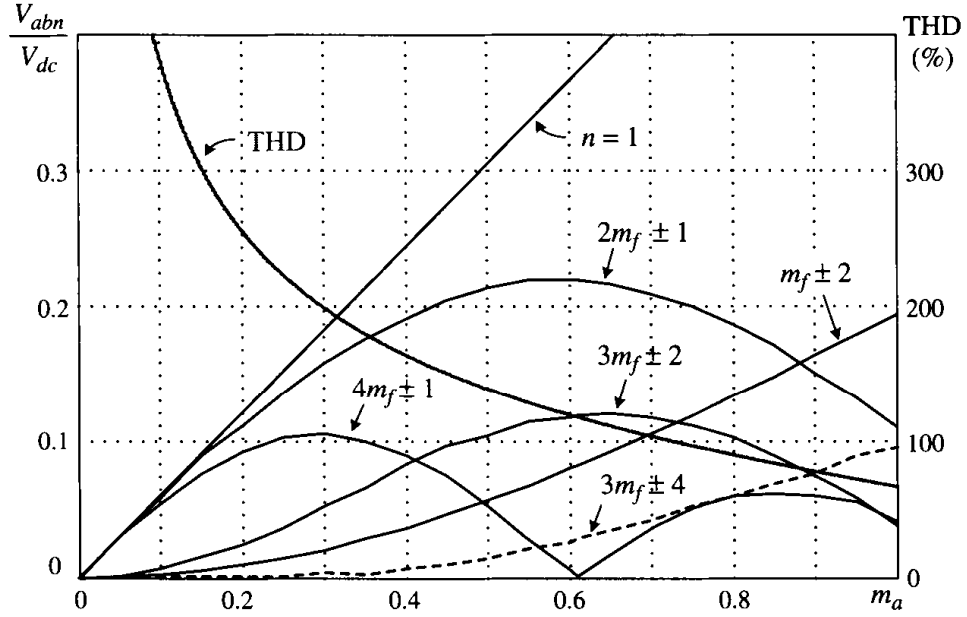


Figure 4-26. Harmonic content of v_{ab} in Figure 4-25.

Switching States. The operating status of the switches in the two-level inverter in Figure 4-23a can be represented by switching states. As indicated in Table 4-1, switching state P denotes that the upper switch in an inverter leg is on and the inverter terminal voltage (v_{aN}, v_{bN}, or v_{cN}) is positive ($+V_{dc}$), whereas O indicates that the inverter terminal voltage is zero due to the conduction of the lower switch.

There are eight possible combinations of switching states in the two-level inverter as listed in Table 4-2. The switching state [POO], for example, corresponds to the conduction of S_1, S_6, and S_2 in the inverter legs a, b, and c, respectively. Among the eight switching states, [PPP] and [OOO] are zero states and the others are active states.

Space Vectors. The active and zero switching states can be represented by active and zero space vectors, respectively. A typical space vector diagram for the two-level inverter is shown in Fig. 4-27, where the six active vectors $\vec{V}_1$ to $\vec{V}_6$ form a regular hexagon with six equal sectors (I to VI). The zero vector $\vec{V}_0$ lies at the center of the hexagon.

To derive the relationship between the space vectors and switching states, refer to the two-level inverter in Figure 4-23a. Assuming that the operation of the inverter is three-phase balanced, we have

$$v_a(t) + v_b(t) + v_c(t) = 0 \tag{4.46}$$

where v_a, v_b, and v_c are the instantaneous load phase voltages. From a mathematical point of view, one of the phase voltages is redundant since, given any two phase voltages, the third one can be readily calculated. Therefore, it is possible to transform the three-phase variables to two-phase variables through the $abc/\alpha\beta$ transformation presented in Chapter 3:

$$\begin{bmatrix} v_\alpha(t) \\ v_\beta(t) \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix} \tag{4.47}$$

A space vector can be generally expressed in terms of the two-phase voltages in the α-β frame:

$$\vec{v}(t) = v_\alpha(t) + j v_\beta(t) \tag{4.48}$$

Table 4-1. Definition of switching states

	Leg a			Leg b			Leg c		
Switching state	S_1	S_4	v_{aN}	S_3	S_6	v_{bN}	S_5	S_2	v_{cN}
P	On	Off	V_{dc}	On	Off	V_{dc}	On	Off	V_{dc}
O	Off	On	0	Off	On	0	Off	On	0

Table 4-2. Space vectors, switching states, and on-state switches

Space vector		Switching state (three phases)	on-state switch	Vector definition
Zero vector	$\vec{V}_0$	[PPP] [OOO]	S_1, S_3, S_5 S_4, S_6, S_5	$\vec{V}_0 = 0$
Active vector	$\vec{V}_1$	[POO]	S_1, S_6, S_2	$\vec{V}_1 = \frac{2}{3} V_{dc} e^{j0}$
	$\vec{V}_2$	[PPO]	S_1, S_3, S_2	$\vec{V}_2 = \frac{2}{3} V_{dc} e^{j\frac{\pi}{3}}$
	$\vec{V}_3$	[OPO]	S_4, S_3, S_2	$\vec{V}_3 = \frac{2}{3} V_{dc} e^{j\frac{2\pi}{3}}$
	$\vec{V}_4$	[OPP]	S_4, S_3, S_5	$\vec{V}_4 = \frac{2}{3} V_{dc} e^{j\frac{3\pi}{3}}$
	$\vec{V}_5$	[OOP]	S_4, S_6, S_5	$\vec{V}_5 = \frac{2}{3} V_{dc} e^{j\frac{4\pi}{3}}$
	$\vec{V}_6$	[POP]	S_1, S_6, S_5	$\vec{V}_6 = \frac{2}{3} V_{dc} e^{j\frac{5\pi}{3}}$

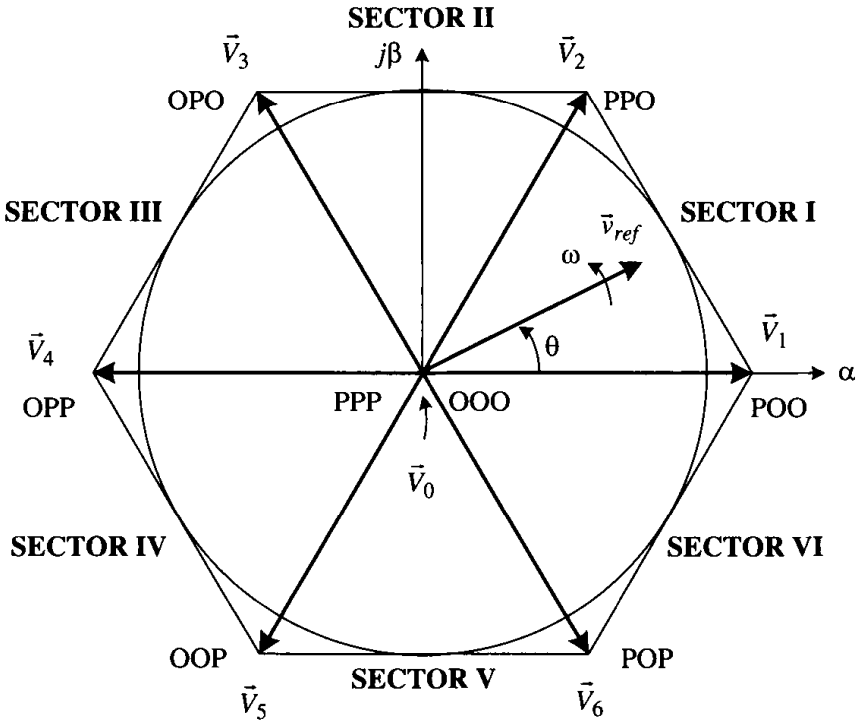


Figure 4-27. Space-vector diagram for the two-level inverter.

Substituting (4.47) into (4.48), we have

$$\vec{v}(t) = \frac{2}{3}\left[v_a(t)e^{j0} + v_b(t)e^{j2\pi/3} + v_c(t)e^{j4\pi/3} \right] \tag{4.49}$$

where $e^{jx} = \cos x + j \sin x$ and $x = 0$, $2\pi/3$ or $4\pi/3$. For the active switching state [POO], the generated load phase voltages are

$$v_a(t) = \frac{2}{3}V_{dc},\ v_b(t) = -\frac{1}{3}V_{dc}, \text{ and } v_c(t) = -\frac{1}{3}V_{dc} \tag{4.50}$$

The corresponding space vector, denoted as $\vec{V}_1$, can be obtained by substituting (4.50) into (4.49):

$$\vec{V}_1 = \frac{2}{3}V_{dc}\,e^{j0} \tag{4.51}$$

Following the same procedure, all six active vectors can be derived:

$$\vec{V}_k = \frac{2}{3}V_{dc}\,e^{j(k-1)\frac{\pi}{3}} \qquad k = 1, 2, \ldots, 6 \tag{4.52}$$

The zero vector $\vec{V}_0$ has two switching states [PPP] and [OOO], one of which is redundant. As will be seen later, the redundant switching state can be utilized to minimize the switching frequency of the inverter or perform other useful functions. The relationship between the space vectors and their corresponding switching states is given in Table 4-2.

Note that the zero and active vectors do not move in space and, thus, are referred to as stationary vectors. On the contrary, the reference vector $\vec{v}_{ref}$ in Figure 4-27 rotates in space at an angular velocity

$$\omega = 2\pi f \tag{4.53}$$

where f is the fundamental frequency of the inverter output voltage. The angular displacement between $\vec{v}_{ref}$ and the α-axis of the α-β frame can be obtained by

$$\theta(t) = \int_0^t \omega(t)\,dt + \theta_0 \tag{4.54}$$

For a given magnitude (length) and position, $\vec{v}_{ref}$ can be synthesized by three nearby stationary vectors, based on which the switching states of the inverter can be selected and gate signals for the active switches can be generated. When $\vec{v}_{ref}$ passes through the sectors one by one, different sets of switches will be turned on or off. As a result, when $\vec{v}_{ref}$ rotates one revolution in space, the inverter output voltage varies one cycle over time. The inverter output frequency corresponds to the rotating speed of $\vec{v}_{ref}$, whereas its output voltage can be adjusted by the magnitude of $\vec{v}_{ref}$.

Dwell Time Calculation. As mentioned earlier, the reference $\vec{v}_{ref}$ can be synthesized by three stationary vectors. The dwell time for the stationary vectors essentially represents the duty-cycle time (on-state or off-state time) of the chosen switches during a sampling period T_s. The dwell time calculation is based on the volt-second balancing principle, that is, the product of the reference voltage $\vec{v}_{ref}$ and sampling period T_s equals the sum of the voltage multiplied by the time interval of chosen space vectors.

Assuming that the sampling period T_s is sufficiently small, the reference vector $\vec{v}_{ref}$ can be considered constant during T_s. Under this assumption, $\vec{v}_{ref}$ can be approximated by two adjacent active vectors and one zero vector. For example, when $\vec{v}_{ref}$ falls into sector I, as shown in Figure 4-28, it can be synthesized by $\vec{V}_1$, $\vec{V}_2$, and $\vec{V}_0$. The volt-second balancing equation is

$$\begin{cases} \vec{v}_{ref} T_s = \vec{V}_1 T_a + \vec{V}_2 T_b + \vec{V}_0 T_0 \\ T_s = T_a + T_b + T_0 \end{cases} \tag{4.55}$$

where T_a, T_b, and T_0 are the dwell times for the vectors $\vec{V}_1$, $\vec{V}_2$, and $\vec{V}_0$, respectively. The space vectors in Equation (4.52) can be expressed as

$$\vec{v}_{ref} = v_{ref} e^{j\theta}, \quad \vec{V}_1 = \frac{2}{3} V_{dc}, \quad \vec{V}_2 = \frac{2}{3} V_{dc} e^{j\frac{\pi}{3}}, \text{ and } \vec{V}_0 = 0 \tag{4.56}$$

where v_{ref} represents the magnitude of the reference vector and θ is the angle between $\vec{v}_{ref}$ and the α-axis of the α-β frame as shown in Figure 4-27.

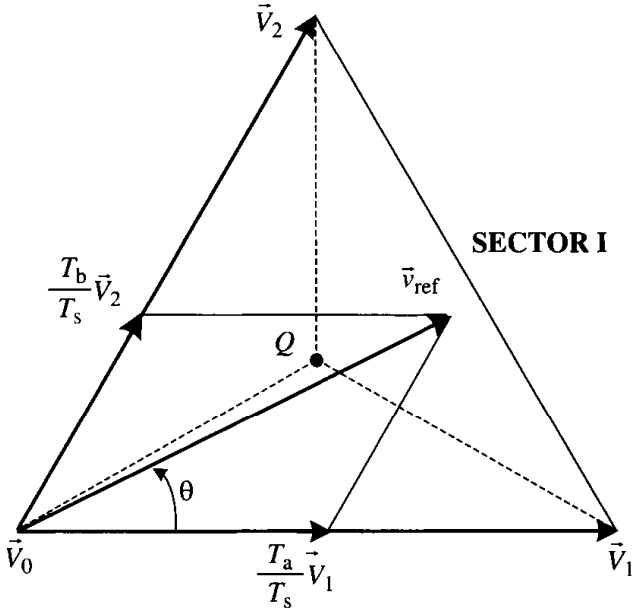


Figure 4-28. $\vec{v}_{ref}$ synthesized by $\vec{V}_1$, $\vec{V}_2$, and $\vec{V}_0$.

Substituting (4.56) into (4.55) and then splitting the resultant equation into the real (α-axis) and imaginary (β-axis) components in the α-β frame, we have

$$\begin{cases} \text{Re}: \quad v_{ref}(\cos\theta)T_s = \dfrac{2}{3}V_{dc}T_a + \dfrac{1}{3}V_{dc}T_b \\ \text{Im}: \quad v_{ref}(\sin\theta)T_s = \dfrac{1}{\sqrt{3}}V_{dc}T_b \end{cases} \tag{4.57}$$

Solving (4.57) together with $T_s = T_a + T_b + T_0$ yields

$$\begin{cases} T_a = \dfrac{\sqrt{3}T_s v_{ref}}{V_{dc}}\sin\left(\dfrac{\pi}{3} - \theta\right) \\ T_b = \dfrac{\sqrt{3}T_s v_{ref}}{V_{dc}}\sin\theta \qquad \text{for } 0 \le \theta < \pi/3 \\ T_0 = T_s - T_a - T_b \end{cases} \tag{4.58}$$

To visualize the relationship between the location of $\vec{v}_{ref}$ and the dwell times, let us examine some special cases. If $\vec{v}_{ref}$ lies exactly in the middle between $\vec{V}_1$ and $\vec{V}_2$ (i.e., $\theta = \pi/6$), the dwell time T_a of $\vec{V}_1$ will be equal to T_b of $\vec{V}_2$. When $\vec{v}_{ref}$ is closer to $\vec{V}_2$, T_b will be greater than T_a. If $\vec{v}_{ref}$ is coincident with $\vec{V}_2$, T_a will be zero. With the head of $\vec{v}_{ref}$ located right on the central point Q, $T_a = T_b = T_0$. The relationship between the $\vec{v}_{ref}$ location and dwell times is summarized in Table 4-3.

Note that although Equation (4.58) is derived when $\vec{v}_{ref}$ is in sector I, it can also be used when $\vec{v}_{ref}$ is in other sectors, provided that a multiple of $\pi/3$ is subtracted from the actual angular displacement θ such that the modified angle θ' falls into the range between zero and $\pi/3$ for use in the equation, that is,

$$\theta' = \theta - (k-1)\pi/3 \qquad \text{for } 0 \le \theta' < \pi/3 \tag{4.59}$$

where $k = 1, 2, \ldots, 6$ for sectors I, II, . . . , VI, respectively. For example, when $\vec{v}_{ref}$ is in sector II, the calculated dwell times T_a, T_b, and T_0 based on Equation (4.58) are for vectors $\vec{V}_2$, $\vec{V}_3$, and $\vec{V}_0$, respectively.

Modulation Index. Equation (4.58) can also be expressed in terms of modulation index m_a:

Table 4-3. $\vec{v}_{ref}$ location and dwell times

$\vec{v}_{ref}$ Location	$\theta = 0$	$0 < \theta < \dfrac{\pi}{6}$	$\theta = \dfrac{\pi}{6}$	$\dfrac{\pi}{6} < \theta < \dfrac{\pi}{3}$	$\theta = \dfrac{\pi}{3}$
Dwell times	$T_a > 0$ $T_b = 0$	$T_a > T_b$	$T_a = T_b$	$T_a < T_b$	$T_a = 0$ $T_b > 0$

$$\begin{cases} T_a = T_s m_a \sin\left(\dfrac{\pi}{3} - \theta\right) \\ T_b = T_s m_a \sin\theta \\ T_0 = T_s - T_a - T_b \end{cases} \tag{4.60}$$

where

$$m_a = \frac{\sqrt{3}\, v_{ref}}{V_{dc}} \tag{4.61}$$

The length of the reference vector $\vec{v}_{ref}$ represents the peak value of the fundamental-frequency component in the inverter output phase voltage, that is,

$$v_{ref} = \hat{V}_{a1} = \sqrt{2} V_{a1} \tag{4.62}$$

where V_{a1} is the rms value of the fundamental component in the inverter output phase (phase-*a*) voltage.

Substituting (4.62) into (4.61), one can find the relationship between m_a and V_{a1}:

$$m_a = \frac{\sqrt{3}\, v_{ref}}{V_{dc}} = \frac{\sqrt{6}\, V_{a1}}{V_{dc}} \tag{4.63}$$

For a given DC voltage V_{dc}, the inverter output voltage V_{a1} is proportional to modulation index m_a.

The maximum length of the reference vector, $v_{ref,\max}$, corresponds to the radius of the largest circle that can be inscribed within the hexagon, as shown in Figure 4-27. Since the hexagon is formed by six active vectors having a length of $2V_{dc}/3$, $v_{ref,\max}$ can be found from

$$v_{ref,\max} = \frac{2}{3} V_{dc} \times \frac{\sqrt{3}}{2} = \frac{V_{dc}}{\sqrt{3}} \tag{4.64}$$

Substituting (4.64) into (4.61) gives the maximum modulation index

$$m_{a,\max} = 1 \tag{4.65}$$

from which the modulation index for the SVM scheme is in the range of

$$0 \le m_a \le 1 \tag{4.66}$$

Switching Sequence. With the space vectors selected and their dwell times calculated, the next step is to arrange the switching sequence. In general, the switching sequence design for a given $\vec{v}_{ref}$ is not unique, but it should satisfy the following two requirements for the minimization of the device switching frequency:

1. The transition from one switching state to the next involves only two switches in the same inverter leg, one being switched on and the other switched off.
2. The transition for $\vec{v}_{ref}$ moving from one sector in the space vector diagram to the next requires no or a minimum number of switchings.

Figure 4-29 shows a typical seven-segment switching sequence and inverter output voltage waveforms for $\vec{v}_{ref}$ in sector I, where $\vec{v}_{ref}$ is synthesized by $\vec{V}_1$, $\vec{V}_2$, and $\vec{V}_0$. The sampling period T_s is divided into seven segments for the selected vectors. It can be observed that

- The dwell times for the seven segments add up to the sampling period ($T_s = T_a + T_b + T_0$).
- Design requirement (1) is satisfied. For instance, the transition from [OOO] to [POO] is accomplished by turning S_1 on and S_4 off, which involves only two switches.
- The redundant switching sates for $\vec{V}_0$ are utilized to reduce the number of switchings per sampling period. For the $T_0/2$ segment in the center of the sampling period, the switching state [PPP] is selected, whereas for the $T_0/4$ segments on both sides, the state [OOO] is used.
- Each of the switches in the inverter turns on and off once per sampling period. The switching frequency f_{sw} of the devices is thus equal to the sampling frequency f_{sp}, that is, $f_{sw} = f_{sp} = 1/T_s$.

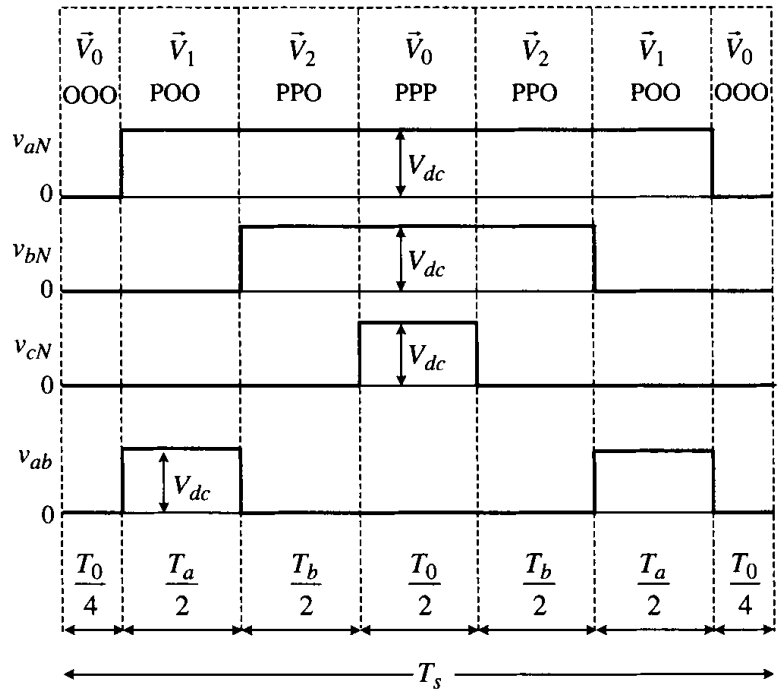


Figure 4-29. Seven-segment switching sequence for $\vec{v}_{ref}$ in sector I.

4.4.3 Harmonic Analysis

The harmonic performance of the SVM scheme for the two-level voltage source inverter is analyzed through the following case study.

Case Study 4-3—Two-Level Voltage Source Inverter with Space Vector Modulation. In this case study, the procedure for computer simulation and real-time digital implementation of the SVM scheme is introduced. Simulation for the two-level voltage source inverter is performance-based, and harmonic performance of the SVM scheme is analyzed.

Figure 4-30 shows a block diagram for computer simulation and digital implementation of the SVM scheme. The input variables, v_a^*, v_b^*, and v_c^*, are the three-phase reference voltages, which are also the required output-phase voltages of the inverter. The reference voltages are normally generated by the controller in a wind energy conversion system. Through the $abc/\alpha\beta$ transformation, the three-phase reference voltages in the abc stationary frame are transformed into two-phase variables, v_β and v_β, in the α-β stationary frame, from which the reference vector for the SVM scheme is established:

$$\vec{v}_{ref} = v_{ref} e^{j\theta} \tag{4.67}$$

where

$$\begin{cases} v_{ref} = \sqrt{(v_\alpha)^2 + (v_\beta)^2} \\ \theta = \tan^{-1} \dfrac{v_\beta}{v_\alpha} \end{cases} \tag{4.68}$$

With the reference vector in place, the modulation index m_a and sector number can be calculated by Equations (4.61) and (4.59), the dwell times can be determined by Equation (4.60), and the switching sequence can be designed according to Table 4-4. Finally, the gate signals for the six switches in the inverter can be generated. With the SVM

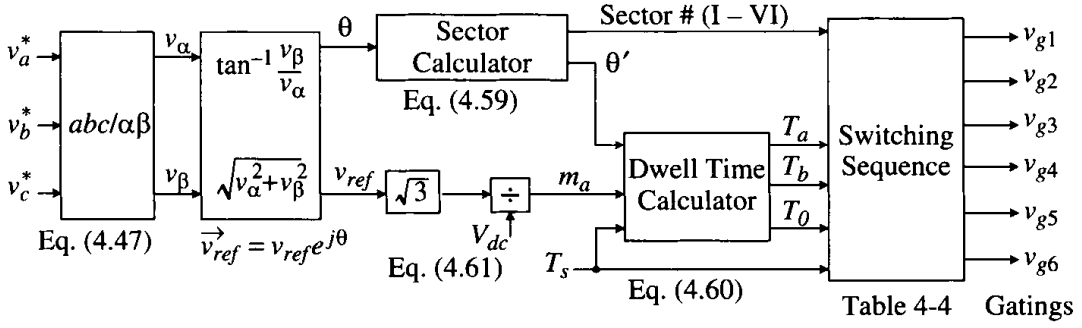


Figure 4-30. Block diagram for computer simulation and real-time digital implementation of the SVM algorithm.

Table 4-4. Seven-segment switching sequence

	Switching segment						
Sector	1	2	3	4	5	6	7
I	$\vec{V}_0$ OOO	$\vec{V}_1$ POO	$\vec{V}_2$ PPO	$\vec{V}_0$ PPP	$\vec{V}_2$ PPO	$\vec{V}_1$ POO	$\vec{V}_0$ OOO
II	$\vec{V}_0$ OOO	$\vec{V}_3$ OPO	$\vec{V}_2$ PPO	$\vec{V}_0$ PPP	$\vec{V}_2$ PPO	$\vec{V}_3$ OPO	$\vec{V}_0$ OOO
III	$\vec{V}_0$ OOO	$\vec{V}_3$ OPO	$\vec{V}_4$ OPP	$\vec{V}_0$ PPP	$\vec{V}_4$ OPP	$\vec{V}_3$ OPO	$\vec{V}_0$ OOO
IV	$\vec{V}_0$ OOO	$\vec{V}_5$ OOP	$\vec{V}_4$ OPP	$\vec{V}_0$ PPP	$\vec{V}_4$ OPP	$\vec{V}_5$ OOP	$\vec{V}_0$ OOO
V	$\vec{V}_0$ OOO	$\vec{V}_5$ OOP	$\vec{V}_6$ POP	$\vec{V}_0$ PPP	$\vec{V}_6$ POP	$\vec{V}_5$ OOP	$\vec{V}_0$ OOO
VI	$\vec{V}_0$ OOO	$\vec{V}_1$ POO	$\vec{V}_6$ POP	$\vec{V}_0$ PPP	$\vec{V}_6$ POP	$\vec{V}_1$ POO	$\vec{V}_0$ OOO

scheme, the fundamental frequency and the magnitude of the inverter output voltages v_a, v_b, and v_c are equal to those of the three-phase reference voltage v_a^*, v_b^*, and v_c^*. As result, the inverter output voltage is fully controllable by its references.

The simulated waveforms for the inverter output voltages and load current are shown in Figure 4-31. The inverter operates under the condition of $f = 60$ Hz, $f_{sw} = 720$ Hz, $T_s = 1/720$ sec, and $m_a = 0.8$ with a rated three-phase inductive load. The load power factor is 0.9 per phase. It can be observed that the waveform of the inverter line-to-line voltage v_{ab} is not half-wave symmetrical, that is, $v_{ab}(\omega t) \neq -v_{ab}(\omega t + \pi)$. Therefore, it contains even-order harmonics, such as 2nd, 4th, 8th, and 10th, in addition to odd-order harmonics. The THDs of v_{ab} and i_a are 80.2% and 8.37%, respectively.

The two-level voltage source converter technology is widely accepted in the variable-speed WECS, including doubly fed induction generator (DFIG), squirrel cage induction generator (SCIG), and synchronous generator (SG) based wind energy systems. The converter can be used either as a rectifier that converts three-phase AC voltage produced by the generator to a DC voltage or as a grid-tied inverter that delivers the active power from the generator and rectifier to the grid. The modulation schemes presented above are applicable to the converter that may operate as a rectifier or an inverter.

4.5 THREE-LEVEL NEUTRAL POINT CLAMPED CONVERTERS

The diode-clamped multilevel inverter employs clamping diodes and cascaded DC capacitors to produce AC voltage waveforms with multiple levels [2]. The inverter can be generally configured as a three-, four-, or five-level topology, and the three-level inverter, often known as neutral point clamped (NPC) inverter, has found wide practical application, especially in medium-voltage (MV) variable-speed drives [3]. The NPC

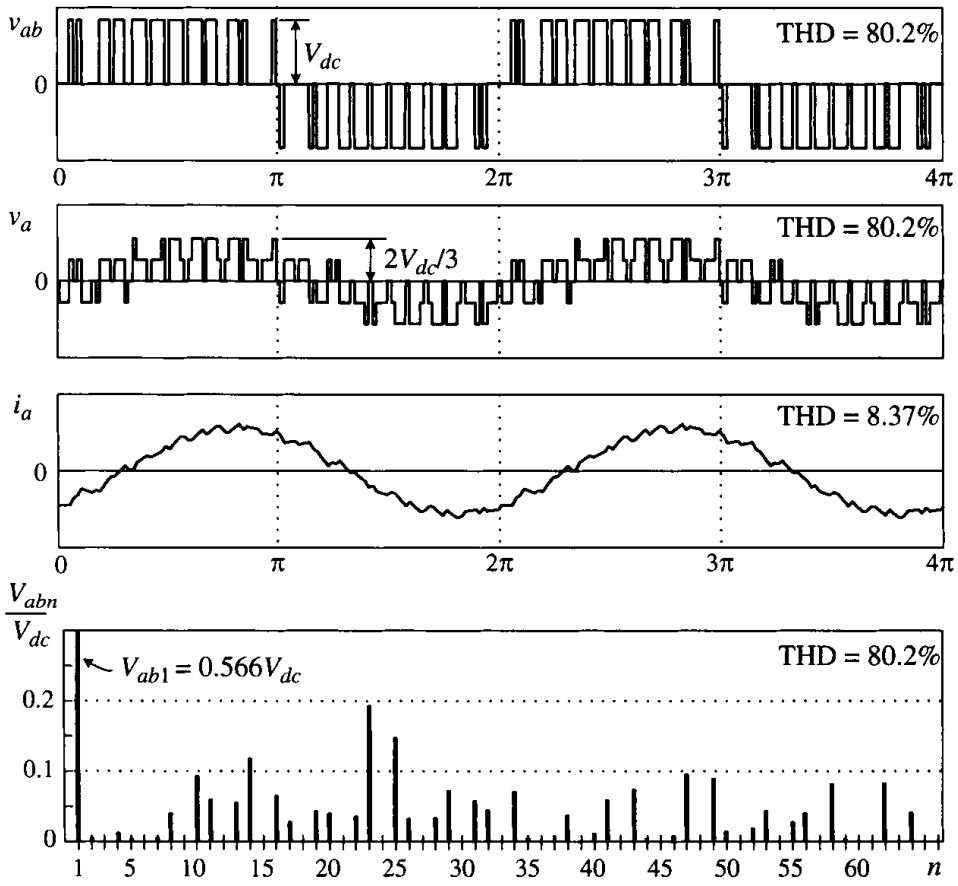


Figure 4-31. Inverter output waveforms produced by SVM scheme with f_1 = 60 Hz, f_{sw} = 720 Hz, and m_a = 0.8.

inverter is also a good candidate for MV (3 kV–4 kV) wind energy systems. The main features of the NPC inverter include reduced *dv/dt* and THD in its AC output voltages in comparison to the two-level inverter discussed earlier. More importantly, the inverter can be used in the MV wind energy systems without switching devices in series. For instance, the NPC inverter using 6 kV IGBT or IGCT devices is suitable for the 4 kV WECS, for which there is no need to connect the switches in series.

4.5.1 Converter Configuration

Figure 4.32 shows the simplified circuit diagram for the three-level NPC inverter. The inverter leg *a* is composed of four active switches S_1 to S_4 with four antiparallel diodes D_1 to D_4. In practice, either an IGBT or IGCT can be employed as a switching device.

On the DC side of the inverter, the DC bus capacitor is split into two, providing a neutral point *Z*. The diodes connected to the neutral point, D_{Z1} and D_{Z2}, are the clamping diodes. When switches S_2 and S_3 are turned on, the inverter output terminal *a* is connected to the neutral point through one of the clamping diodes. The voltage across each of the DC capacitors is *E*, which is normally equal to half of the total DC voltage V_{dc}.

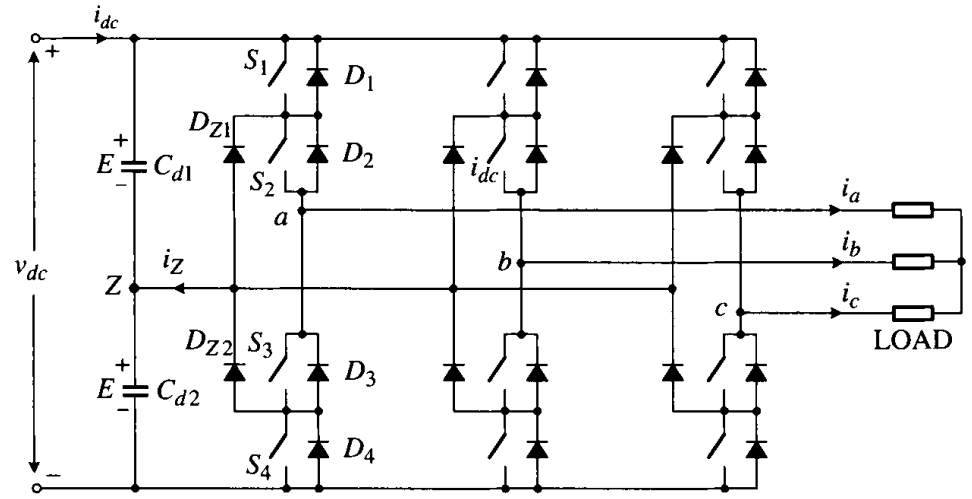


Figure 4-32. Three-level NPC inverter.

The operating status of the switches in the NPC inverter can be represented by switching states as shown in Table 4-5. Switching state P denotes that the upper two switches in leg a are on and the inverter terminal voltage v_{aZ}, which is the voltage at terminal a with respect to the neutral point Z, is $+E$, whereas N indicates that the lower two switches conduct, leading to $v_{aZ} = -E$.

Switching state O signifies that the inner two switches S_2 and S_3 are on and v_{aZ} is clamped to zero through the clamping diodes. Depending on the direction of load current i_a, one of the two clamping diodes is turned on. For instance, a positive load current ($i_a > 0$) forces D_{Z1} to turn on, and the terminal a is connected to the neutral point Z through the conduction of D_{Z1} and S_2.

It can be observed from Table 4.5 that switches S_1 and S_3 operate in a complementary manner. With one switched on, the other must be off. Similarly, S_2 and S_4 are a complementary pair as well.

Figure 4-33 shows an example of switching states and gate signal arrangements, where v_{g1} to v_{g4} are the gate signals for S_1 to S_4, respectively. The gate signals can be generated by carrier-based modulation, space vector modulation, or selective harmonic elimination schemes. The waveform for v_{aZ} has three voltage levels, $+E$, 0, and $-E$, based on which the inverter is referred to as a three-level inverter.

Table 4-5. Definition of switching states

	Device switching states (Phase a)				Inverter terminal voltage
Switching state	S_1	S_2	S_3	S_4	V_{aZ}
P	On	On	Off	Off	E
O	Off	On	On	Off	0
N	Off	Off	On	On	$-E$

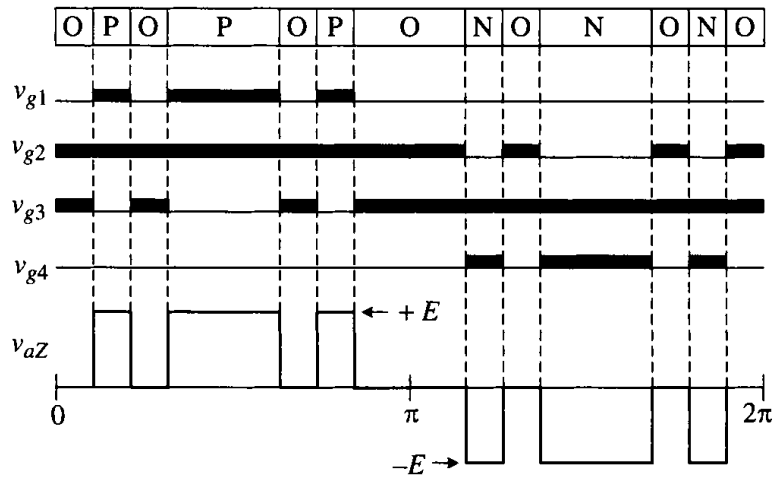


Figure 4-33. Switching states, gate signals, and inverter terminal voltage v_{aZ}.

Figure 4-34 shows how the line-to-line voltage waveform is obtained. The inverter terminal voltages v_{aZ}, v_{bZ}, and v_{cZ} are three-phase balanced with a phase shift of $2\pi/3$ between each other. The line-to-line voltage v_{ab} can be found from $v_{ab} = v_{aZ} - v_{bZ}$, which contains five voltage levels ($+2E$, $+E$, 0, $-E$, and $-2E$).

4.5.2 Space Vector Modulation

As indicated earlier, the operation of each inverter phase leg can be represented by three switching states P, O, and N. Taking all three phases into account, the inverter

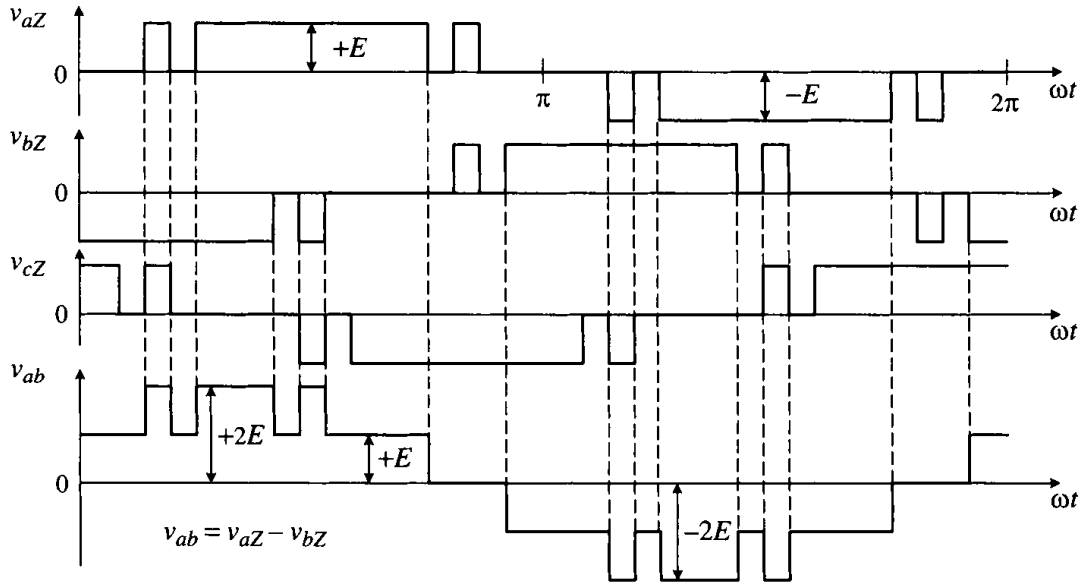


Figure 4-34. Inverter terminal and line-to-line voltage waveforms.

has a total of 27 possible combinations of switching states and 19 different stationary space vectors ($\vec{V}_0 \sim \vec{V}_{18}$) as shown in Figure 4-35. The principle of the space vector modulation for the NPC inverter is the same as that for the two-level inverter, but the implementation is more complicated. For a given position in space, the reference vector $\vec{v}_{ref}$ can be synthesized by three adjacent stationary vectors, based on which the dwell times for each of the selected stationary vectors can be calculated. According to the calculated dwell times, the turn-on times of the switches during a sampling period T_s can be determined, from which the switching sequence can be designed. The gate signals for the switches in the inverter can then be generated, based on which of the inverter output voltages are generated. When the reference vector $\vec{v}_{ref}$ rotates in space for one cycle, the inverter output voltage varies by one cycle at the fundamental frequency [3].

Case Study 4-4—Three-Level NPC Inverter with Space Vector Modulation. The main purpose of this case study is to investigate the harmonic profile of the three-level NPC inverter with space vector modulation, and then compare its THD profile with that of the two-level inverter.

Consider a 3 MW/4000 V three-level NPC inverter modulated by the SVM scheme. The inverter is loaded with a three-phase inductive load with a power factor of 0.9. Figure 4-36 shows the simulated waveforms for the inverter operating at $f = 60$ Hz, $T_s = 1/1080$ sec, $f_{sw,dev} = 1080/2 + 60/2 = 570$ Hz, and $m_a = 0.8$. The gate signals v_{g1} and v_{g4}

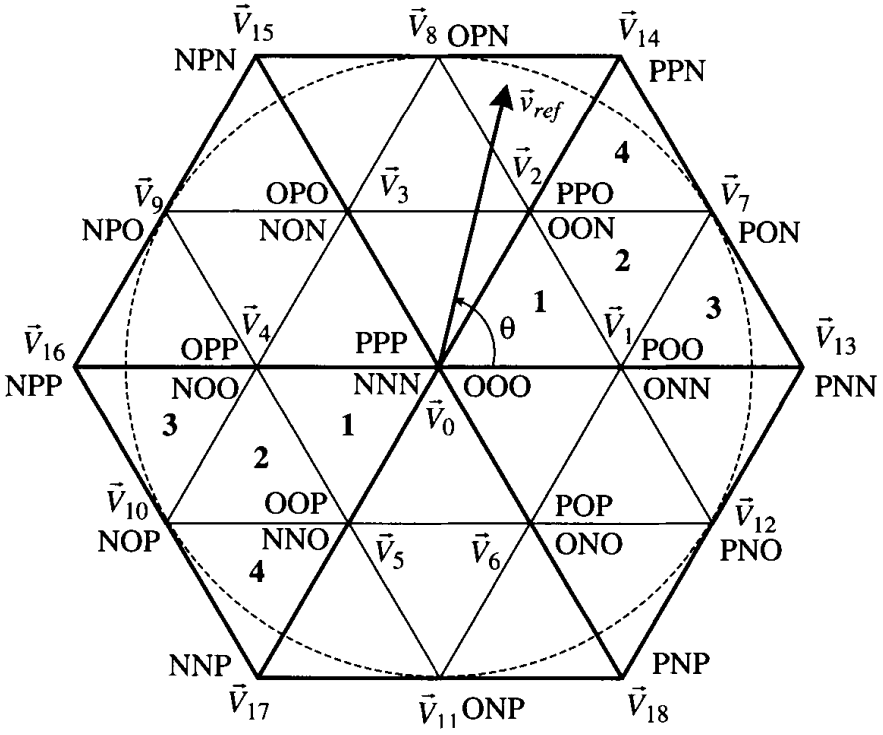


Figure 4-35. Space-vector diagram of the NPC inverter.

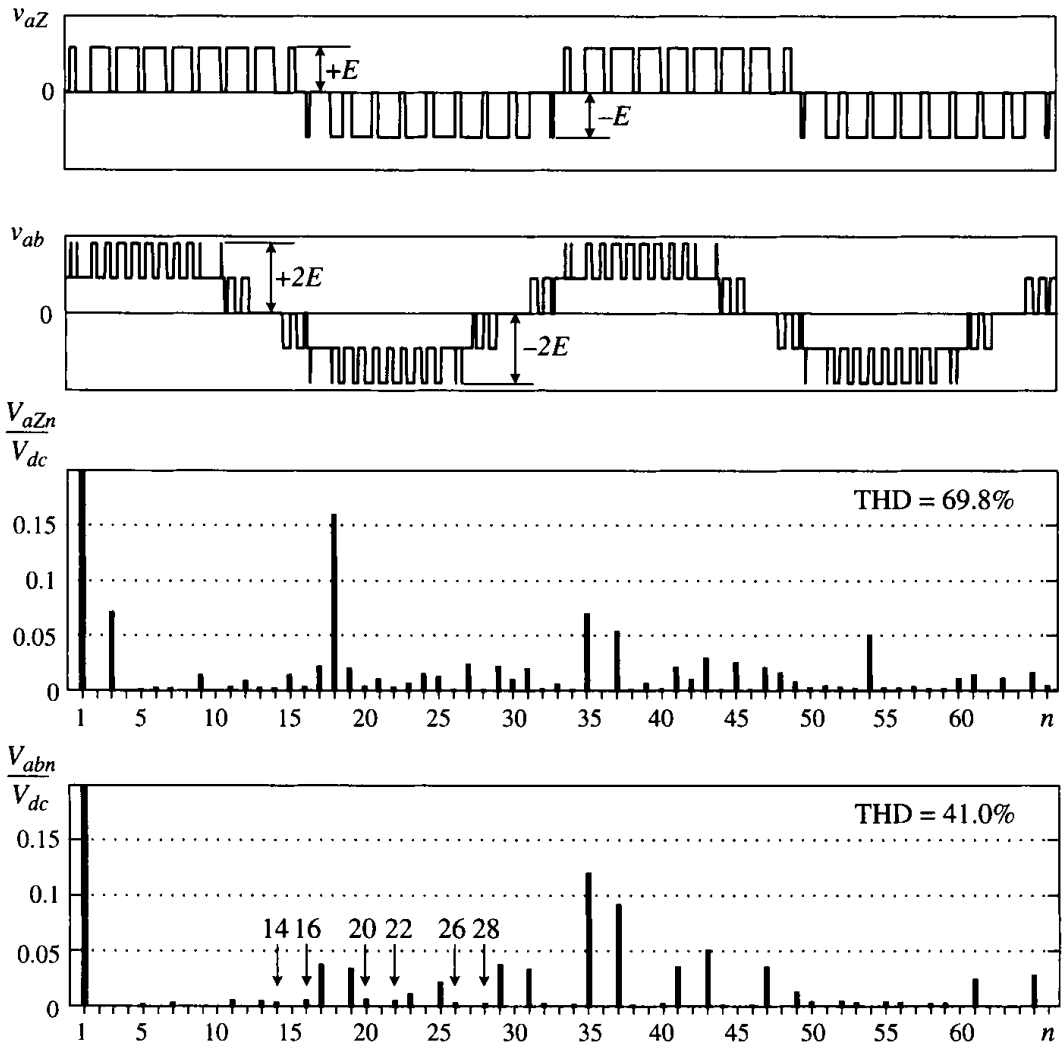


Figure 4-36. Simulated voltage waveforms of the NPC inverter (f_1 = 60 Hz, T_s = 1/1080 sec, $f_{sw,dev}$ = 570 Hz, and m_a = 0.8).

are for the switches S_1 and S_4 of the inverter circuit in Figure 4-32. Since the inner switches S_2 and S_3 operate complementarily with S_4 and S_1, their gatings are not shown.

The waveform of the inverter terminal voltage v_{aZ} is composed of three voltage levels, whereas the inverter line-to-line voltage v_{ab} has five voltage levels. The waveform for v_{aZ} contains triplen harmonics with the third and eighteenth being dominant. Since the triplen harmonics are of zero sequence, they do not appear in the line-to-line voltage v_{ab}. However, v_{ab} contains even-order harmonics such as the fourteenth and sixteenth in addition to odd-order harmonics. This is due to the fact that waveform of v_{ab} produced by the SVM scheme is not half-wave symmetrical.

The dominant harmonics in v_{ab} are the seventeenth and nineteenth, centered around the eighteenth harmonic, whose frequency is 1080 Hz. This frequency can be considered as the equivalent inverter switching frequency $f_{sw,inv}$, which is approximately twice the device switching frequency $f_{sw,dev}$.

Figure 4-37 shows the THD profile of the output line-to-line voltage produced by the two- and three-level inverters. Both inverters are modulated by the SVM schemes. The device switching frequencies for the two- and three-level inverters are 720 Hz and 570 Hz, respectively. It can be observed that the THD produced by the three-level inverter is much lower than that of the two-level inverter, which is one of the main advantages of the three-level converters.

The two-level inverter is often used in low-voltage (e.g., 690 V) WECS, whereas the NPC inverter is normally used in medium-voltage (e.g., 4000 V) WECS. For a given power rating, the NPC inverter has much lower output current than the two-level inverter. For example, the rated output current of a 3 MW/4000 V NPC inverter with unity power factor operation is 433 A in comparison to 2510 A for a 3 MW/690 V two-level inverter. The power cable that carries 2510 A current and runs from the top of the wind turbine tower to ground is much heavier and more costly than the 433 A cable and also has higher I^2R losses.

4.6 PWM CURRENT SOURCE CONVERTERS

Solid-state converters can be generally classified into voltage source converters (VSCs) and current source converters (CSCs). The voltage source converter produces a defined three-phase PWM output voltage waveform, whereas the current source converter outputs a defined PWM current waveform. The PWM current source converter features simple converter topology, nearly sinusoidal waveforms, and reliable short-circuit protection. It is particularly suitable for high-power applications such as megawatt variable-speed drives and wind energy conversion systems.

This section mainly deals with the modulation schemes for the current source inverter. Two modulation techniques for the inverter are discussed: selective harmonic

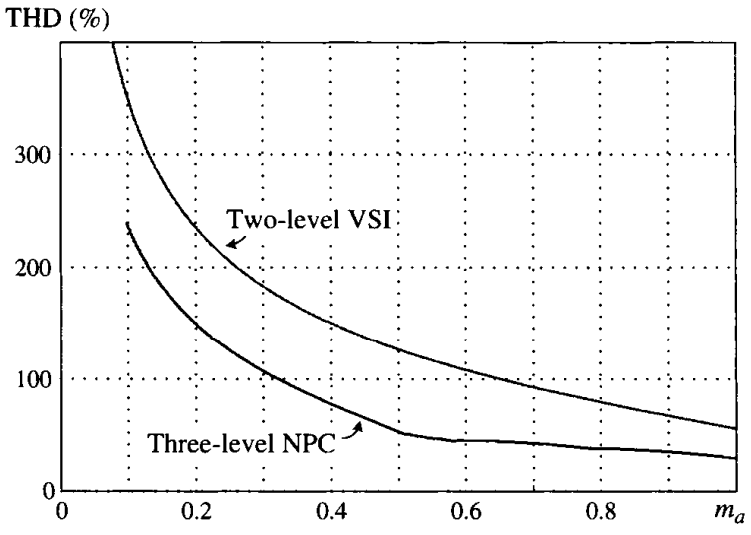


Figure 4-37. THD profile of the output voltage produced by the two-level and three-level NPC inverters.

elimination (SHE) and space vector modulation (SVM). These modulation schemes are developed for high-power inverters operating with a switching frequency below 1 kHz for reduction in switching losses.

4.6.1 Current Source Inverter Topology

A typical three-phase PWM current source inverter (CSI) circuit is shown in Figure 4-38. The inverter is composed of six IGCT devices of symmetrical type or reverse blocking IGBTs. The inverter requires a DC current source i_{dc} at its DC input and produces a defined PWM output current i_{aw}.

The current source inverter normally requires a three-phase capacitor C_i at its output to assist in the commutation of the switching devices. For instance, at the turn-off of switch S_1, the inverter PWM current i_{aw} falls to zero within a very short period of time. The capacitor provides a current path for the energy trapped in the phase-a load inductance. Otherwise, a high-voltage spike would be induced, causing damages to the switching devices. The capacitor also acts as a harmonic filter, improving the load current and voltage waveforms. The value of the capacitor is normally in the range of 0.3 to 0.6 per unit for an inverter with a switching frequency of 200 Hz to 400 Hz.

4.6.2 Selective Harmonic Elimination

The switching pattern design for the CSI should generally satisfy two conditions: (1) the DC current i_{dc} should be continuous and (2) the inverter PWM current i_{aw} should be defined. The two conditions can be translated into a switching constraint: at any instant of time (excluding commutation intervals) there are only two switches conducting: one in the top half of the bridge and the other in the bottom half. With only one

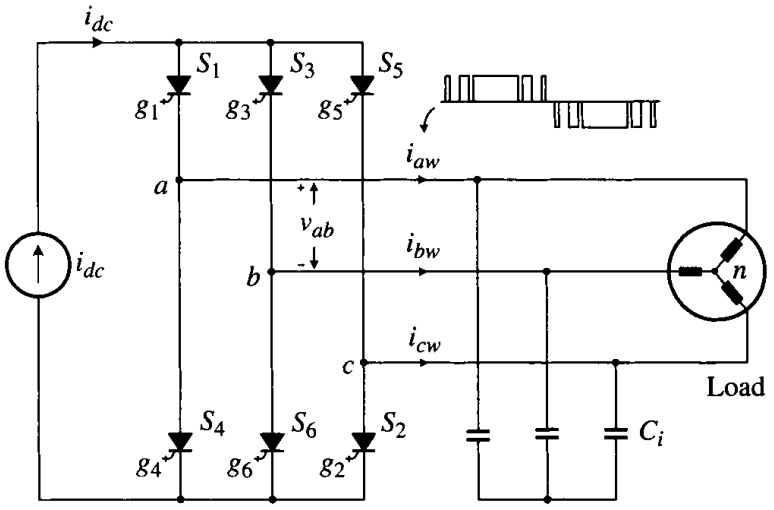


Figure 4-38. PWM current-source inverter.

switch turned on, the continuity of the DC current is lost. A very high voltage will be induced by the constant DC current, causing damage to the switching devices. If more than two devices are on simultaneously, the PWM current i_{aw} is not defined by the switching pattern. For instance, with S_1, S_2, and S_3 conducting at the same time, the currents in S_1 and S_3, which are the PWM currents in the inverter phases a and b, are load-dependent although the sum of the two currents is equal to i_{dc}.

Selective harmonic elimination is an offline modulation scheme, which is able to eliminate a number of low-order unwanted harmonics in the inverter PWM current i_{aw}. The switching angles are precalculated and then imported into a digital controller for implementation. Figure 4-39 shows a typical SHE waveform that satisfies the switching constraint for the CSI. There are five pulses per half-cycle ($N_p = 5$) with five switching angles in the first $\pi/2$ period. However, only two out of the five angles, θ_1 and θ_2, are independent. Given these two angles, all other switching angles can be calculated.

The two switching angles provide two degrees of freedom, which can be used to either eliminate two harmonics in i_{aw} without modulation index control or eliminate one harmonic and provide an adjustable modulation index m_a. The first option is preferred since the adjustment of i_{aw} is normally done by varying i_{dc}. The number of harmonics to be eliminated is then given by $k = (N_p - 1)/2$.

To determine switching angles such as θ_1 and θ_2 in Figure 4-39 for harmonic elimination, Fourier analysis can be performed, from which a set of nonlinear equations can be formulated [3]. These equations can be solved by numerical methods. Table 4-6 gives a list of switching angles for the elimination of up to four harmonics in i_{aw}. It is noted that the nonlinear equations for harmonic elimination may not always have a valid solution. If this happens, optimization techniques can be used to find optimal switching angles that minimize the magnitude of low-order harmonics.

4.6.3 Space Vector Modulation

In addition to the SHE scheme, the current source inverter can also be controlled by space vector modulation (SVM). This section presents the principle of the SVM scheme for current source inverters.

Switching States. As stated earlier, the PWM switching pattern for the CSI shown in Figure 4-38 must satisfy the constraint that only two switches in the inverter conduct at any time instant, one in the top half of the CSI bridge and the other in the

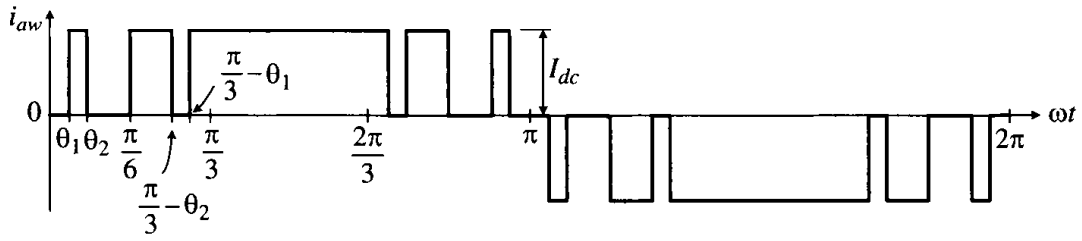


Figure 4-39. Selective harmonic elimination (SHE) scheme.

Table 4-6. SHE switching angles

Harmonics eliminated	Switching angles			
	θ_1	θ_2	θ_3	θ_4
5	18.00	—	—	—
7	21.43	—	—	—
11	24.55	—	—	—
5,7	7.93	13.75	—	—
5,11	12.96	19.14	—	—
5,13	14.48	21.12	—	—
5,7,11	2.24	5.60	21.26	—
5,7,13	4.21	8.04	22.45	—
5,7,17	6.91	11.96	25.57	—
5,7,11,13*	0.00	1.60	15.14	20.26
5,7,11,17	0.07	2.63	16.57	21.80
5,7,11,19	1.11	4.01	18.26	23.60

*Harmonics not completely eliminated but their magnitude minimized.

bottom half. Under this constraint, the three-phase inverter has a total of nine switching states, as listed in Table 4-7. These switching states can be classified as zero switching states and active switching states.

There are three zero switching states: (1,4), (3,6), and (5,2). The zero state (1,4) signifies that switches S_1 and S_4 in inverter-phase leg a conduct simultaneously and the other four switches in the inverter are off. The DC current source i_{dc} is bypassed, leading to $i_{aw} = i_{bw} = i_{cw} = 0$. This operating mode is often referred to as bypass operation.

There exist six active switching states. State (1,2) indicates that switch S_1 in leg a and S_2 in leg c are on. The DC current flows through S_1, the load, S_2, and then back to the DC source, resulting in $i_{aw} = I_{dc}$ and $i_{cw} = -I_{dc}$. The definition of the other five active states is also given in the table.

Table 4-7. Switching states and space vectors

Type	Switching state	On-state switch	Inverter PWM current			Space vector
			i_{aw}	i_{bw}	i_{cw}	
Zero states	(1,4)	S_1, S_4	0	0	0	$\vec{I}_0$
	(3,6)	S_3, S_6				
	(5,2)	S_5, S_2				
Active states	(6,1)	S_6, S_1	I_{dc}	$-I_{dc}$	0	$\vec{I}_1$
	(1,2)	S_1, S_2	I_{dc}	0	$-I_{dc}$	$\vec{I}_2$
	(2,3)	S_2, S_3	0	I_{dc}	$-I_{dc}$	$\vec{I}_3$
	(3,4)	S_3, S_4	$-I_{dc}$	I_{dc}	0	$\vec{I}_4$
	(4,5)	S_4, S_5	$-I_{dc}$	0	I_{dc}	$\vec{I}_5$
	(5,6)	S_5, S_6	0	$-I_{dc}$	I_{dc}	$\vec{I}_6$

Space Vectors. The active and zero switching states can be represented by active and zero space vectors, respectively. A space vector diagram for the CSI is shown in Figure 4-40, where $\vec{I}_1$ to $\vec{I}_6$ are the active vectors and $\vec{I}_0$ is the zero vector. The active vectors form a regular hexagon with six equal sectors, whereas the zero vector $\vec{I}_0$ lies at the center of the hexagon.

Assuming that the operation of the inverter in Figure 4-38 is three-phase balanced, that is,

$$i_{aw}(t) + i_{bw}(t) + i_{cw}(t) = 0 \tag{4.69}$$

where i_{aw}, i_{bw}, and i_{cw} are the instantaneous PWM output currents in the inverter phases a, b, and c, respectively, the three-phase currents can be transformed into two-phase currents in the α-β frame:

$$\begin{bmatrix} i_\alpha(t) \\ i_\beta(t) \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} i_{aw}(t) \\ i_{bw}(t) \\ i_{cw}(t) \end{bmatrix} \tag{4.70}$$

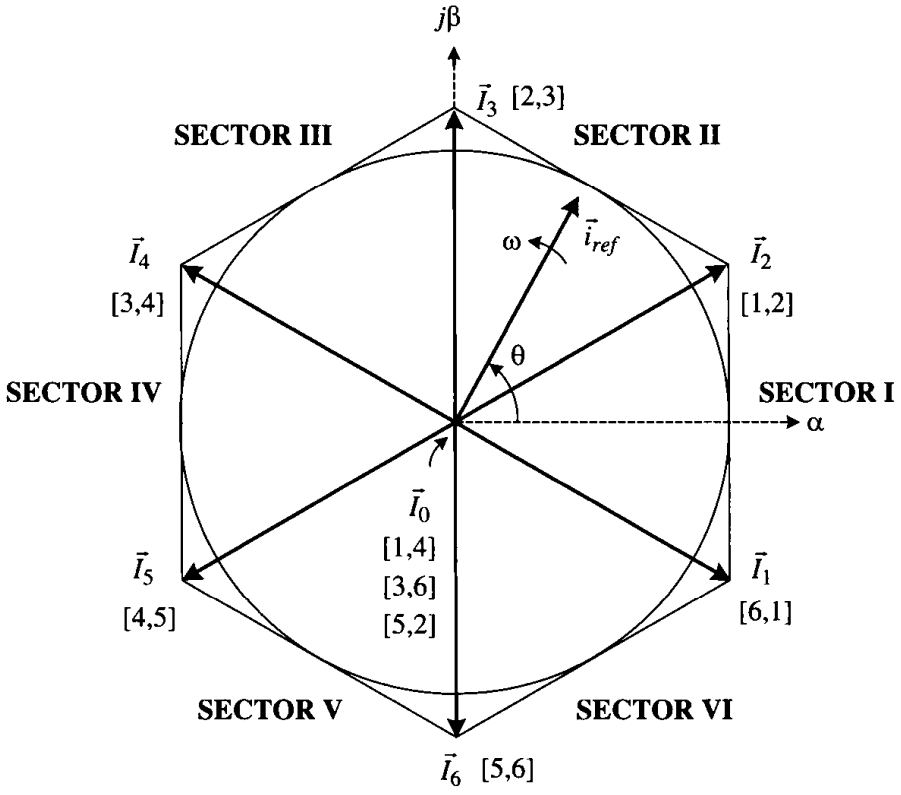


Figure 4-40. Space-vector diagram for the current-source inverter.

A current-space vector can be generally expressed in terms of the two-phase currents as

$$\vec{i}(t) = i_\alpha(t) + j i_\beta(t) \tag{4.71}$$

Substituting (4.70) into (4.71), $\vec{i}(t)$ can be expressed in terms of i_{aw}, i_{bw}, and i_{cw}:

$$\vec{i}(t) = \frac{2}{3}\left[i_{aw}(t)e^{j0} + i_{bw}(t)e^{j2\pi/3} + i_{cw}(t)e^{j4\pi/3} \right] \tag{4.72}$$

For the active state (6,1), S_1 and S_6 are turned on, and the inverter PWM currents are

$$i_{aw}(t) = I_{dc},\ i_{bw}(t) = -I_{dc} \text{ and } i_{cw}(t) = 0 \tag{4.73}$$

Substituting (4.73) into (4.72) yields

$$\vec{I}_1 = \frac{2}{\sqrt{3}} I_{dc}\, e^{j(-\pi/6)} \tag{4.74}$$

Similarly, the other five active vectors can be derived. The active vectors can be expressed as

$$\vec{I}_k = \frac{2}{\sqrt{3}} I_{dc}\, e^{j\left((k-1)\frac{\pi}{3}-\frac{\pi}{6}\right)} \qquad \text{for } k = 1, 2, ..., 6. \tag{4.75}$$

Note that the active and zero vectors do not move in space, and thus are referred to as stationary vectors. On the contrary, the current reference vector $\vec{i}_{ref}$ in Figure 4-40 rotates in space at an angular velocity

$$\omega = 2\pi f \tag{4.76}$$

where f is the fundamental frequency of the inverter output current i_{aw}. The angular displacement between $\vec{i}_{ref}$ and the α-axis of the α-β frame can be obtained by

$$\theta(t) = \int_0^t \omega(t)\, dt + \theta_0 \tag{4.77}$$

For a given length and position, $\vec{i}_{ref}$ can be synthesized by three nearby stationary vectors, based on which the switching states of the inverter can be selected and gate signals for the active switches can be generated. When $\vec{i}_{ref}$ passes through sectors one by one, different sets of switches are turned on or off. As a result, when $\vec{i}_{ref}$ rotates one revolution in space, the inverter output current varies one cycle over time. The frequency and magnitude of the inverter output current correspond to the rotating speed and length of $\vec{i}_{ref}$, respectively.

Dwell Time Calculation. As indicated above, the reference $\vec{i}_{ref}$ can be synthesized by three stationary vectors. The dwell time for the stationary vectors essentially

represents the duty-cycle time (on-state or off-state time) of the chosen switches during a sampling period T_s. The dwell time calculation is based on the ampere-second balancing principle, that is, the product of the reference vector $\vec{i}_{ref}$ and sampling period T_s equals the sum of the current vectors multiplied by the time interval of chosen space vectors. Assuming that the sampling period T_s is sufficiently small, the reference vector $\vec{i}_{ref}$ can be considered constant during T_s. Under this assumption, $\vec{i}_{ref}$ can be approximated by two adjacent active vectors and a zero vector. For example, with $\vec{i}_{ref}$ falling into Sector I as shown in Figure 4-41, it can be synthesized by $\vec{I}_1$, $\vec{I}_2$, and $\vec{I}_0$. The ampere-second balancing equation is thus given by

$$\begin{cases} \vec{i}_{ref} T_s = \vec{I}_1 T_1 + \vec{I}_2 T_2 + \vec{I}_0 T_0 \\ T_s = T_1 + T_2 + T_0 \end{cases} \tag{4.78}$$

where T_1, T_2 and T_0 are the dwell times for the vectors $\vec{I}_1$, $\vec{I}_2$, and $\vec{I}_0$, respectively. Substituting

$$\vec{i}_{ref} = i_{ref} e^{j\theta},\ \vec{I}_1 = \frac{2}{\sqrt{3}} I_{dc} e^{-j\frac{\pi}{6}},\ \vec{I}_2 = \frac{2}{\sqrt{3}} I_{dc} e^{j\frac{\pi}{6}},\ \text{and}\ \vec{I}_0 = 0 \tag{4.79}$$

into (4.78) and then splitting the resultant equation into the real (α-axis) and imaginary (β-axis) components leads to

$$\begin{cases} \text{Re}: & i_{ref}(\cos\theta) T_s = I_{dc}(T_1 + T_2) \\ \text{Im}: & i_{ref}(\sin\theta) T_s = \frac{1}{\sqrt{3}} I_{dc}(-T_1 + T_2) \end{cases} \tag{4.80}$$

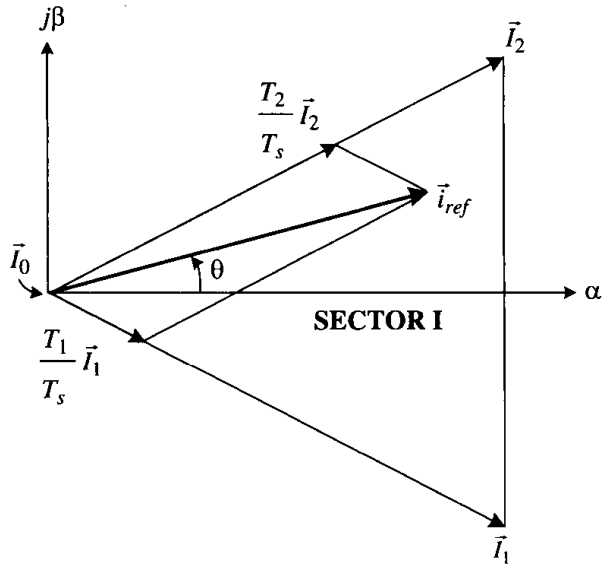


Figure 4-41. Synthesis of $\vec{i}_{ref}$ by $\vec{I}_1$, $\vec{I}_2$, and $\vec{I}_0$.

Solving (4.80) together with $T_s = T_1 + T_2 + T_0$ gives

$$\begin{cases} T_1 = m_a \sin(\pi/6 - \theta) T_s \\ T_2 = m_a \sin(\pi/6 + \theta) T_s \\ T_0 = T_s - T_1 - T_2 \end{cases} \qquad \text{for } -\pi/6 \le \theta < \pi/6 \tag{4.81}$$

where m_a is the modulation index, given by

$$m_a = \frac{i_{ref}}{I_{dc}} = \frac{\hat{I}_{aw1}}{I_{dc}} \tag{4.82}$$

in which $\hat{I}_{aw1}$ is the peak value of the fundamental-frequency component in i_{aw}.

Note that although Equation (4.81) is derived when $\vec{i}_{ref}$ is in sector I, it can also be used when $\vec{i}_{ref}$ is in other sectors provided that a multiple of $\pi/3$ is subtracted from the actual angular displacement θ such that the modified angle θ' falls into the range of $-\pi/6 \le \theta' < \pi/6$ for use in the equation, that is,

$$\theta' = \theta - (k-1)\pi/3 \qquad \text{for } -\pi/6 \le \theta' < \pi/6 \tag{4.83}$$

where $k = 1, 2, \ldots, 6$ for sectors I, II, . . . , VI, respectively.

The maximum length of the reference vector, $i_{ref,\max}$, corresponds to the radius of the largest circle that can be inscribed within the hexagon as shown in Figure 4-40. Since the hexagon is formed by the six active vectors having a length of $2I_{dc}/\sqrt{3}$, $i_{ref,\max}$ can be found from

$$i_{ref,\max} = \frac{2I_{dc}}{\sqrt{3}} \times \frac{\sqrt{3}}{2} = I_{dc} \tag{4.84}$$

Substituting (4.84) into (4.82) gives the maximum modulation index

$$m_{a,\max} = 1 \tag{4.85}$$

from which the modulation index is in the range of

$$0 \le m_a \le 1 \tag{4.86}$$

Switching Sequence. Similar to the space vector modulation for the two-level VSI, the switching sequence design for the CSI should satisfy the following two requirements for the minimization of switching frequencies:

1. The transition from one switching state to the next involves only two switches, one being switched on and the other switched off.
2. The transition for $\vec{i}_{ref}$ moving from one sector to the next requires the minimum number of switchings.

Figure 4-42 shows a typical three-segment sequence for the reference vector $\vec{i}_{ref}$ residing in sector I, where v_{g1} to v_{g6} are the gate signals for switches S_1 to S_6, respectively. The reference vector $\vec{i}_{ref}$ is synthesized by $\vec{I}_1$, $\vec{I}_2$, and $\vec{I}_0$. The sampling period T_s is divided into three segments composed of T_1, T_2, and T_0. The switching states for vectors $\vec{I}_1$ and $\vec{I}_2$ are (6,1) and (1,2), and their corresponding on-state switch pairs are (S_6, S_1) and (S_1, S_2). The zero state (1,4) is selected for $\vec{I}_0$ such that design requirement 1 above is satisfied.

Case Study 4-5—Current Source Inverter with Space Vector Modulation. Consider a 1 MW/4000 V CSI using the space vector modulation. The inverter operates at f = 60 Hz, f_{sp} = 1080 Hz, and f_{sw} = 540 Hz with m_a = 1. The filter capacitor C_i is 0.3 pu per phase. The inverter is loaded with a three-phase balanced inductive load having a resistance of 1.0 pu and an inductance of 0.1 pu per phase. The DC current of the inverter is adjusted such that the fundamental-frequency inverter output current i_{awl} is rated. The simulated waveforms for the converter are shown in Figure 4-43, where i_{aw} is the inverter PWM current and v_{ab} is the line-to-line output voltage of the inverter.

The spectra for i_{aw} and v_{ab} are also shown in the figure, where I_{awn} is the rms value of the nth-order harmonic current in i_{aw} and $I_{awl,max}$ is the maximum rms fundamental-frequency current that can be found from Equation (4.82):

$$I_{awl,max} = \frac{m_{a,max} \times I_{dc}}{\sqrt{2}} = 0.707 I_{dc} \qquad \text{for } m_{a,max} = 1 \tag{4.87}$$

The PWM current i_{aw} contains no even-order harmonics and its THD is 45.7%. Similar to the two-level inverter, the SVM current source inverter produces low-order harmon-

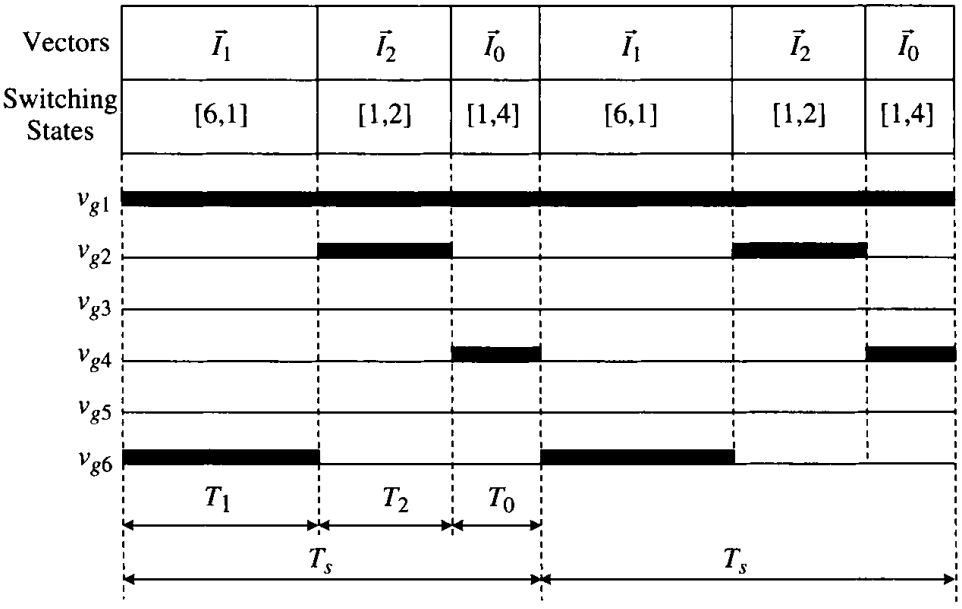


Figure 4-42. Switching sequence for $\vec{i}_{ref}$ in sector I.

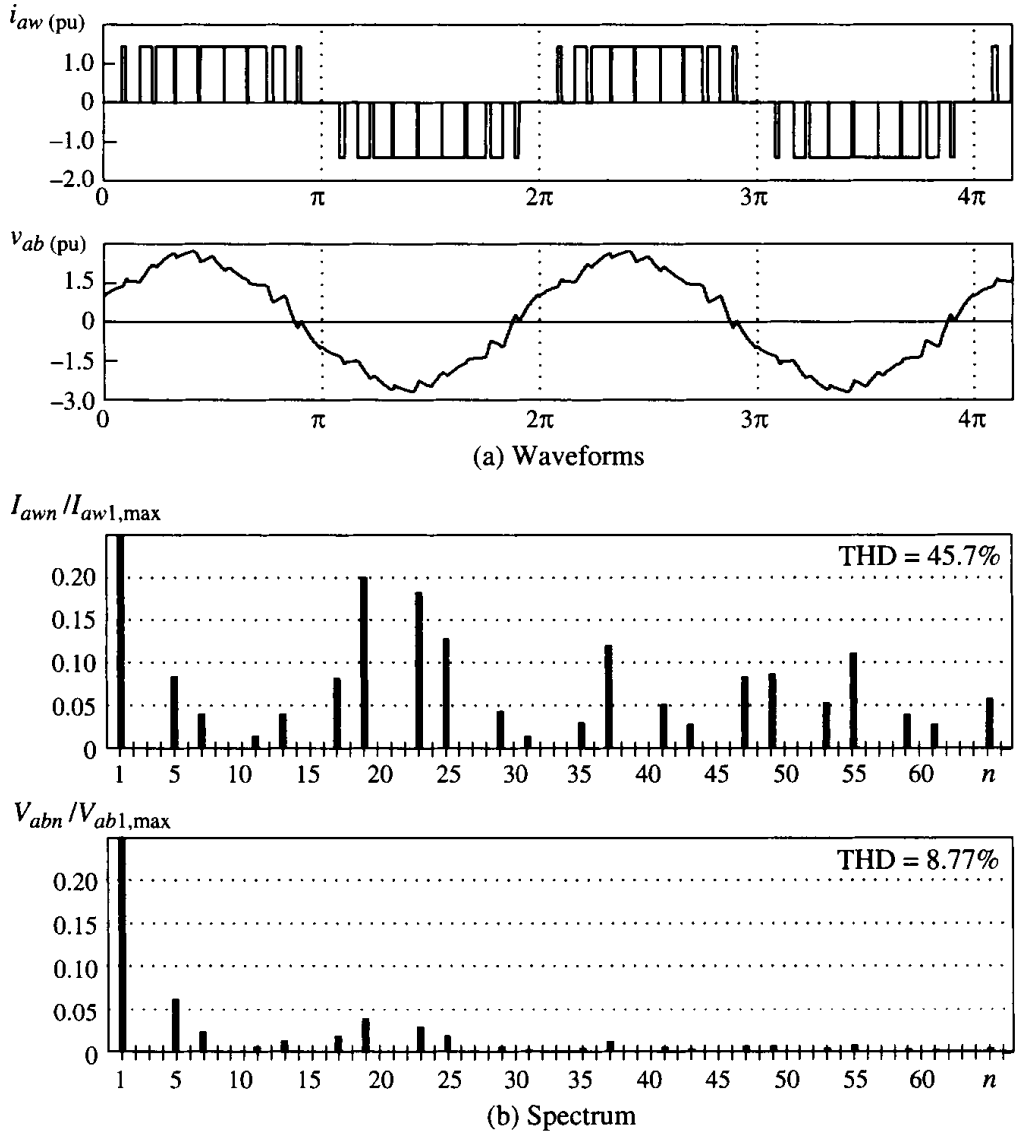


Figure 4-43. Waveforms in a 1 MVA CSI using the SVM scheme (f_1 = 60 Hz, f_{sw} = 540 Hz, m_a = 1, and C_i = 0.3 pu).

ics such as the fifth and seventh. The magnitude of these harmonics can be substantially reduced by using multisampling techniques [7]. Unlike the voltage source inverters, the current source inverter does not have high *dv/dt* in its output voltage waveform, and the THD of its line-to-line voltage v_{ab} is only 8.77%.

4.6.4 PWM Current Source Rectifier

Figure 4.44 shows a typical configuration of a PWM current source rectifier (CSR) in a wind energy conversion system. Like the current source inverter (CSI), the PWM rectifier requires a filter capacitor C_r to assist the commutation of switching devices

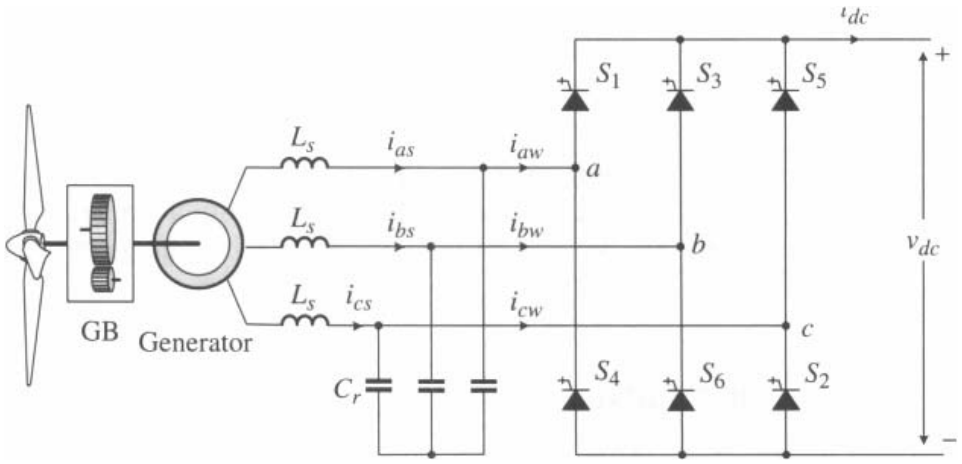


Figure 4-44. Typical configuration of a PWM current-source rectifier in a wind energy system.

and filter out current harmonics. The capacitor size is dependent on a number of factors such as the rectifier switching frequency, LC resonant mode, required line current THD, and type of generator. It is normally in the range of 0.1 to 0.3 pu for WECS with a large synchronous generator and 0.3 to 0.6 pu for induction-generator-based WECS with a switching frequency of a few hundred hertz. Both the SHE and SVM schemes developed for the CSI can be used for the CSR.

The DC output voltage v_{dc} of the rectifier can be adjusted by two methods: modulation index (m_a) control and delay angle (α) control. The operating principle of delay angle control is the same as that of phase-controlled SCR rectifiers.

The input active power of the rectifier can be expressed as

$$P_{ac} = 3 V_{a1} I_{aw1} \cos\alpha = \sqrt{3}\, V_{ab1} I_{aw1} \cos\alpha \tag{4.88}$$

where V_{a1}, V_{ab1}, and I_{aw1} are the fundamental-frequency rms phase input voltage, line-to-line input voltage, and PWM input current of the rectifier, respectively. The delay angle α is defined as the angle between V_{a1} and I_{aw1}, respectively. The DC output power is given by

$$P_{dc} = V_{dc} I_{dc} \tag{4.89}$$

where V_{dc} and I_{dc} are the average DC output voltage and current, respectively. Neglecting the power losses in the rectifier, the AC input power is equal to the DC output power:

$$\sqrt{3}\, V_{ab1} I_{aw1} \cos\alpha = V_{dc} I_{dc} \tag{4.90}$$

from which

$$V_{dc} = \sqrt{3/2}\; V_{ab1} m_a \cos\alpha \tag{4.91}$$

where

$$m_a = \hat{I}_{aw1} / I_{dc} = \sqrt{2} I_{aw1} / I_{dc} \tag{4.92}$$

Equation (4.91) illustrates that for a given line-to-line input voltage V_{ab1}, the average DC voltage of the rectifier can be controlled by both modulation index m_a and delay angle α. The above results will be used for the analysis of wind energy systems discussed in Chapters 7 and 9.

4.7 CONTROL OF GRID-CONNECTED INVERTER

Most commercial wind turbines deliver the generated power to the electric grid through power converters. A typical grid-connected (grid-tied) inverter for wind energy applications is shown in Figure 4-45, where a two-level voltage source inverter is used as an example. The inverter is connected to the grid through a line inductance L_g, which represents the leakage inductance of the transformer, if any, and the line reactor of 0.05 to 0.1 per unit, which is normally added to the system for the reduction of line current distortion. The line resistance is negligibly small and has little impact on the system performance. It is, therefore, omitted in the analysis.

The grid-tied inverter can be modulated by the PWM schemes presented in the previous sections, such as the space vector modulation scheme. The inverter is a boost converter by nature, and its average DC voltage V_{dc} can be derived from Equation (4.63) and given by

$$V_{dc} = \frac{\sqrt{6}\, V_{ai1}}{m_a} \qquad \text{for } 0 < m_a \leq 1 \tag{4.93}$$

where m_a is the modulation index and V_{ai1} is the rms value of the fundamental-frequency component of the inverter phase (phase-a) voltage v_{ai1}. Assuming that V_{ai1}

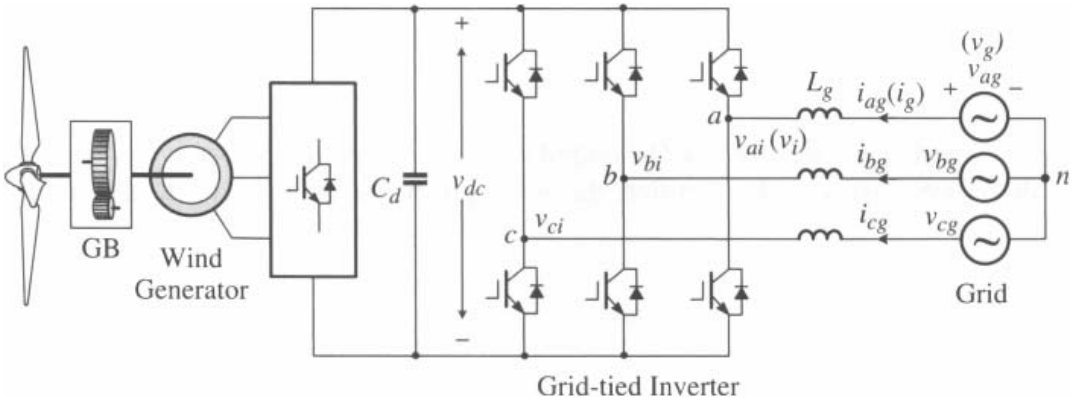


Figure 4-45. Grid-connected inverter in a wind energy system.

is equal to the rms value of grid phase voltage V_g, which can be considered constant, the DC voltage can be boosted to a high value by a small m_a.

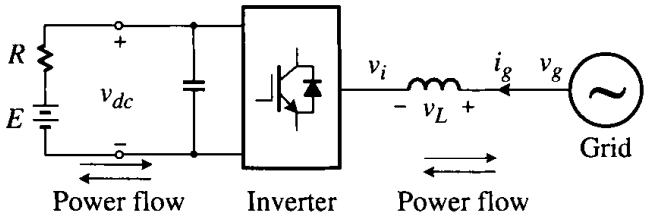
Figure 4-46a shows a simplified diagram for a wind energy system, in which the wind turbine, generator, and rectifier are replaced by a battery in series with a small resistance that represents the power losses in the system. The power flow between the inverter and grid is bidirectional. Power can be transferred from the grid to the DC circuit of the inverter, or vice versa. For wind energy applications, the power is normally delivered from the inverter to the grid. The active power of the system delivered to the grid can be calculated by

$$P_g = 3\, V_g I_g \cos \varphi_g \tag{4.94}$$

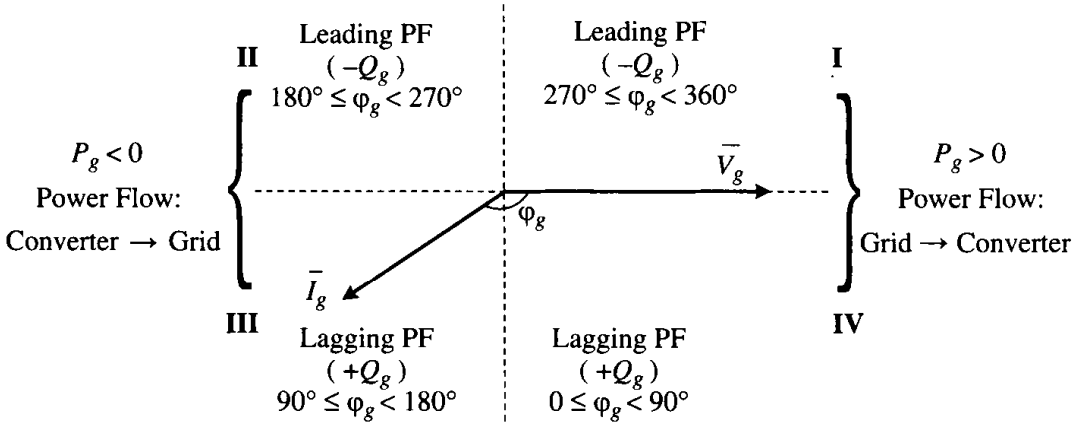
where φ_g is the grid power factor angle, defined by

$$\varphi_g = \angle \bar{V}_g - \angle \bar{I}_g \tag{4.95}$$

The grid power factor can be unity, leading, or lagging, as shown in Figure 4-46b. It is often required by the grid operator that a wind energy system provide a controllable reactive power to the grid to support the grid voltage in addition to the active power production. Therefore, a wind energy system can operate with the power factor angle in the range of $90° \leq \varphi_g < 270°$.



(a) Simplified diagram



(b) Phasor diagram and PF

Figure 4-46. Simplified system diagram and definition of power factor.

4.7.1 Voltage Oriented Control (VOC)

The grid-connected inverter can be controlled with various schemes. One of the schemes is known as voltage oriented control (VOC), as shown in Figure 4-47. This scheme is based on transformation between the *abc* stationary reference frame and *dq* synchronous frame as introduced in Chapter 3. The control algorithm is implemented in the grid-voltage synchronous reference frame, where all the variables are of DC components in steady state. This facilitates the design and control of the inverter.

To realize the VOC, the grid voltage is measured and its angle θ_g is detected for the voltage orientation. This angle is used for the transformation of variables from the *abc* stationary frame to the *dq* synchronous frame through the *abc*/*dq* transformation or from the synchronous frame back to the stationary frame through the *dq*/*abc* transformation, as shown in Figure 4-47. Various methods are available to detect the grid voltage angle θ_g. Assuming that the grid voltages, v_{ag}, v_{bg}, and v_{cg}, are three-phase balanced sinusoidal waveforms, θ_g can be obtained by

$$\theta_g = \tan^{-1}\frac{v_\beta}{v_\alpha} \tag{4.96}$$

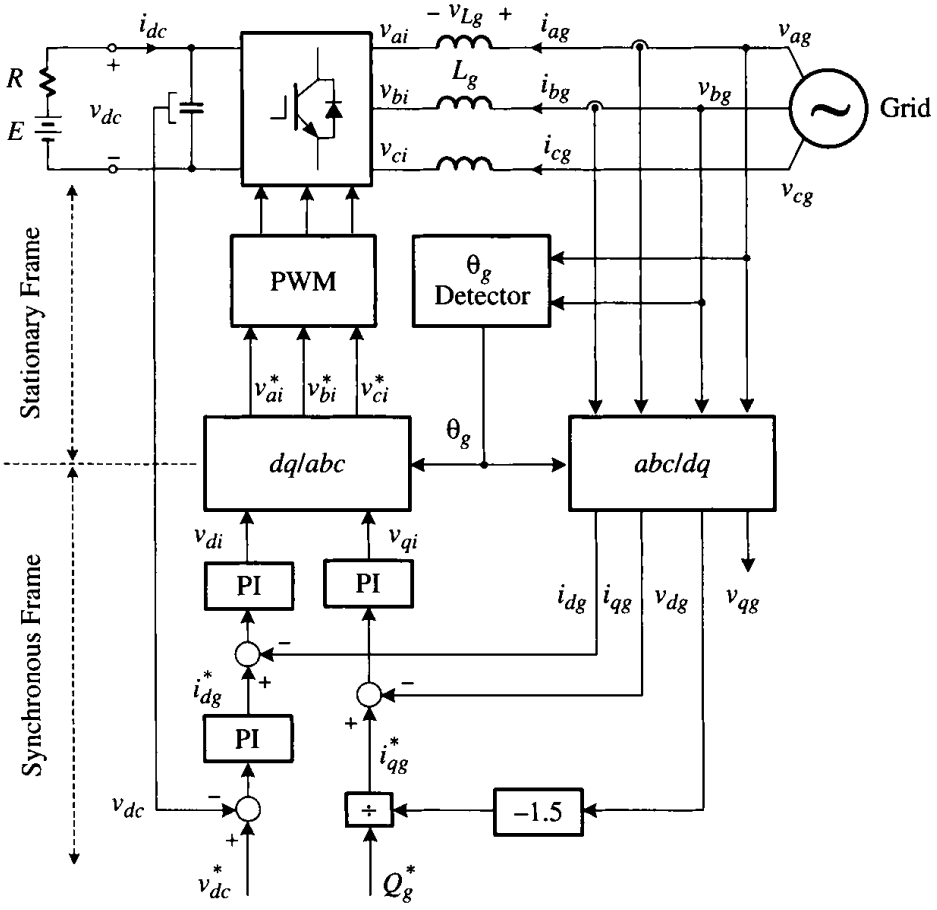


Figure 4-47. Block diagram of voltage-oriented control (VOC).

where v_β and v_β can be obtained by the $abc/\alpha\beta$ transformation:

$$\begin{cases} v_\alpha = \dfrac{2}{3}\left(v_{ag} - \dfrac{1}{2}v_{bg} - \dfrac{1}{2}v_{cg}\right) = v_{ag} \\ v_\beta = \dfrac{2}{3}\left(\dfrac{\sqrt{3}}{2}v_{bg} - \dfrac{\sqrt{3}}{2}v_{cg}\right) = \dfrac{\sqrt{3}}{3}\left(v_{ag} + 2v_{bg}\right) \end{cases} \quad \text{for} \quad v_{ag} + v_{bg} + v_{cg} = 0 \qquad (4.97)$$

The above equation indicates that there is no need to measure the phase-c grid voltage v_{cg} as shown in Figure 4-47. In practice, the grid voltage may contain harmonics and be distorted, so digital filters or phase-locked loops (PLLs) may be used for the detection of the grid voltage angle θ_g.

There are three feedback control loops in the system: two inner current loops for the accurate control of the dq-axis currents i_{dg} and i_{qg}, and one outer DC voltage feedback loop for the control of DC voltage v_{dc}. With the VOC scheme, the three-phase line currents in the abc stationary frame i_{ag}, i_{bg}, and i_{cg} are transformed to the two-phase currents i_{dg} and i_{qg} in the dq synchronous frame, which are the active and reactive components of the three-phase line currents, respectively. The independent control of these two components provides an effective means for the independent control of system active and reactive power.

To achieve the VOC control scheme, the d-axis of the synchronous frame is aligned with the grid voltage vector, therefore the d-axis grid voltage is equal to its magnitude ($v_{dg} = v_g$), and the resultant q-axis voltage v_{qg} is then equal to zero ($v_{qg} = \sqrt{v_g^2 - v_{dg}^2} = 0$), from which the active and reactive power of the system can be calculated by

$$\begin{cases} P_g = \dfrac{3}{2}(v_{dg}i_{dg} + v_{qg}i_{qg}) = \dfrac{3}{2}v_{dg}i_{dg} \\ Q_g = \dfrac{3}{2}(v_{qg}i_{dg} - v_{dg}i_{qg}) = -\dfrac{3}{2}v_{dg}i_{qg} \end{cases} \quad \text{for } v_{qg} = 0 \qquad (4.98)$$

The q-axis current reference i_{qg}^* can then be obtained from

$$i_{qg}^* = \frac{Q_g^*}{-1.5v_{dg}} \qquad (4.99)$$

where Q_g^* is the reference for the reactive power, which can be set to zero for unity power factor operation, a negative value for leading power factor operation, or a positive value for lagging power factor operation.

The d-axis current reference i_{dg}^*, which represents the active power of the system, is generated by the PI controller for DC voltage control. When the inverter operates in steady state, the DC voltage v_{dc} of the inverter is kept constant at a value set by its reference voltage v_{dc}^*. The PI controller generates the reference current i_{dg}^* according to the operating conditions. Neglecting the losses in the inverter, the active power on the AC side of the inverter is equal to the DC-side power, that is,

$$P_g = \frac{3}{2}v_{dg}i_{dg} = v_{dc}i_{dc} \qquad (4.100)$$

As mentioned earlier, the power flow of the inverter system is bidirectional. When the active power is delivered from the grid to the DC circuit, the inverter operates in a rectifying mode ($P_g > 0$), whereas when the power is transferred from the DC circuit to the grid ($P_g < 0$), the inverter is in an inverting mode. The control system will automatically switch between the two operating modes and, therefore, no extra measures should be taken for the controller. To study the bidirectional power flow, the DC load of the inverter can be modeled by a resistor R in series with a battery E, as shown in Figure 4-47. Since the average DC voltage V_{dc} of the inverter is set by its reference v^*_{dc} and is kept constant by the PI controller, the direction of the power flow is set by the difference between E and V_{dc} according to the following conditions

$$\begin{cases} E < V_{dc} \rightarrow I_{dc} > 0 \rightarrow P_g > 0 \rightarrow \text{Power from grid to load (rectifying mode)} \\ E > V_{dc} \rightarrow I_{dc} < 0 \rightarrow P_g < 0 \rightarrow \text{Power from load to grid (inverting mode)} \\ E = V_{dc} \rightarrow I_{dc} = 0 \rightarrow P_g = 0 \rightarrow \text{No power flow between the DC circuit and the grid} \end{cases} \tag{4.101}$$

To determine an appropriate DC voltage reference reference v^*_{dc}, one should take system transients and possible grid voltage variations into account. Assume that when the inverter operates under the rated conditions, the modulation index m_a is 0.8. The DC reference voltage can then be set by

$$V^*_{dc} = \frac{\sqrt{6}V_{ail}}{m_a} = \frac{\sqrt{6}}{0.8} = 3.06 \text{ pu} \quad (V_{ail} = 1 \text{ pu}) \tag{4.102}$$

which gives around a 20% voltage margin for adjustment during the transients and grid voltage variations.

4.7.2 VOC with Decoupled Controller

To further investigate the VOC scheme, the state equation for the grid-side circuit of the inverter in the *abc* stationary reference frame can be expressed as

$$\begin{cases} \dfrac{di_{ag}}{dt} = \left(v_{ag} - v_{ai}\right)/L_g \\ \dfrac{di_{bg}}{dt} = \left(v_{bg} - v_{bi}\right)/L_g \\ \dfrac{di_{cg}}{dt} = \left(v_{cg} - v_{ci}\right)/L_g \end{cases} \tag{4.103}$$

The above equations can be transformed into the *dq* synchronous reference frame

$$\begin{cases} \dfrac{di_{dg}}{dt} = \left(v_{dg} - v_{di} + \omega_g L_g i_{qg}\right)/ L_g \\ \dfrac{di_{qg}}{dt} = \left(v_{qg} - v_{qi} - \omega_g L_g i_{dg}\right)/ L_g \end{cases} \tag{4.104}$$

where ω_g is the speed of the synchronous reference frame, which is also the angular frequency of the grid, and $\omega_g L_g i_{qg}$ and $\omega_g L_g i_{dg}$ are the induced speed voltages due to the transformation of the three-phase inductance L_g from the stationary reference frame to the synchronous frame, as discussed in Chapter 3.

Equation (4.104) illustrates that the derivative of the d-axis line current i_{dg} is related to both d- and q-axis variables, as is the q-axis current i_{qg}. This indicates that the system control is cross-coupled, which may lead to difficulties in controller design and unsatisfactory dynamic performance. To solve the problem, a decoupled controller shown in Figure 4-48 can be implemented.

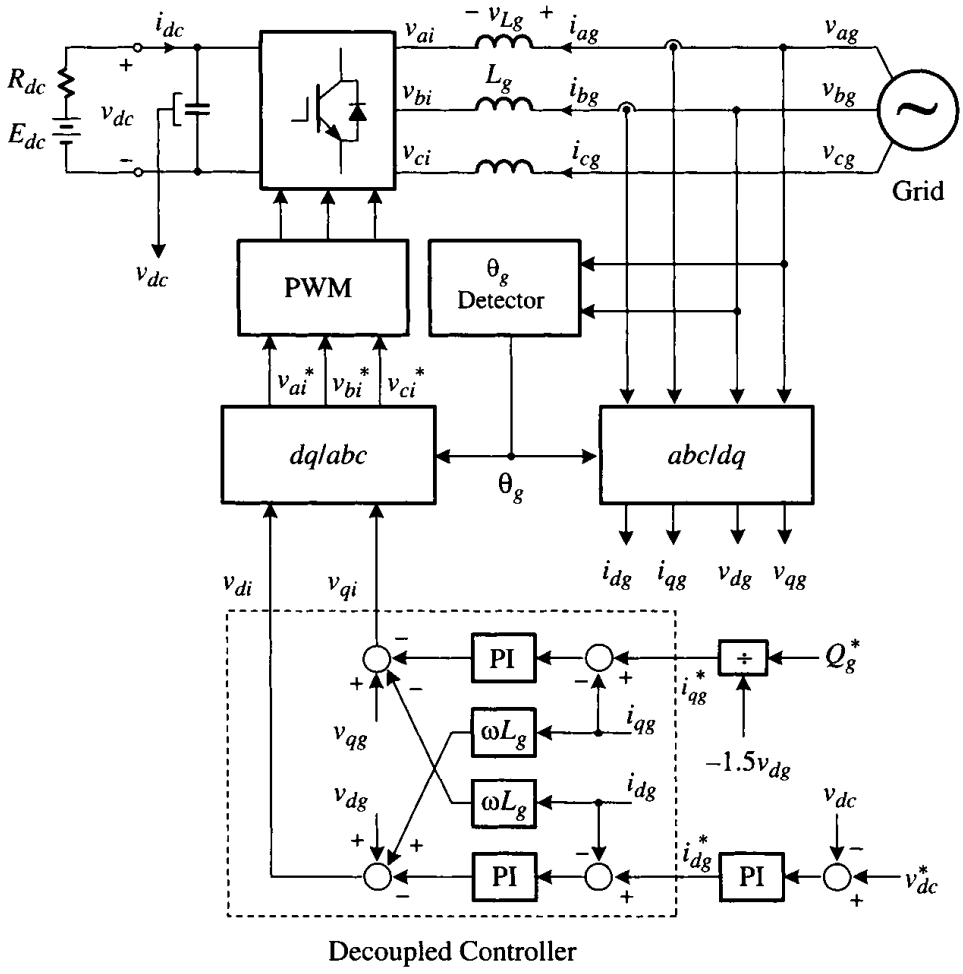


Figure 4-48. Voltage-oriented control (VOC) with a decoupled controller.

Assuming that the controllers for the dq-axis currents in Figure 4-48 are of the PI type, the output of the decoupled controller can be expressed as

$$\begin{cases} v_{di} = -(k_1 + k_2/S)(i_{dg}^* - i_{dg}) + \omega_g L_g i_{qg} + v_{dg} \\ v_{qi} = -(k_1 + k_2/S)(i_{qg}^* - i_{qg}) - \omega_g L_g i_{dg} + v_{qg} \end{cases} \tag{4.105}$$

where $(k_1 + k_2/S)$ is the transfer function of the PI controller.

Substituting (4.105) into (4.104) yields

$$\begin{cases} \dfrac{di_{dg}}{dt} = (k_1 + k_2/S)(i_{dg}^* - i_{dg})/L_g \\ \dfrac{di_{qg}}{dt} = (k_1 + k_2/S)(i_{qg}^* - i_{qg})/L_g \end{cases} \tag{4.106}$$

The above equation indicates that the control of the d-axis grid current i_{dg} is decoupled, involving only d-axis components, as is the q-axis current i_{qg}. The decoupled control makes the design of the PI controllers more convenient, and the system is more easily stabilized.

4.7.3 Operation of Grid-Connected Inverter with VOC and Reactive Power Control

The operation of the grid-tied inverter with VOC and reactive power control is analyzed through a case study below.

Case Study 4-6—Operation and Analysis of Grid-Connected Inverter. Consider a 2.3 MW/690 V grid-connected inverter. This inverter is controlled by the VOC scheme with a decoupled PI controller as shown in Figure 4-48. The DC reference is set to 1220 V, which is 3.06 pu as specified by Equation (4.102). The system parameters and operating conditions are given in Table 4.8.

Figure 4-49a illustrates the space vector diagram for the grid voltage vector $\vec{v}_g$. With the VOC scheme, $\vec{v}_g$ is aligned with the d-axis of the synchronous frame, and rotates in space at the synchronous speed of ω_g, which is also the grid angular frequency given by

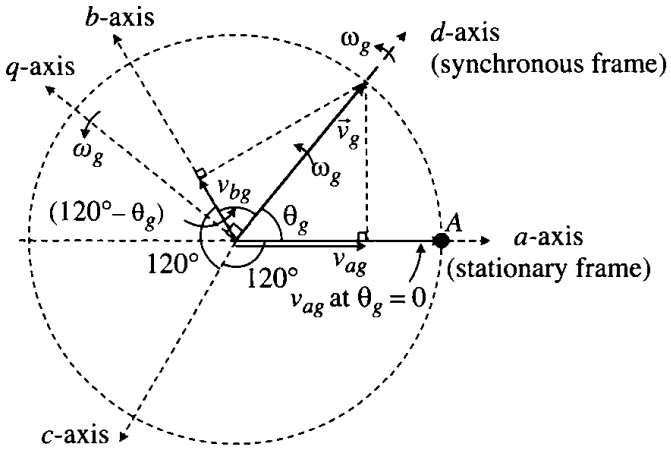
$$\omega_g = 2\pi f_g \tag{4.107}$$

where f_g is the frequency of the grid voltage.

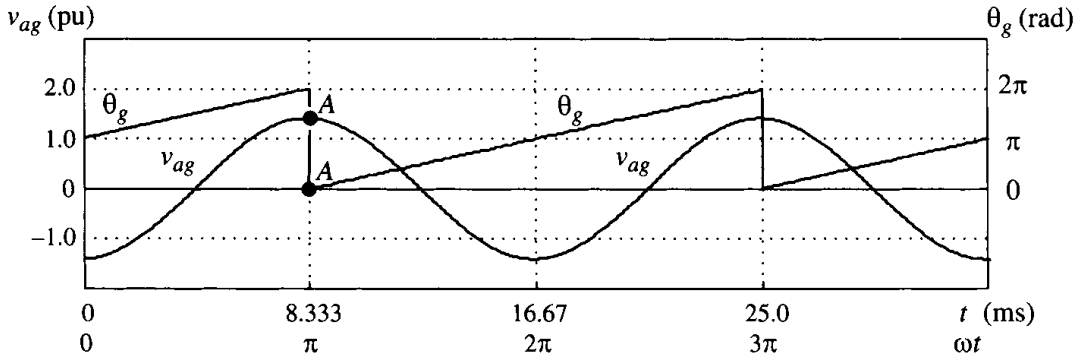
The q-axis voltage v_{qg} of the space vector $\vec{v}_g$ is zero, and d-axis voltage v_{dg} is equal to v_g, which is the magnitude (peak value) of $\vec{v}_g$. The angle θ_g of the vector is referenced to the a-axis of the stationary frame. Based on $\vec{v}_g$ and θ_g in Figure 4-49a, the three-phase grid voltage in the stationary frame is reconstructed by

Table 4-8. Parameters and operating condition the grid-connected inverter

Inverter ratings	2.3 MW, 690 V, 1924.5 A	
Control scheme	VOC with decoupled PI controller	Figure 4-48
System input references	v_{dc}^*	1220V (3.062 pu)
	Q_g^*	Adjustable
Inverter	Converter type	Two-level VSC
	Modulation scheme	Space-vector modulation
	Switching frequency	2.04 kHz
DC link circuit	Resistance R	0.0207 ohms (0.1 pu)
	Battery E	1259 V (3.16 pu)
Electric grid	Grid voltage/frequency	690 V/60 Hz
	Line inductance	0.1098 mH (0.2 pu)
Reference frame transformation	*abc*/*dq* and *dq*/*abc* transformation	Equations 3.1 and 3.2, Chapter 3



(a) Space vector diagram



(b) Waveforms

Figure 4-49. Angle of grid-voltage vector for the VOC scheme.

$$\begin{cases} v_{ag} = v_g \cos\theta_g = v_g \cos\omega_g t \\ v_{bg} = v_g \cos(\theta_g - 120°) = v_g \cos(\omega_g t - 120°) \\ v_{cg} = v_g \cos(\theta_g - 240°) = v_g \cos(\omega_g t - 240°) \end{cases} \tag{4.108}$$

Figure 4-49b shows the waveforms of the phase-*a* grid voltage v_{ag} and the space angle θ_g. When $\vec{v}_g$ rotates in space, θ_g and v_{ag} varies from zero to 2π periodically. When θ_g is equal to zero, v_{dg} reaches its peak value, shown at point *A* in Figure 4-49.

The transient waveforms of the inverter are illustrated in Figure 4-50, where the inverter initially delivers the rated active power ($P_g = -1$ pu) and zero reactive power ($Q_g = 0$) to the grid. Ignoring all the ripples (produced by current harmonics), the *d*-axis current i_{dg} is –1.41 pu (rated) and the zero *q*-axis current i_{qg} is zero. The corresponding waveforms of phase-*a* grid voltage and current during the transient are also given in the figure.

At t = 0.05 sec, the battery voltage E starts to reduce such that the active power to the grid is reduced to 0.8 pu around t = 0.075 sec, which leads the reduction of the *d*-axis current from its rated value to –1.13pu ($\sqrt{2} \times 0.8$). The *q*-axis current remains unchanged during the transients due to the decoupled control of the active and reactive power. The magnitude of the phase-*a* grid current i_{ag} is reduced, but kept out of phase with its voltage.

At t = 0.15 sec, the reference for the reactive power Q_g^* starts to vary from zero to –0.5 pu, demanding a leading power factor operation. The *q*-axis current i_{qg} reaches 0.707 pu at t = 0.20 sec, which is half of the rated value. The *d*-axis current is almost kept constant during the transients.

Figure 4-51a shows the simulated waveforms of the inverter operating in steady state I defined in Figure 4-50. The peak value of the phase-*a* grid current i_{ag} is 1.41 pu

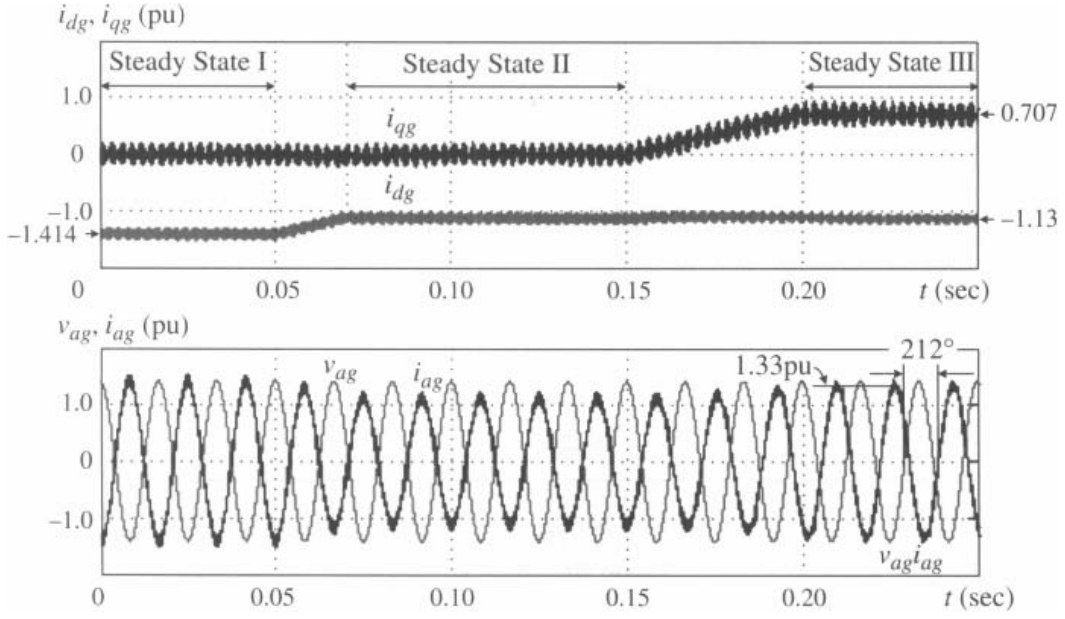


Figure 4-50. Transient waveforms of the grid-tied inverter with voltage-oriented control.

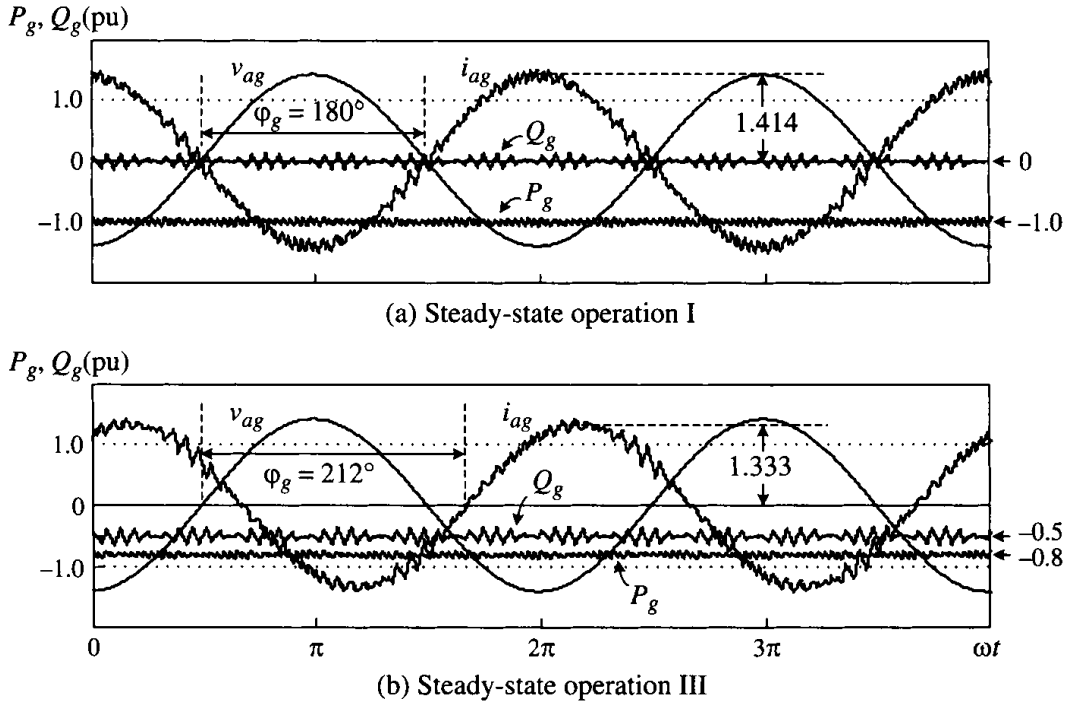


Figure 4-51. Steady-state waveforms of the grid-tied inverter with VOC scheme.

(rated). The grid current i_{ag} is out of phase with its voltage v_{ag}. The active power delivered to the grid is

$$P_g = V_{ag} I_{ag} \cos \varphi_g = \frac{i_{ag}}{\sqrt{2}} \times \frac{v_{ag}}{\sqrt{2}} \times \cos 180° = -1 \text{ pu} \tag{4.109}$$

The negative value in the above equation indicates that the inverter delivers active power to the grid.

Figure 4-51b shows the simulated waveforms when the system reaches steady state III in Figure 4-50. The measured phase-*a* current i_{ag} is 1.33 pu, which lags phase-*a* voltage v_{ag} by 212°. The active and reactive power to the grid can be calculated by

$$\begin{aligned} P_g &= V_{ag} I_{ag} \cos \varphi_g = \frac{1.333}{\sqrt{2}} \times \frac{1.414}{\sqrt{2}} \times \cos 212° = -0.8 \text{ pu} \\ Q_g &= V_{ag} I_{ag} \cos \varphi_g = \frac{1.333}{\sqrt{2}} \times \frac{1.414}{\sqrt{2}} \times \sin 212° = -0.5 \text{ pu} \end{aligned} \tag{4.110}$$

The negative reactive power indicates that the inverter operates with a leading (capacitive) power factor, which corresponds to operation in quadrant II of Figure 4-46. In practical WECS, the capacitive leading power operation is often required to support the grid voltage.

4.8 SUMMARY

A variety of power converter topologies used in wind energy conversion systems (WECS) were analyzed in this chapter, including AC voltage controllers, DC/DC boost converters, two-level voltage source converters (VSC), three-level neutral point clamped (NPC) converters, and PWM current source converters (CSC). The operating principles and switching schemes of these converters were discussed in detail. For wind energy systems with grid-tied converters, a voltage oriented control (VOC) scheme with decoupled PI controllers was elaborated. Case studies were provided for the in-depth analysis of the converter systems. The equations and tables derived in this chapter will be used for the analysis and design of wind energy conversion systems in the subsequent chapters.

REFERENCES

1. F. Blaabjerg and Z. Chen, *Power Electronics for Modern Wind Turbines,* Morgan & Claypool, 2006.
2. B. K. Bose, *Power Electronics and Motor Drives: Advances and Trends,* Academic Press, 2006.
3. B. Wu, *High-Power Converters and AC Drives,* Wiley-IEEE Press, 2006.
4. M. H. Rashid, *Power Electronics Handbook,* 2nd Edition, Academic Press, 2007.
5. N. Mohan, T. M. Undeland, and W. P. Bobbins, *Power Electronics—Converters, Applications and Design,* 2nd Edition, Wiley, 1998.
6. M. O'Loughlin, 350W Two-Phase Interleaved PFC Pre-regulator Design Review, Texas Instruments, 2005.
7. J. Dai, Y. Lang, B. Wu, D. Xu, and N. R. Zargari, A Multisampling SVM Scheme for Current Source Converter with Superior Harmonic Performance, *IEEE Transactions on Power Electronics,* Vol. 24, No. 11, 2436–2445, 2009.