Four Quasi-Z-Source Inverters

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***Abstract* - In this paper, theoretical results are shown for several novel inverters. These inverters are similar to the Z-Source inverters presented in previous works, but have several advantages, including in some combination; lower component ratings, reduced source stress, reduced component count and simplified control strategies. Like the Z-Source inverter, these inverters are particularly suited for applications which require a large range of gain, such as in motor controllers or renewable energy. Simulation and experimental results are shown for one topology to verify the analysis. Also, a back-to-back inverter system featuring bidirectionality on both inverters, as well as secondary energy storage with only a single additional switch, is shown.**

I. INTRODUCTION

Traditional voltage fed inverters, VSIs, and current fed inverters, CSIs, suffer from similar problems when used in many applications. Specifically, VSIs must have an input voltage which is greater than the peak value of the line-to-line output voltage. Similarly, practical CSIs must have an input voltage which is less than the peak value of the line-to-line output voltage. This limits the high voltage operation of VSI motor controllers and the low voltage, and hence low speed, operation of CSI motor controllers. Since the source in a practical CSI cannot maintain bidirectional power flow, these inverters are effectively unidirectional. Frequently to overcome these problems, a dc-dc converter is used as an input stage to the inverter to allow the inverter input voltage, and therefore the output voltage, to be varied as desired. Recently, the voltage and current fed Z-source inverters, ZSIs, have been proposed to overcome these problems. These inverters replace the dc-dc input stage with a special LC Z-network, which allows the input voltage to be varied as desired. The voltage fed ZSI has some significant drawbacks; namely that the input current is discontinuous in the boost mode and that the capacitors

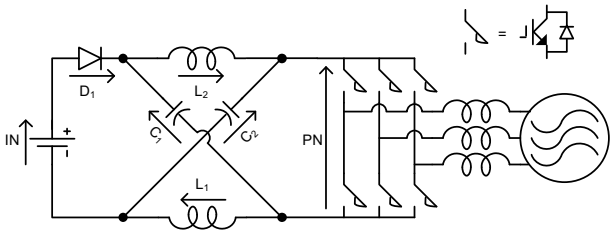

Figure 1a: Voltage Fed ZSI with Discontinuous Input Current

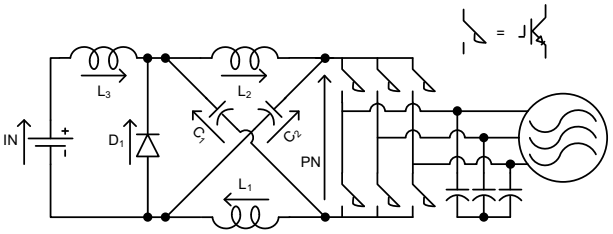

Figure 2a: Current Fed ZSI with Continuous Input Current

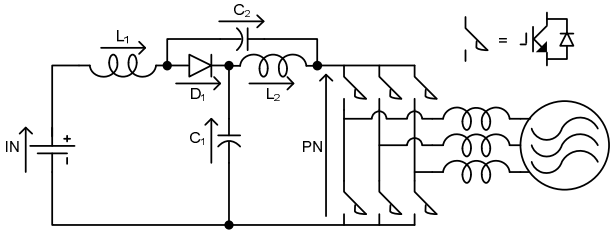

Figure 1b: Voltage Fed qZSI with Continuous Input Current

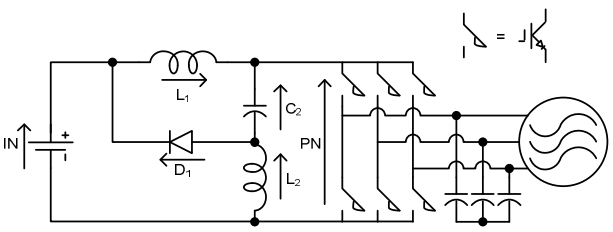

Figure 2b: Current Fed qZSI with Discontinuous Input Current

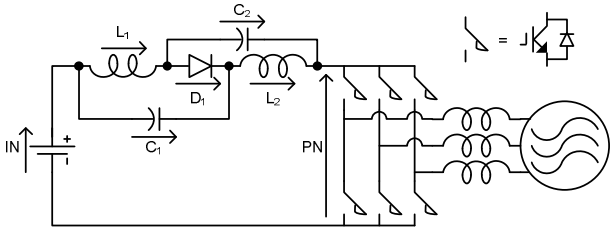

Figure 1c: Voltage Fed qZSI with Discontinuous Input Current

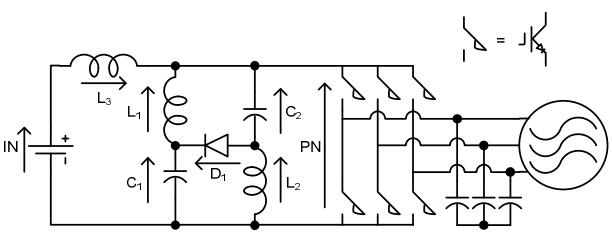

Figure 2c: Current Fed qZSI with Continuous Input Current

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must sustain a high voltage. The main drawback of the current fed ZSI is that the inductors must sustain high currents. Also, control complexity is an issue when the ZSI is used in a back-to-back configuration due to the coupling of the inverter switching functions.

To improve on the traditional ZSIs, four new quasi-Z-source inverters, qZSIs, have been developed which feature several improvements and no disadvantages when compared to the traditional ZSIs. The voltage fed ZSI as well as the two novel voltage fed inverters, with similar properties to the ZSI, are shown in Figs. 1a, 1b, and 1c, while the current fed ZSI, as well as two novel current fed inverters are shown in Figs. 2a, 2b, and 2c. The novel qZSI topologies shown in Figs. 1b and 1c, in a manner consistent with the voltage fed ZSI, can be made bidirectional by replacing the diode, D_1, with a bidirectionally conducting, unidirectionally blocking switch. The qZSI, shown in Fig. 1b, when compared to the ZSI shown in Fig. 1a, features lower dc voltage on capacitor C_2 as well as continuous input current, while the qZSI topology, shown in Fig. 1c, features lower dc voltage on capacitors C_1 and C_2, however, the input current is discontinuous. Also, due to the input inductor, L_1, the qZSI shown in Fig. 1b does not require input capacitance, unlike the ZSI and the qZSI shown in figure 1c. The current fed qZSI topologies shown in Figs. 2b and 2c, in a manner consistent with the current fed ZSI, are bidirectional with the diode, D_1. The qZSI shown in Fig. 2b, when compared to the ZSI shown in Fig. 2a, features reduced current in inductor L_2, as well as reduced passive component count, while the qZSI shown in Fig. 2c features lower current in inductors L_1 and L_2. Again, due to the input inductor, L_3, the ZSI and qZSI in Fig. 1c do not require input capacitance. All four qZSI topologies also feature a common dc rail between the source and inverter, unlike the traditional ZSI circuits. Furthermore, these qZSI circuits have no disadvantages when compared to the traditional ZSI topologies. These qZSI topologies therefore can be used in any application in which the ZSI would traditionally be used.

II. Theoretical Analysis

Both the voltage and current fed qZSIs can be controlled using any methods which can be used to control the traditional ZSIs. These methods have been explored in detail in [1-5] and others, so the methods will not be explained here.

Regardless of the control strategy used, for the voltage fed ZSI and qZSIs, the operation can be broken down into five modes; the active mode, the shoot through mode, and the three discontinuous modes. In the active mode, one and only one device in each phase leg conducts. During the active mode, the inverter is controlled in the same manner as a standard VSI. The shoot through mode

TABLE 1: Voltage Fed ZSI and qZSI Governing Equations

	Voltage Fed ZSI	Voltage Fed qZSI w/ Continuous Input Current	Voltage Fed qZSI w/ Discontinuous Input Current
$\frac{V_{C1}}{V_{IN}}$	$\frac{1-D}{1-2D}$	$\frac{1-D}{1-2D}$	$\frac{D}{1-2D}$
$\frac{V_{C2}}{V_{IN}}$	$\frac{1-D}{1-2D}$	$\frac{D}{1-2D}$	$\frac{D}{1-2D}$
$I_{L1} = I_{L2}$	$\frac{P}{V_{IN}}$	$\frac{P}{V_{IN}}$	$\frac{P}{V_{IN}}$
I_{C1}	$-I_{PN} - I_{L1}$	$-I_{PN} - I_{L1}$	$-I_{PN} - I_{L1}$
I_{C2}	$-I_{PN} - I_{L2}$	$-I_{PN} - I_{L2}$	$-I_{PN} - I_{L2}$
$\frac{V_{L1}}{V_{IN}} = \frac{V_{L2}}{V_{IN}}$	$\frac{D}{1-2D} - S_D * \frac{1}{1-2D}$	$\frac{D}{1-2D} - S_D * \frac{1}{1-2D}$	$\frac{D}{1-2D} - S_D * \frac{1}{1-2D}$
$\frac{V_{PN}}{V_{IN}}$	$\overline{S_D} * \frac{1}{1-2D} \geq 0$	$\overline{S_D} * \frac{1}{1-2D} \geq 0$	$\overline{S_D} * \frac{1}{1-2D} \geq 0$
$\frac{V_D}{V_{IN}}$	$S_D * \frac{1}{1-2D} \geq 0$	$S_D * \frac{1}{1-2D} \geq 0$	$S_D * \frac{1}{1-2D} \geq 0$
I_D	$I_{L1} + I_{L2} + I_{PN}$	$I_{L1} + I_{L2} + I_{PN}$	$I_{L1} + I_{L2} + I_{PN}$
I_{IN}	I_D	I_{L1}	$-I_{PN}$

TABLE 2 CURRENT FED ZSI AND qZSI GOVERNING EQUATIONS

	Current Fed ZSI	Current Fed qZSI w/ Discontinuous Input Current	Current Fed qZSI w/ Continuous Input Current
$\frac{I_{L1}}{P/V_{IN}}$	$\frac{1-D}{1-2D}$	$\frac{1-D}{1-2D}$	$\frac{D}{1-2D}$
$\frac{I_{L2}}{P/V_{IN}}$	$\frac{1-D}{1-2D}$	$\frac{D}{1-2D}$	$\frac{D}{1-2D}$
$\frac{I_{L3}}{P/V_{IN}}$	1	Not Applicable	1
V_{C1}	V_{IN}	Not Applicable	V_{IN}
V_{C2}	V_{IN}	V_{IN}	V_{IN}
V_{L1}	$V_{PN}-V_{C2}$	$V_{PN}-V_{IN}$	$V_{PN}-V_{C1}$
V_{L2}	$V_{PN}-V_{C1}$	$V_{PN}-V_{C2}$	$V_{PN}-V_{C2}$
V_{L3}	$V_{C1}+V_{C2}-V_{PN}-V_{IN}$	Not Applicable	$V_{PN}-V_{IN}$
$\frac{I_{C1}}{P/V_{IN}}$	$\frac{D}{1-2D}-S_D*\frac{1}{1-2D}$	Not Applicable	$\frac{D}{1-2D}-S_D*\frac{1}{1-2D}$
$\frac{I_{C2}}{P/V_{IN}}$	$\frac{D}{1-2D}-S_D*\frac{1}{1-2D}$	$\frac{D}{1-2D}-S_D*\frac{1}{1-2D}$	$\frac{D}{1-2D}-S_D*\frac{1}{1-2D}$
$\frac{I_{PN}}{P/V_{IN}}$	$\overline{S_D}*\frac{1}{1-2D}\geq 0$	$\overline{S_D}*\frac{1}{1-2D}\geq 0$	$\overline{S_D}*\frac{1}{1-2D}\geq 0$
$\frac{I_D}{P/V_{IN}}$	$S_D*\frac{1}{1-2D}\geq 0$	$S_D*\frac{1}{1-2D}\geq 0$	$S_D*\frac{1}{1-2D}\geq 0$
V_D	$V_{C1}+V_{C2}-V_{PN}\geq 0$	$V_{IN}+V_{C2}-V_{PN}\geq 0$	$V_{C1}+V_{C2}-V_{PN}\geq 0$
I_{IN}	I_{L3}	$I_{L1}-I_D$	I_{L3}

occurs when both switches in at least one phase conduct. The voltage across the inverter, V_{pn}, during this mode is zero. The discontinuous modes, which have been explored in detail in [6], can occur when the inductors, L_1 and L_2, have a small value relative to other system parameters. In general, the discontinuous modes occurs when the inverter is gated as if in the active mode, but one phase current is greater than or equal to the sum of the inductor currents. In this situation, no current flows through the diode, D_1. The discontinuous modes are not controllable; however, these modes are not entirely unpredictable. For purposes of analysis in this work, it will be assumed that the inductors are large enough to avoid the discontinuous operating modes.

For the current fed ZSI and qZSIs, the operation can be divided into modes in a similar manner. In the active mode one and only one upper device, and one and only one lower device conduct. During the active mode, the inverter is controlled in the same manner as a standard CSI. During the shoot through mode, all of the upper and/or all of the lower switches are gated off. In general, during the discontinuous mode, the switches are gated as if in an active state, but one line-to-line voltage is greater than or equal to the sum of the capacitor voltages. When this occurs, the diode, D_1, conducts and the inverter behaves as if it is an open circuit. Again for the analysis of the current fed ZSI and qZSIs, these modes will be ignored.

Using the modes described above, Kirchhoff's voltage and current laws, and state-space averaging on the inductors and capacitors for each circuit, the governing equations can be developed, along with the equations for gain as a function of the shoot through duty cycle, D. Table 1 shows the governing equations for the three different voltage fed inverters, while Table 2 shows the equations for the current fed inverters, where all voltages and currents are positive in the sense of the arrows shown in Figs. 1 and 2. In these equations, S_D is the shoot through switching function. S_D is defined to be 1 when the inverter is in the shoot through mode and 0 when the

inverter is in the active mode. From Table 1, it can be seen that the only parameters which change for the different voltage fed topologies are the capacitor voltages, and the input current. The maximum shoot through duty cycle, D, is 0.5 for these topologies with a positive input voltage, V_{IN}. Therefore, by the gain equations for the capacitor voltages, it can be seen that with the qZSI circuits, the capacitor voltages are reduced when compared with the traditional ZSI. If the input voltage is negative, it is also possible to operate the voltage fed topologies with a shoot through duty cycle, D, greater than 0.5. In this case, the ZSI has lower capacitor voltage than the qZSIs. Similarly, from Table 2, it can be seen that when the shoot through duty cycle, D, is less than 0.5, the current through the inductors is decreased for the current fed qZSI topologies when compared to the traditional current fed ZSI. When the shoot through duty cycle, D, is greater than 0.5 for the current fed ZSI or the qZSIs, the power flow is negative, and the current through the inductors is lower for the ZSI than the qZSIs. If the diode D_1 is replaced with a bidirectionally blocking, unidirectionally conducting switch in any of the current fed topologies, it is possible to feed the system with a positive or negative voltage, and several new operating regions are allowed.

III. Simulation and Experimental Results

To verify the operation of these new topologies, simulations were performed for three operating points. The qZSI with continuous input current shown in Fig. 3 was simulated with the systems parameters as follows:

$$L_1 = L_2 = 100 \text{ uH}, C_1 = C_2 = 200 \text{ uF},$$
$$L_f = 1\text{mH}, C_f = 120 \text{ uF } \Delta, R_L = 20\ \Omega\ \Delta$$

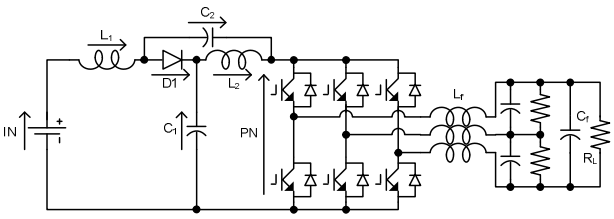

Figure 3: Voltage Fed qZSI with Continuous Input Current

On the upper half of all simulation plots, the output voltages are shown with a timescale of two milliseconds per division. On the lower half of the simulation plots, the LC network voltages and current are shown with a timescale of ten microseconds per division.

Experimental results were obtained for the voltage fed qZSI with continuous input current using an appropriately modified z-source inverter, with an LC filter and resistive load. The topology of this circuit is the same as that shown in Fig. 4, with the same parameters. This inverter system is operated with no dead-time. The switching

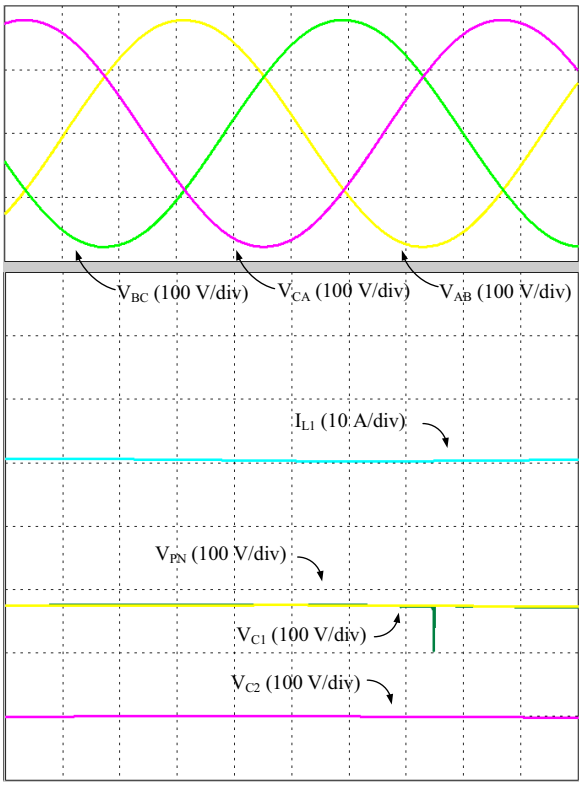

Figure 4: Simulation Results with D = 0.0

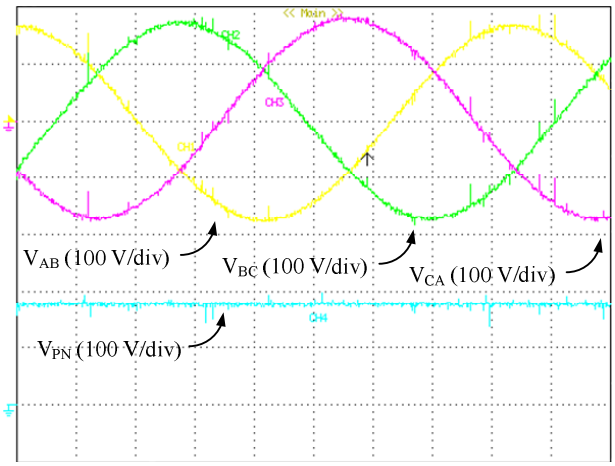

Figure 5: Output waveforms with D = 0.0

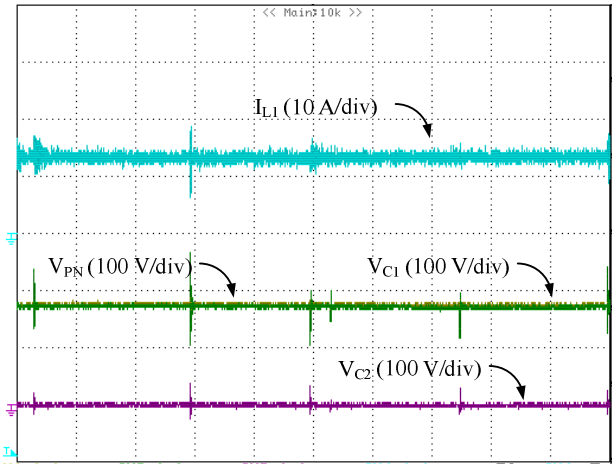

Figure 6: Inductor Current and Capacitor Voltages with D = 0.0

frequency seen from the output is 10 kHz, while the frequency seen by the LC network is 20 kHz. Also, there are no snubbers on either the individual IGBTs or the positive and negative terminals of the 6-pack IGBT module.

For all experiments, the three phase output voltages, V_{AB}, V_{BC}, V_{CA}, and the IGBT module voltage, V_{PN}, were measured with isolated probes. The timescale on the plots which show these waveforms have a timescale of two milliseconds per division. Simultaneously, the two capacitor voltages, V_{C1}, V_{C2}, and the IGBT module voltage, V_{PN}, were measured using differential probes, and the input inductor current, I_{L1}, was measured using a current probe. The timescale on these plots is ten microseconds per division.

A. *Case 1: D = 0.0*

The first experiment was performed with an input voltage of 175 volts and no shoot through, D = 0.0. The inverter was controlled as a traditional VSI with third harmonic injection. The output voltage was controlled to be 120 Vrms line-to-line. Fig. 4 shows the simulation results for this case. These results are consistent with the results predicted by the theoretical analysis for the qZSI with continuous input current shown in Table 1. Fig. 5 shows the output voltage waveforms, and the voltage on the IGBT module, while Fig. 6 shows the LC network measurements for the experimental setup. As can be seen in Fig. 6, the input current is continuous, and constant, unlike either the traditional ZSI or the VSI. The results of the theoretical analysis, simulation, and experiments for the case of no shoot through are shown in numerical format in Table 3. As can be seen in Table 3, the theoretical, simulation and experimental results are all in agreement for this case.

TABLE 3: CASE 1 RESULTS

D = 0.0	V_{IN}	V_{C1}	V_{C2}	$I_{L1} = I_{L2}$
Theoretical	175 V	175 V	0 V	12.34 A
Simulation	175 V	175 V	0 V	10.5 A
Experimental	175 V	175 V	0 V	13.3 A

B. *Case 2: D = .1*

The second experiment was performed with an input voltage of 152 volts and a shoot through duty cycle, D, of 0.1. Third harmonic injection and constant boost ratio were used. The output voltage was again controlled at 120 Vrms. Fig. 7 shows the simulation results for this case. Fig. 8 shows the output voltage waveforms, and the voltage on the IGBT module, while Fig. 9 shows the LC network measurements for the experimental case. Again, due to the inductor on the input connection, the input current is continuous; however, unlike the case with no boost, the input current is not constant. Also, while the average voltage is approximately the same at the

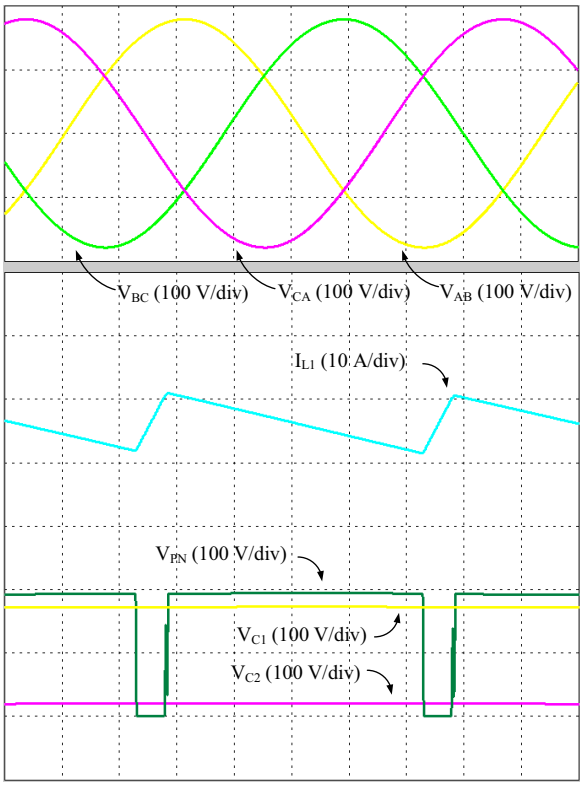

Figure 7: Simulation Results for D = 0.1

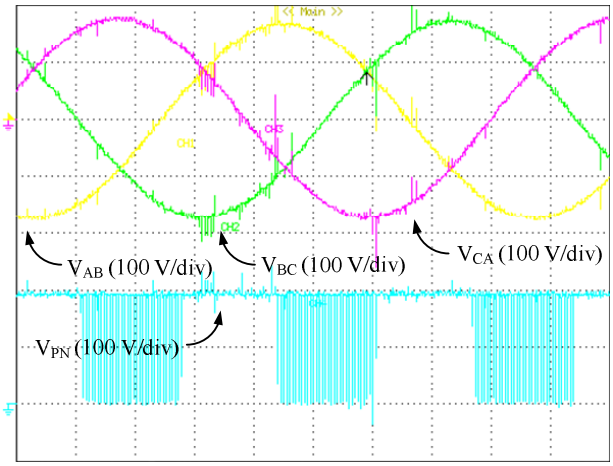

Figure 8: Output waveforms with D = 0.1

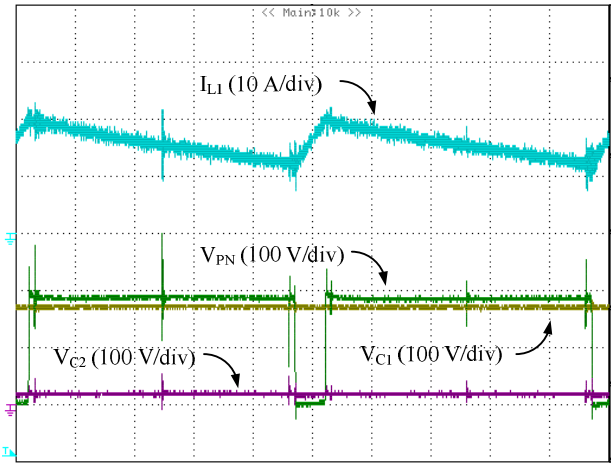

Figure 9: Inductor Current and Capacitor Voltages with D = 0.1

terminals of the IGBT module as the case with no boost, the maximum value, and therefore the stress, is increased. It is also worth noting that with this input voltage it would not be possible to produce the output voltage with a traditional VSI. Table 4 shows the results of the theoretical analysis, simulation, and experiments for the case of D = 0.1 in numerical format. These results are all consistent and again confirm the theoretical analysis above.

TABLE 4 : CASE 2 RESULTS

D = 0.1	V_{IN}	V_{C1}	V_{C2}	$I_{L1} = I_{L2}$
Theoretical	152 V	171 V	19 V	14.21 A
Simulation	152 V	173 V	21 V	16.3 A
Experimental	152 V	172 V	20 V	16.1 A

C. *Case 3: D = 0.2*

The third experiment was performed with an input voltage of 129 volts and a shoot through duty cycle, D, of 0.2. Again, third harmonic injection and constant boost ratio were used. The output voltage was controlled at 120 Vrms. Fig. 10 shows the simulation results, Fig. 11 shows the output voltage waveforms, and the voltage on the IGBT module, while Fig. 12 shows the LC network measurements for the experiment. Again in this case, the input current is continuous and non-constant. Also as in all cases, the average value of the voltage on the IGBT module, V_{PN}, is equal to the voltage on capacitor C_1, V_{C1}.

TABLE 5 : CASE 3 RESULTS

D = 0.2	V_{IN}	V_{C1}	V_{C2}	$I_{L1} = I_{L2}$
Theoretical	129 V	172 V	43 V	16.74 A
Simulation	129 V	173 V	44 V	21.6 A
Experimental	129 V	170 V	42 V	20.0 A

The simulation and experimental results above confirm the theoretical analysis shown in Table 1 for the qZSI with continuous input current. These results also show that the inverter has similar behavior to the ZSI presented in [1-6]. These results also show that, as predicted by the theoretical analysis, the voltage on capacitor C_2, V_{C2}, is reduced when compared to the traditional ZSI. Also, as can be seen in Figs. 6, 9, and 12, the input inductor current, IL1, is continuous, which significantly reduces the input stress when compared to both the traditional ZSI and VSI.

IV. CONCLUSION AND FUTURE WORK

The four novel inverter topologies presented in this work offer several advantages when compared to the traditional ZSI. These advantages include reduced passive component ratings, reduced component count, and improved input profiles. Theoretical analysis for these four inverters was presented, and for the voltage fed qZSI with continuous input current, simulation and

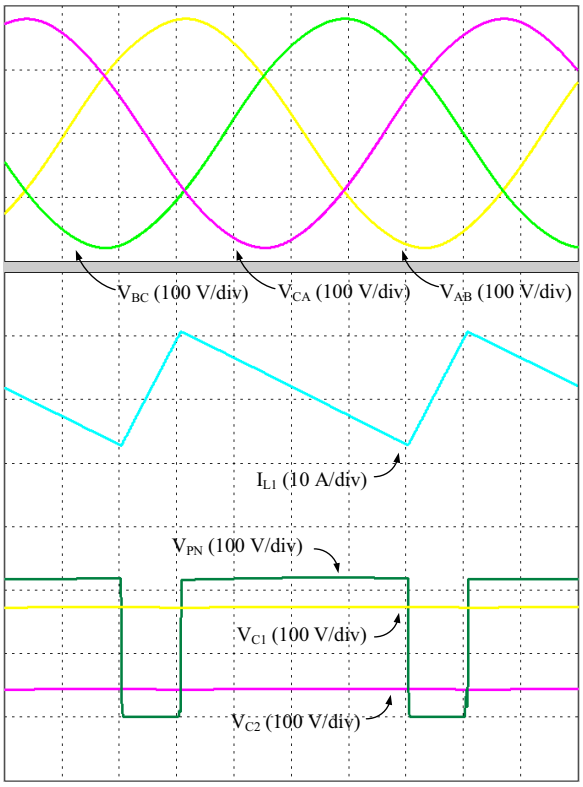

Figure 10: Simulation Results for D = 0.2

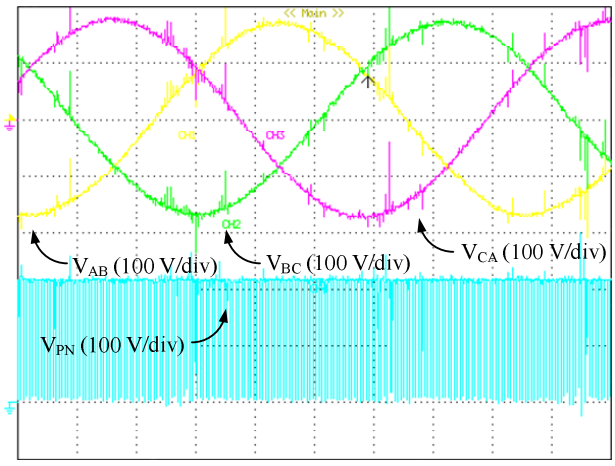

Figure 11: Output waveforms with D = 0.2

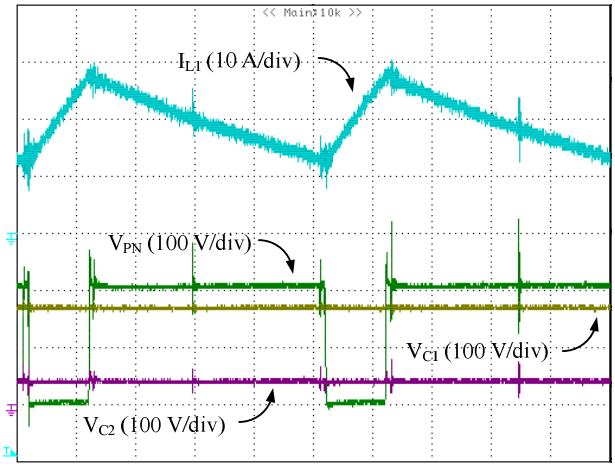

Figure 12: Inductor Current and Capacitor Voltages with D = 0.2

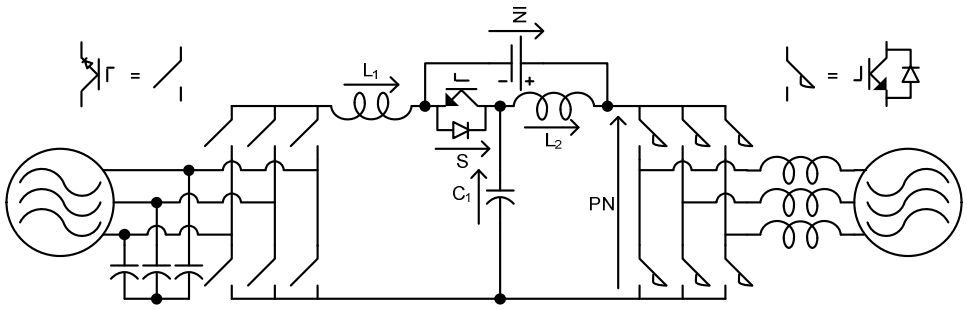

Figure 13: Back-to-Back qZSI

experimental results were presented which confirm the theoretical analysis. All four of the qZSI topologies, like the ZSIs, are well suited for systems which require a large range of gain, or a large gain, such as motor controllers and renewable energy applications.

Currently in the planning stages is the back-to-back qZSI system shown in Fig. 13. This system is based on the qZSI topology shown in Fig. 1b, and features bidirectionality on both inverters and incorporates low voltage secondary energy storage with only a single additional switch. The system is particularly suited for use in series hybrid electric vehicles, where a low voltage battery is desired.

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