This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2019.2902785, IEEE Transactions on Industrial Electronics

A High Efficiency Non-Isolated Buck-Boost Converter Based on ZETA Converter

Mohamad Reza Banaei, Hossein Ajdar Faeghi Bonab

***Abstract*—In this paper, a new transformerless buck-boost converter based on ZETA converter is introduced. The proposed converter has the ZETA converter advantages such as, buck-boost capability, input to output DC insulation and continuous output current. The suggested converter voltage gain is higher than the classic ZETA converter. In the presented converter, only one main switch is utilized. The proposed converter offers low voltage stress of the switch; therefore, the low on-state resistance of the main switch can be selected to decrease losses of the switch. The presented converter topology is simple; hence, the control of the converter is simple. The converter has the continuous output current. The mathematical analyses of the presented converter are given. The experimental results confirm the correctness of the analysis.**

***Index Terms*— Transformerless buck-boost converter, voltage gain, main switch, voltage stress.**

I. INTRODUCTION

FUEL cell and photovoltaic cell are the two most vital energies. However, the voltage levels of these sources are too low and unpredictable unstable, varying with climate conditions such as solar irradiance and temperature. Therefore, high voltage gain converters are required for photovoltaic cell and fuel cell systems [1-2]. In theory, the classic boost converter can be used for high voltage applications. However, the efficiency and the voltage gain of the classic boost converter are limited with large duty cycle and the losses of the diode and switch, and the equivalent series resistance of inductors and capacitors. The classic boost converter has high stress on the main switch. This high stress of the main switch makes high conduction losses [3]. Dc-dc converters are utilized for transferring power in many applications. It is necessary to obtain a regulated output voltage. In addition, the high voltage conversion can be significant [4-5]. Aiming to provide higher voltage conversion ratios, many modifications for the DC-DC converters are presented. In switched-capacitor converters, the input voltage is used to provide energy and the switched-capacitors are linked in series and supply energy to the load. Thus, the source voltage can be multiplied [6]. Using switched-capacitors converters is the one method for voltage gain improvement. However, many switched-capacitor cells are needed to achieve high voltage, which makes the circuit complex. The major problem of the switched-capacitor cells is voltage stress of the switches. Also high voltage rated devices make high conduction losses. Converters with couple inductor can provide high step-up voltage gain with low duty cycle and with a simple topology. However, the main problem of these converters is the high voltage stress of the switch due to leakage inductance [7-11]. In [12] a transformerless buck-boost converter with high voltage gain is proposed. The stress of the switch and diode in the converter is high. Hence, the losses of the converter will be high. In [13] high step-up transformerless converters are proposed. In these converters, one main switch is used. In these converters, the switched-capacitor technique is used. In [14] a multi phase transformerless dc-dc converter with high voltage gain is proposed. The voltage stress of the converter is low. Hence, the losses can be reduced. In [15] a transformerless converter based on diode-capacitor cell is proposed. The converter has some advantages such as high voltage gain, low diodes and switches stresses, low ripple and high efficiency. In [16] the interleaved converters with transformer are presented. In these converters, active and passive clamps are used to reduce the switch voltage stress. In [17] a zero voltage switching (ZVS) ZETA dc-dc converter with active clamp is presented. In the presented converter, the ZETA and flyback converters utilize the same active switches to reduce the switch. In [18] a transformerless buck-boost converter is proposed. The voltage gain of the converter is triple as large as the classic buck-boost converter. In [19] a transformerless KY buck-boost converter is proposed. In [20] two ZETA dc-dc converters are used for reducing the output voltage ripple. In [21] a high step-up converter with the coupled inductor is proposed. This converter has one main switch and the stress across the main switch is reduced. However, the voltage stresses of the three diodes of the converter are high. In this converter, the leakage inductance energy can be recycled. In [22] a high step-up interleaved converter is presented. In this converter, the interleaved boost converter and the voltage-double module are used and the converter has two main switches and the stresses of the diodes of the converter are high. In [23] a high step-up DC-DC converter is proposed. This converter employs two main switches and the diodes and switches stresses are high. In [24] a transformerless buck-boost converter is proposed. This converter has three main switches. In this converter, the

Manuscript received October 18, 2018; revised December 9, 2018; accepted February 12, 2019.

Mohamad Reza Banaei and Hossein Ajdar Faeghi Bonab are with the Department of Electrical Engineering, Azarbaijan Shahid Madani University, Tabriz, Iran (e-mail: m.banaei@azaruniv.ac.ir).

0278-0046 (c) 2018 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2019.2902785, IEEE Transactions on Industrial Electronics

voltage stress of the switch is equal to the output voltage. The converter conduction and switching losses are high. In [25-27] high step-up transformerless dc-dc converters are proposed. In this paper, a novel transformerless buck boost converter based on ZETA converter is proposed. The converter voltage gain is higher than the classic buck-boost converter, ZETA, CUK and SEPIC converters. The proposed converter topology is very simple; hence, the converter control is simple. This converter has one main switch. The main switch and diodes stresses are less than the output voltage, hence the switch loss will be low and the converter efficiency can be improved. The buck-boost converters are used in some applications like LED drivers, fuel-cell, car electronic devices. The modes analysis is explained and to confirm the operation of the converter, experimental results are given.

II. OPERATING PRINCIPLE OF THE PROPOSED CONVERTER

Fig. 1. shows the circuit topology of the presented converter. The converter consists one main switch S, two diodes D_1 and D_2, three inductors L_1, L_2 and L_3, four capacitors C_1, C_2, C_3 and C_o and load R.

To simplify the analysis of the new buck-boost converter, the following conditions were considered:

1) All capacitors are large enough hence; the voltages of the capacitors can be seen as constant.

2) Semiconductor elements such as diodes and switch are ideal.

The proposed converter can be used in the continuous conduction mode (CCM) and the discontinuous conduction mode (DCM). The continuous conduction mode has two operating modes. The analysis of the converter at (CCM) is presented in detail as follows:

1) State 1 $[t_0,t_1]$*:* During this time interval, the switch S is turned ON and the diodes D_1 and D_2 are turned OFF. The current-flow path is shown in Fig. 2(a). The inductors L_1, L_2 and L_3 are magnetized. The capacitor C_1 is discharged and the capacitors C_2 and C_3 are charged. Thus, the corresponding equations can be achieved as follows:

$$V_{L1}=V_i \tag{1}$$

$$V_{L2}=V_i+V_{C1}-V_{C2}-V_{C3} \tag{2}$$

$$V_{L3}=V_{C1}+V_i-V_o \tag{3}$$

2) State 2 $[t_1,t_2]$: The current-flow path is shown in Fig. 2(b). During this time interval, switch S is turned OFF. Diodes D_1 and D_2 are turned ON. The L_1, L_2 and L_3 are demagnetized. The capacitor C_1 is charged by the inductor L_1. The capacitors C_2 and C_3 are discharged. The voltages of inductors are obtained as follows:

$$V_{L1}=V_{C2}-V_{C1} \tag{4}$$

$$V_{L2}=-V_{C2}=-V_{C3} \tag{5}$$

$$V_{L3}=V_{C3}-V_o \tag{6}$$

III. STEADY STATE ANALYSIS OF THE PROPOSED CONVERTER

A. Voltage gain

By applying volt-sec balance principle on L_1 and L_2 and using (1), (2), (4) and (5), we have:

$$\frac{1}{T_s}\left(\int_0^{DT_s} V_i\,dt+\int_{DT_s}^{T_s}(V_{C2}-V_{C1})dt\right)=0 \tag{7}$$

$$\frac{1}{T_s}\left(\int_0^{DT_s}(V_i+V_{C1}-V_{C2}-V_{C3})dt+\int_{DT_s}^{T_s}(-V_{C2})dt\right)=0 \tag{8}$$

By using (5), (7) and (8), the voltage of the capacitors C_1, C_2 and C_3 (V_{C1}, V_{C2} and V_{C3}) can be achieved as follows:

$$V_{C1}=\frac{2DV_i}{1-D} \tag{9}$$

$$V_{C2}=V_{C3}=\frac{DV_i}{1-D} \tag{10}$$

By applying a volt-sec balance L_3 and using (9) and (10), the voltage transfer gain (M_{CCM}) can be found as follows:

$$\frac{1}{T_s}\left(\int_0^{DT_s}(V_{C1}+V_i-V_o)dt+\int_{DT_s}^{T_s}(V_{C3}-V_o)dt\right)=0 \tag{11}$$

$$M_{CCM}=\frac{V_o}{V_i}=\frac{2D}{1-D} \tag{12}$$

According to (12), it is apparent that the voltage gain of the proposed converter is twice as large as the ZETA converter. Therefore, the voltage gain of the converter is higher than that of ZETA converter. Fig. 3. shows some key waveforms of the proposed converter in (CCM).

The voltage gain curves for the proposed converter, ZETA and classic buck boost converter are shown in Fig. 4. It is seen that the voltage transfer gain of the converter is higher than that of the other converters.

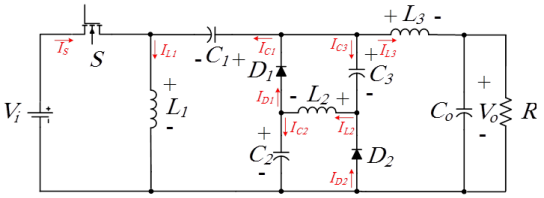
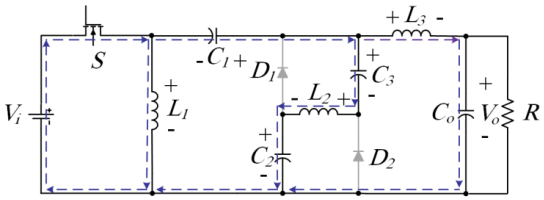


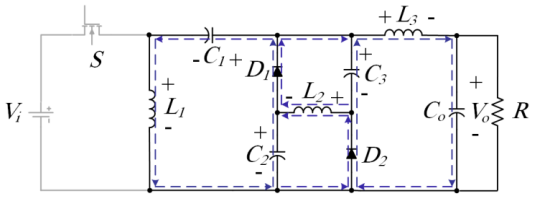
Fig. 1. Equivalent circuit of the proposed converter



(a)

0278-0046 (c) 2018 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2019.2902785, IEEE Transactions on Industrial Electronics



(b)

Fig. 2. Operation modes of the proposed converter (a) First mode, (b) Second mode.

B. Calculation of the currents

The average current of the inductor L_3 (I_{L3}) and the inductor L_2 (I_{L2}) and the capacitors C_2 and C_3 $(I_{C2,on}$ and $I_{C3,on})$ during state 1 can be obtained as follows:

$$I_{L3} = \frac{V_i(2D)}{R(1-D)} \tag{13}$$

$$I_{C1,on} = -\left(I_{L2} + \frac{V_i(2D)}{R(1-D)}\right) \tag{14}$$

$$I_{C2,on} = I_{C3,on} = I_{L2} \tag{15}$$

The average current of the capacitor C_1 during state 2 $(I_{C1,off})$ can be earned as follows:

$$I_{C1,off} = \left(I_{L2} - I_{C2,off} - I_{C3,off} - I_{L3}\right) \tag{16}$$

Where, $I_{C2,off}$ and $I_{C3,off}$ are the average current of the capacitors C_2 and C_3 during state 2.

By applying amper-second balance principle on the capacitors C_1, C_2 and C_3 to yield:

$$\frac{1}{T_s}\left(\int_0^{DT_s} I_{C1,2,3,on}dt + \int_{DT_s}^{T_s} I_{C1,2,3,off}\,dt\right) = 0 \tag{17}$$

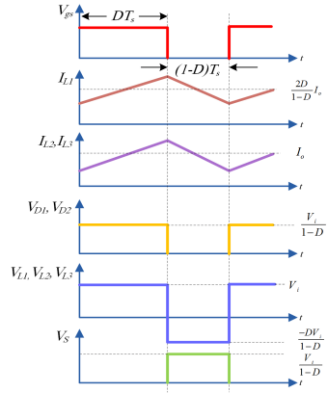


Fig. 3. Some waveforms of the proposed converter

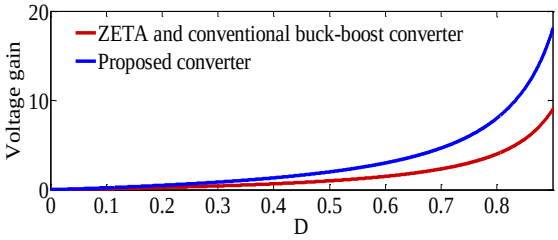


Fig. 4. Curves of voltage gain comparison of proposed converter and other converters at CCM operation

By substituting (13)-(16) into (17), the average current of the inductor L_2 (I_{L2}) and the capacitors C_2 and C_3 $(I_{C2,on}$ and $I_{C3,on})$ can be obtained as follows:

$$I_{L2} = I_{C2,on} = I_{C3,on} = \frac{V_i(2D)}{R(1-D)} \tag{18}$$

According to above equations, the average currents of capacitor C_1 $(I_{C1,on})$ can be calculated as follows:

$$I_{C1,on} = \frac{V_i(-4D)}{R(1-D)} \tag{19}$$

According to Fig. 2(b) and (19), the average current of inductor L_1 (I_{L1}) can be earned as follows:

$$I_{L1} = I_{C1,off} = \frac{V_i\left(4D^2\right)}{R(1-D)^2} \tag{20}$$

According to Figs. 2(a) and 2(b), the currents stresses of the switch S (I_S) and the diodes D_1 and D_2 $(I_{D1}$ and $I_{D2})$ can be obtained as follows:

$$I_S = I_{L1} - I_{C1,on} = \frac{V_i(4D)}{R(1-D)^2} \tag{21}$$

$$I_{D1} = I_{L2} - I_{C2,off} = \frac{V_i(2D)}{R(1-D)^2} \tag{22}$$

$$I_{D2} = I_{L2} - I_{C3,off} = \frac{V_i(2D)}{R(1-D)^2} \tag{23}$$

The switch current stress curves for the proposed converter and converter in [18] are shown in Fig. 5. It is seen that the current stress of the converter is lower than converter in [18] and the conduction loss of the presented converter will be low.

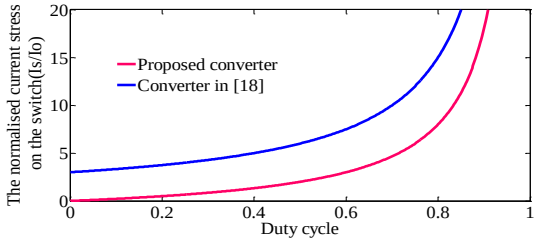


Fig. 5. Switch current stress of the converters versus duty cycle

C. Discontinuous conduction mode

There are three modes in Discontinuous conduction mode (DCM). The state 1 in (DCM) is the same as the state 1 in (CCM). In the state 2, the currents of the diodes will decrease. In the state 3, the current of the diodes decreases to zero. In this state, the diodes are turned off. The equivalent circuit is shown in Fig. 6. In this state, the inductors L_1, L_2 and L_3 voltage will be zero.

According to Fig 2(b), the sum of the average currents of the diodes D_1 and D_2 can be earned as follows:

$$I_{D1} + I_{D2} = I_{L1} + I_{L2} + I_{L3} \tag{24}$$

The average of diodes D_1 and D_2 currents $(I_{D1,av}$ and $I_{D2,av})$ can be achieved as follows:

0278-0046 (c) 2018 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2019.2902785, IEEE Transactions on Industrial Electronics

$$I_{D1,av} = I_{D2,av} = \frac{V_o}{R} \tag{25}$$

According to Fig. 7, the sum of the average of the diodes D_1 and D_2 over one switching period can be earned as follows:

$$I_{D1,av} + I_{D2,av} = \frac{1}{2} \times D_{m2} \times I_{D-PK} \tag{26}$$

Where, D_{m2} is duty cycle in state 2 under DCM and I_{D-pk} is sum of the inductors L_1, L_2 and L_3 peak currents.

$$I_{D-pk} = I_{L1-pk} + I_{L2-pk} + I_{L3-pk} = \frac{V_i D T_s}{L_e} \tag{27}$$

Where,

$$\frac{1}{L_e} = \frac{1}{L_1} + \frac{1}{L_2} + \frac{1}{L_3} \tag{28}$$

By using volt-sec balance on inductors L_1, L_2 and L_3 duty cycle in state 2 under DCM (D_{m2}) can be obtained as follows:

$$D_{m2} = \frac{2DV_i}{V_o} \tag{29}$$

According to (24)-(29), the voltage gain of the converter in discontinuous conduction mode (M_{DCM}) can be achieved as follows:

$$M_{DCM} = \frac{D}{\sqrt{\tau_L}} \tag{30}$$

Where, the normalized inductor time constant τ_L is obtained as follows:

$$\tau_L = \frac{2L_e}{RT_s} \tag{31}$$

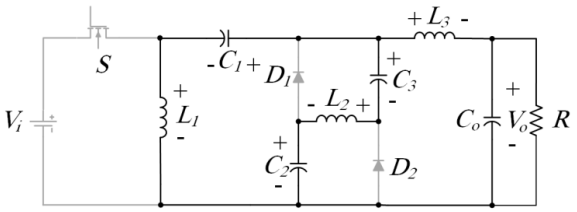


Fig. 6. Equivalent circuits of the presented converter in third mode at DCM operation

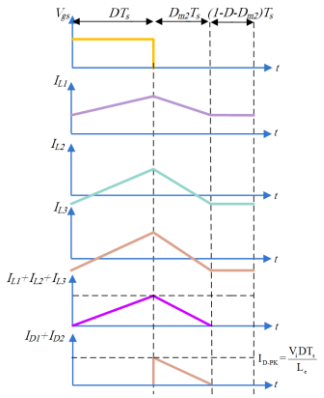


Fig. 7. Some illustrated waveforms of the proposed converter at DCM operation

D. Boundary condition mode

When the proposed converter is operated in boundary conduction mode (BCM) operation, the voltage gain in CCM is equal to DCM. Combing (12) and (30), the boundary normalized inductor time constant (τ_b) is:

$$\tau_b = \frac{(1-D)^2}{4} \tag{32}$$

Fig 8. shows the boundary normalized inductor time constant curve (τ_b). When τ_L is larger than τ_b, the presented buck-boost converter operates in CCM.

The boundary normalized inductor time constant curves for the proposed and the ZETA converter are shown in Fig. 9.

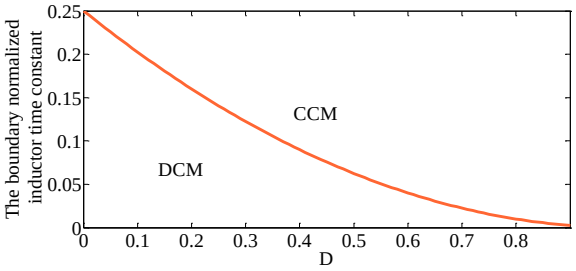


Fig. 8. Boundary normalized inductor time constant versus duty cycle

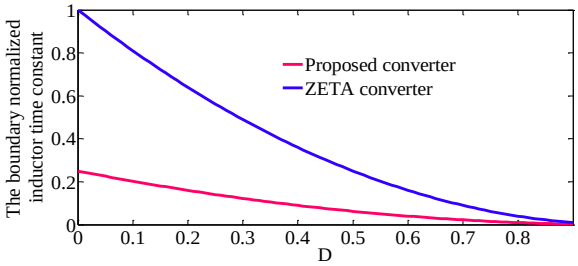


Fig. 9. Curves of boundary inductor time constant comparison of proposed converter and other converters

E. Efficiency analysis

For efficiency analysis of the presented buck-boost converter, parasitic resistances are defined as follows: switch on-state resistances is r_{DS}, forward resistances of the diodes D_1 and D_2 are R_{F1} and R_{F2} respectively, V_{F1} and V_{F2} are the threshold voltages of the diodes D_1 and D_2 respectively, inductors L_1, L_2 and L_3 equivalent series resistances (ESR) are R_{L1}, R_{L2} and R_{L3} respectively, the capacitors C_1, C_2, C_3 and C_o ESR are r_{C1}, r_{C2}, r_{C3} and r_{Co} respectively and the voltage ripple of the capacitors and the inductors is ignored.

The condition loss of the switch S (P_{rDS}) can be obtained as follows:

$$P_{rDS} = r_{DS} I_{S,rms}{}^2 = r_{DS} \frac{4D}{(1-D)^2} I_o{}^2 \tag{33}$$

The proposed converter switching loss (P_{Sw}) can be achieved as follows:

0278-0046 (c) 2018 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2019.2902785, IEEE Transactions on Industrial Electronics

$$P_{Sw} = f_s C_S V_S{}^2 = f_s C_S \left(\frac{V_i}{1-D}\right)^2 \quad (34)$$

The total losses of the switch S (P_{Switch}) can be achieved as follows:

$$P_{Switch} = P_{rDS} + \frac{P_{Sw}}{2} \quad (35)$$

The losses of the diodes D_1 and D_2 $(P_{D1,2})$ can be obtained as follows:

$$P_{D1,2} == R_{F1,2}\frac{1}{1-D} I_o{}^2 + V_{F1,2} I_o \quad (36)$$

The losses of capacitors C_1, C_2, C_3 and C_o $(P_{C1,2,3,o})$ can be derived as:

$$P_{C1,2,3,o} = r_{C1}\frac{4DP_o}{(1-D)R} + r_{C2,3}\frac{DP_o}{(1-D)R} + r_{Co}\frac{(1-D)^2 RP_o}{48L_3{}^2 f_s{}^2} \quad (37)$$

The losses of inductors L_1, L_2 and L_3 $(P_{L1,2,3})$ can be achieved as follows:

$$P_{L1,2,3} = R_{L1}\left(\frac{2D}{1-D}\right)^2 \frac{P_o}{R} + R_{L2,3}\frac{P_o}{R} \quad (38)$$

The total loss of the proposed converter (P_{Loss}) can be expressed as follows:

$$P_{Loss} = P_{Switch} + \sum_{u=1}^{2}(P_{RF})_{Du} + \sum_{u=1}^{2}(P_{VF})_{Du} + \sum_{u=1}^{3} P_{RCu} + P_{RCo} + P_{rL1} + P_{rL2} + P_{rL3} \quad (39)$$

The efficiency of the proposed converter (η) can be achieved as follows:

$$\eta = \frac{P_O}{P_O + P_{Loss}} = \frac{1}{1+\frac{P_{Loss}}{P_O}} \quad (40)$$

According to above equations, the proposed converter efficiency can be obtained as follows:

$$\eta = \frac{1}{1+\frac{A_1}{R(1-D)^2} + r_{Co}\frac{(1-D)^2 R}{48Lf_s{}^2} + \frac{f_s C_s V^2{}_i}{2(1-D)^2 RI^2{}_o}} \quad (41)$$

Where,

$$A_1 = 4Dr_{DS} + (1-D)(R_{F1}+R_{F2}) + \frac{(1-D)^2}{I_o}(V_{F1}+V_{F2}) + 4D(1-D)r_{C1} + D(1-D)(r_{C2}+r_{C3}) + 4D^2 R_{L1} + (1-D)^2(R_{L2}+R_{L3}) \quad (42)$$

F. Voltage stress

The voltage stress of the converter is an important parameter in the circuits. The voltage stress of the diodes and switch can be achieved as follows:

$$V_S = \frac{V_i}{1-D} \quad (43)$$

$$V_{D1} = V_{D2} = \frac{V_i}{1-D} \quad (44)$$

From (43) and (44), the voltage stresses of the diodes and switch are smaller than the output voltage. The comparison of the normalized voltage stress of the switch for the proposed converter and ZETA converter is shown in Fig. 10. The normalized voltage stress of the ZETA converter is higher than the presented converter therefore; the switch with low conduction loss can be selected.

Table I shows the comparison among the voltage stress, voltage gain and the number of elements of the converters. According to Table I, the voltage gain of the proposed converter is higher than other converters comparing to the number of elements. The normalized voltage stress of the proposed converter is lesser than other converters and the structure of the converter is simple. The switch number of the proposed converter is lesser than that in the other converters.

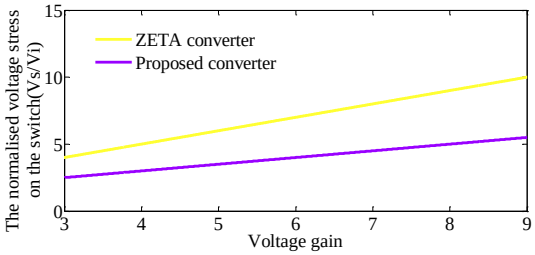


Fig. 10. Normalized switch voltage stress of the proposed converter versus voltage gain

TABLE I
COMPARISON BETWEEN PROPOSED CONVERTER AND OTHER STRUCTURES

	Proposed converter	Converter in [24]	ZETA converter	KY converter in [19]
Quantities of switches	1	3	1	2
Quantities of diodes	2	3	1	1
Quantities of capacitors	4	1	2	3
Quantities of inductors	3	2	2	2
Total device count	10	10	6	8
Voltage stress of the switch	$\frac{V_o+2V_i}{2V_i}$	1 $\frac{V_o}{V_i}$ $\frac{V_o}{V_i}$	$\frac{V_o+V_i}{V_i}$	$\frac{V_o}{V_i}$
Voltage gain	$\frac{2D}{1-D}$	$\frac{2D}{1-D}$	$\frac{D}{1-D}$	$2D$
$V_{Diode(Max)}/V_o$	$\frac{1}{2D}$	1	$\frac{1}{D}$	$\frac{1}{2}$

G. Calculation of the voltage ripple of the capacitors

According to Fig. 11, the capacitor C_1 voltage ripple called ΔV_{C1}, $\Delta V_{C1,ESR}$ is created from the voltage ripple composed from the current of the equivalent series resistance of the capacitor C_1 and the voltage ripple created from the charging and discharging of the capacitor C_1 is denoted by $\Delta V_{C1,cap}$. Fig. 12. shows the voltage and current of the capacitors C_2 and C_3. Therefore, the voltage ripple of the capacitor C_1 can be obtained as follows:

$$\Delta V_{C1} = \Delta V_{C1,ESR} + \Delta V_{C1,cap} \quad (45)$$

0278-0046 (c) 2018 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2019.2902785, IEEE Transactions on Industrial Electronics

$\Delta V_{C1,ESR}$ can be achieved as follows

$$\Delta V_{C1,ESR} = ESR_{C1}\Delta I_{C1} \simeq ESR_{C1}(I_{C1,on} - I_{C1,off}) = \frac{ESR_{C1}(4D)V_i}{(1-D)^2 R} \quad (46)$$

Where,

$$ESR_{C1} = \frac{\tan\delta_{C1}}{2\pi f_s} \quad (47)$$

Where, $\tan\delta_{C1}$ is the dissipation factor of capacitor C_1.

$\Delta V_{C1,cap}$ can be obtained as follows:

$$\Delta V_{C1,cap} = \frac{I_{C1,on}DT_s}{C_1} = \frac{2DT_sV_o}{RC_1} \quad (48)$$

Similarly, the voltage ripple of the capacitors C_2 and C_3 $\left(\Delta V_{C2,3}\right)$ can be expressed as follows:

$$\Delta V_{C2,3} = \Delta V_{C2,3,ESR} + \Delta V_{C2,3,cap} = \frac{ESR_{C2,3}(2D)V_i}{(1-D)^2 R} + \frac{DT_sV_o}{RC_{2,3}} \quad (49)$$

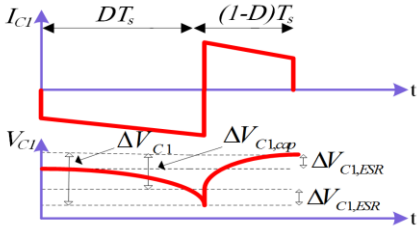


Fig. 11. The current and voltage of the capacitor C_1

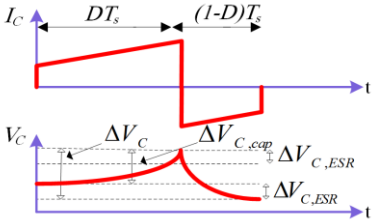


Fig. 12. The current and voltage of the capacitors C_2 and C_3

H. Capacitors and inductors design

The theoretical value of the inductors L_1, L_2 and L_3 to work in CCM can be derived as follows:

$$L_1 \geq \frac{V_o(1-D)^2}{8DI_of_s} = \frac{80\times(1-0.53)^2}{8\times0.53\times2.5\times40\times10^3} = 41\mu H \quad (50)$$

$$L_{2,3} \geq \frac{V_o(1-D)}{4I_of_s} = \frac{80\times(1-0.53)}{4\times2.5\times40000} = 94\mu H \quad (51)$$

The theoretical value of the capacitors C_1, C_2, C_3 and C_o can be achieved as follows:

$$C_1 \geq \frac{2DT_sV_o}{R\Delta V_{C1}} = \frac{2DV_o}{R\times0.01\times V_o\times f_s} = \frac{2\times0.53\times80}{32\times0.01\times80\times40000} = 82\mu F \quad (52)$$

$$C_{2,3} \geq \frac{DT_sV_o}{R\Delta V_{C2,3}} = \frac{DV_o}{R\times0.01\times V_o\times f_s} = \frac{0.53\times80}{32\times0.01\times80\times40000} = 41\mu F \quad (53)$$

$$C_o \geq \frac{V_o(1-D)}{16L_3f_s^2\Delta V_{Co}} = \frac{100\times(1-0.53)}{16\times.001\times(40\times10^3)^2\times1} = 1.8\mu F \quad (54)$$

IV. Experimental Results

In order to verify the performance of the presented converter, experimental results are provided. The presented buck-boost converter is operated in the step-up and step-down modes.

The proposed converter utilized components are as follows:

1) input voltage : 36 V
2) switching frequency: 40 kHz
3) switch: IRFP460A
4) diodes D_1 and D_2 : MUR860
5) inductor L_1 : 900 µH
6) inductors L_2 and L_3 : 1mH
7) capacitors C_1, C_2 and C_3 : 100 µF
8) capacitor C_o : 100 µF

The presented converter is tested under CCM. In the step-up mode, the output voltage is shown in Fig. 13(a). The output voltage is 80 V and the output power is 200 W. Figs. 13(b), 13(c) and 13(d) show the waveform of the inductors currents of L_1, L_2 and L_3 respectively. According to (13), (18) and (20), the average of inductors currents of L_1, L_2 and L_3 are 5.6, 2.5 and 2.5 A respectively. The diode D_2 voltage waveform is similar to diode D_1 voltage waveform. The voltage on the diodes D_1 and D_2 is given in Fig. 13(e). According to (44), the voltage across the diodes D_1 and D_2 is equal to 75 V. The voltage on the switch S is shown in Fig. 13(f). According to (43), the switch S voltage is 75 V. The voltage of inductors L_1, L_2 and L_3 is shown in Fig. 13(g). The voltage of inductors L_1, L_2 and L_3 during state 1 is 36 V and during state 2 is equal to -40 V. In the step-down mode, the output voltage is shown in Fig. 14(a). The output voltage is 18 V. Figs. 14(b), 14(c) and 14(d) shows the waveform of the inductors currents of L_1, L_2 and L_3 respectively. According to (13), (18) and (20), the average of inductors currents of L_1, L_2 and L_3 are 0.3, 0.6 and 0.6 A respectively. The voltage on diodes D_1 and D_2 is shown in Fig. 14(e). According to (44), the voltage on D_1 and D_2 is equal to 45 V.

Fig. 15 shows the efficiency curves of converters with different output power. It is seen that the efficiency of proposed converter is higher than that of ZETA converter and converter in [18] and the theoretical efficiency of the proposed converter is higher than the experimental efficiency. Fig. 16 shows the curve of efficiency of the proposed converter versus

0278-0046 (c) 2018 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2019.2902785, IEEE Transactions on Industrial Electronics

load current in step-up mode. It is seen that the theoretical efficiency of the presented converter is higher than the experimental efficiency.

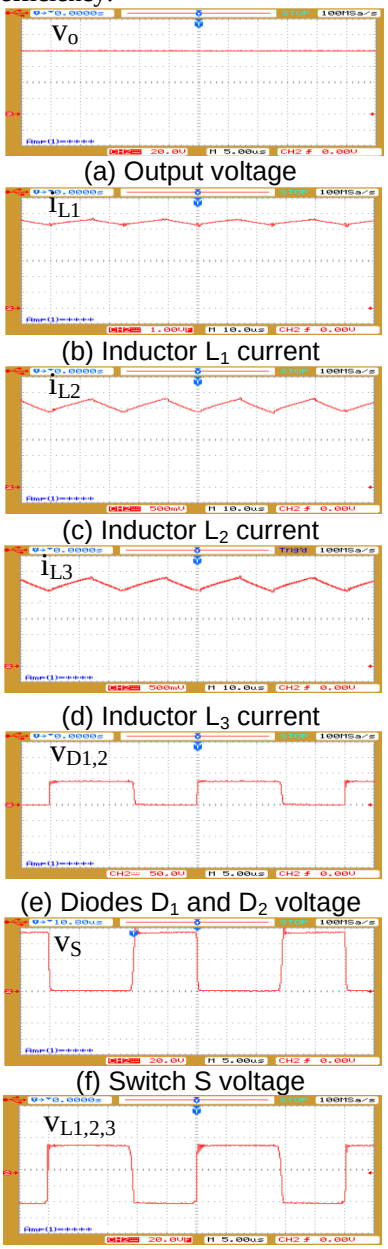
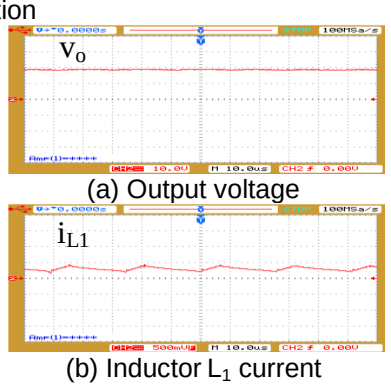


Fig. 13. Experimental results in step-up mode and under CCM operation



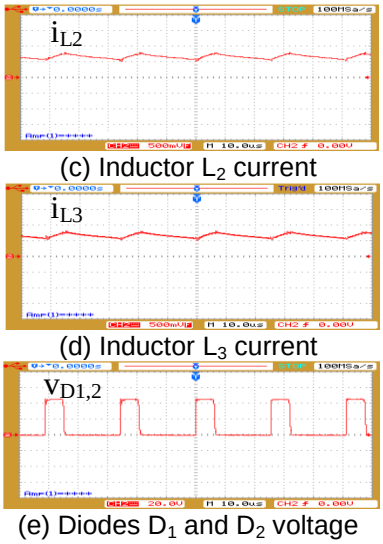


Fig. 14. Experimental results in step-down mode and under CCM operation

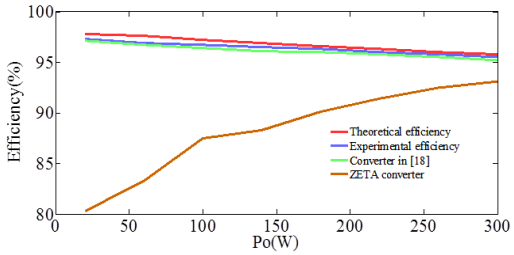


Fig. 15. Measured efficiency of the proposed converter versus output power

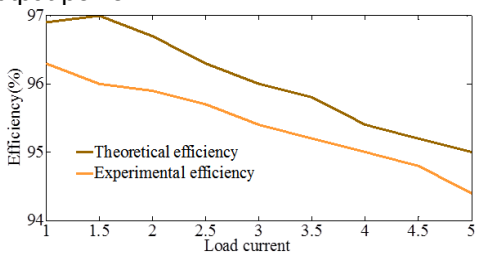


Fig. 16. Measured efficiency of the proposed converter versus load current in step-up mode

V. Conclusion

In this paper, a novel transformerless buck boost converter based on ZETA converter is presented. In this converter, only one main switch is used, which decreases the losses and improves efficiency. The active switch voltage stress is low and switch with low on-state resistance can be utilized. The voltage gain of the converter is higher than that of the classic boost, buck-boost, ZETA, CUK and SEPIC converters. The presented converter structure is simple; hence, the converter control is simple. The buck-boost converters are used in some applications such as fuel-cell, car electronic devices, and LED drivers. Finally, the experimental results are given to verify the proposed converter.

0278-0046 (c) 2018 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2019.2902785, IEEE Transactions on Industrial Electronics

REFERENCES

[1] W. Li and X. He, "Review of nonisolated high-step-up DC/DC converters in photovoltaic grid-connected applications," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1239-1250, Apr. 2011.

[2] H. S. Lee, H. J. Choe, S. H. Ham and B. Kang, "High-efficiency asymmetric forward-flyback converter for wide output power range," *IEEE Trans. Power Electron*., vol. 32, no. 1, pp. 433-440, Jan. 2017.

[3] N. Mohan, T. M. Underland, W. P. Robbins, "Power Electronics Converters,Applications and Design" Wiley, New York, USA, 2nd Edition, 1995.

[4] H. Tao, J. L. Duarte, M. A. M. Hendrix, "Line-interactive UPS using a fuel cell as the primary source," *IEEE Trans. Ind. Electron.*, vol. 55, no. 8, pp. 3012-3021, Aug. 2008.

[5] P. James, A. Forsyth, G. Calderon-Lopez, V. Pickert "DC-DC converter for hybrid and all electric vehicles," EVS24 Stavanger, Norway, May 13-16, 2009.

[6] H. S. Chung, A. Ioinovici, and W. Cheung, "Generalized structure of bidirectional switched-capacitor dc/dc converters," *IEEE Trans. Circuit Syst. I, Fundam. Theory Appl.*, vol. 50, no. 6, pp. 743–753, Jun. 2003.

[7] K. K. Law, K. W. E. Cheng, and Y. P. B. Yeung, "Design and analysis of switched-capacitor-based step-up resonant converters," *IEEE Trans. Circuit Syst. I, Fundam. Theory Appl.*, vol. 52, no. 5, pp.1998–2016, May. 2005.

[8] F. Zhang, L. Du, F.Z. Peng and Z. Qian, "A new design method for high-power high-efficiency switched-capacitor DC-DC converters," *IEEE Trans. Power Electron*., vol. 23, no. 2. pp. 832-840, Mar. 2008.

[9] T. Wu, Y. lai, J.C. Hung and Y. Chen, "Boost converter with coupled inductors and buck-boost type of active clamp," *IEEE Trans. Ind. Electrons*., vol. 55, no. 1. pp. 154-162, Jan. 2008.

[10] A. Tahavorgar and J. E. Quaicoe, "A dual series-resonant DC–DC converter," *IEEE Trans. Power Electron*., vol. 32, no. 5, pp. 3708-3718, May. 2017.

[11] Y. Zhao, W. Li and X. He, "Single-phase improved active clamp coupled-inductor-based converter with extended voltage doubler cell," *IEEE Trans. Power Electron*., vol. 27, no 6, pp. 2869-2878, Jun. 2012.

[12] S. Miao, F. Wang and X. Ma, "A new transformerless buck–boost converter with positive output voltage," *IEEE Trans. Ind. Electron*., vol. 63, no. 5, pp. 2965-2975, May. 2016.

[13] G. Wu, X. Ruan and Z. Ye, "Nonisolated high step-up DC–DC converters adopting switched-capacitor cell," *IEEE Trans. Ind. Electron*., vol. 62, no. 1, pp. 383-393, Jan. 2015.

[14] K. I. Hwu and W. Z. Jiang, "Analysis, design and derivation of a two-phase converter," *IET Power Electron*., vol. 8, no. 10, pp. 1987-1995, Oct. 2015.

[15] S. Hou, J. Chen, T. Sun and X. Bi, "Multi-input step-up converters based on the switched-diode-capacitor voltage accumulator," *IEEE Trans. Power. Electron*., vol. 31, no. 1, pp. 381-393, Jan. 2016.

[16] S. Dwari and L. Parsa , "An efficient high-step-up interleaved dc-dc converter with a common active clamp," *IEEE Trans. Power Electron.*, vol. 26, no. 1, pp. 66-78, Jan. 2011.

[17] B. R. Lin, J. J. Chen, "Analysis of an integrated flyback and Zeta converter with active clamping technique," *IET Power Electron.*, vol. 2, no. 4, pp. 355-363, Jul. 2009.

[18] M. R. Banaei, H. A. F. Bonab, "A novel structure for single-switch nonisolated transformerless buck–boost DC–DC converter," *IEEE Trans. Ind. Electron*., vol. 64, no. 1, pp. 198-205, Jan. 2017.

[19] K. I. Hwu and T. J. Peng, "A novel buck boost converter combining KY and buck converters", *IEEE Trans. Power Electron.*, vol. 27 , no. 5 , pp. 2236 -2241, May. 2012.

[20] N. Valsalan and S. T. Subha, "Dual zeta converter with reduced ripple for sensitive load applications," *in Proc International Conference on Energy Efficient Technologies for Sustainability*, pp. 1195-1200, 2013.

[21] J. Ai and M. Lin, "High step-up DC–DC converter with low power device voltage stress for a distributed generation system," *IET Power Electron*., vol. 11, no. 12, pp. 1955-1963, Oct. 2018.

[22] Y. Chen, Z. Lu and R. Liang, "Analysis and Design of a Novel High-Step-Up DC/DC Converter With Coupled Inductors," *IEEE Trans. Power Electron*., vol. 33, no. 1, pp. 425-436, Jan. 2018.

[23] A. Rajaei, R. Khazan, M. Mahmoudian, M. Mardaneh and M. Gitizadeh, "A Dual Inductor High Step-Up DC/DC Converter Based on the Cockcroft–Walton Multiplier," *IEEE Trans. Power Electron*., vol. 33, no. 11, pp. 9699-9709, Nov. 2018.

[24] H. K. Liao, T. J. Liang, L. S. Yang and J. F. Chen, "Non-inverting buck–boost converter with interleaved technique for fuel-cell system," *IET Power Electron*., vol. 5, no. 8, pp. 1379-1388, Sep. 2012.

[25] M. R. Banaei and H. A. F. Bonab, "A nonisolated transformerless high voltage gain buck boost dc-dc converter," *Modares Journal of Electrical Engineering*., vol. 15, no. 3, pp. 9-19, 2015.

[26] M. R. Banaei and H. A. F. Bonab, "High Efficiency Transformerless Buck Boost dc dc Converter," *Int. J. Circ. Theor. Appl*., vol. 45, no. 8, pp. 1129-1150, Aug. 2017.

[27] H. A. F. Bonab and M. R. Banaei, "A Novel High Step-Up DC-DC Converter Based on KY Converter," *JEEE Journal*., vol. 10, no. 1, pp. 5-10, 2016.

Mohamad Reza Banaei was born in Tabriz, Iran. He received his M.Sc. degree from the Poly Technique University of Tehran, Iran, in control engineering in 1999 and his Ph.D. degree from the electrical engineering faculty of Tabriz University in power engineering in 2005. He is a Professor in the Electrical Engineering Department of Azarbaijan Shahid Madani University, Iran, which he joined in 2005. His main research interests include the designing and controlling of power electronic converters, renewable energy systems, modeling and controlling of FACTS and Custom Power devices and power systems dynamics.

Hossein Ajdar Faeghi Bonab was born in Bonab, Iran, in 1991. He received the B.S. degree in power engineering from Tabriz university, Iran, and the M.S. degree in power engineering from Azarbaijan Shahid Madani university, Iran , in 2012 and 2015, respectively. His research interests are power electronics converters, dc–dc converters and renewable energy.

0278-0046 (c) 2018 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.