

Analysis on the Performance of a Three-phase Cascaded H-Bridge Multilevel Inverter

N. A. Azli, *Member IEEE* and Y. C. Choong

Abstract—Previous works have pointed out the limitations of conventional inverters especially in high voltage and high power applications. In recent years, multilevel inverters are becoming increasingly popular for high power applications due to its improved harmonic profile and increased power ratings. Works on the aspect of topology, control techniques and applications of multilevel inverters have been reported in literatures. However, there are no concrete findings that actually discuss or evaluate the performance of a three-phase multilevel inverter. This paper presents some analysis on the performance of a 5-level cascaded H-bridge multilevel inverter (CHMI) based on a multi-carrier sinusoidal pulse width modulation (MSPWM) control technique. Performance analysis are made based on the results of a simulation study conducted on the operation of the CHMI using MATLAB/Simulink. The performance parameters chosen in the work include the waveform pattern, harmonic spectrum, fundamental value, and total harmonic distortion (THD) of the three-phase CHMI output voltage. From the results of the simulation study and the analysis conducted, several distinct features of the three-phase 5-level CHMI employing the MSPWM control scheme, in particular the phase disposition (PD) type of the carrier disposition (CD) method from the aspect of line voltage have been identified.

Index Terms—Multilevel inverter, cascaded, three-phase, high power applications

I. INTRODUCTION

Switch-mode inverters are used in various power electronics applications that request for control of both the magnitude and frequency of an AC output. Practically, inverters are used in both single-phase and three-phase AC systems. A half-bridge inverter is the simplest topology, which is used to produce a two-level square-wave output waveform. A center-tapped voltage source supply is needed in such a topology. On the other hand, the full-bridge topology is used to synthesize both three-level and two-level output waveforms.

However, there are many limitations for these conventional two-level and three-level inverters in handling high voltage and high power conversion. For higher output voltage capacity and reduction in harmonic distortion, these converters are connected in series using transformers, which are the main

contributor to problems such as bulkiness, high loss and high cost to the overall AC system. Besides that, conventional inverters have some disadvantages operating at high frequency mainly due to switching losses and constraints of the device ratings. There are also concerns on the complex structure due to dynamic voltage balance circuit [1].

Hence, multilevel inverters are emerging as a new breed of power converter option for high power applications, which can create high voltage and reduce harmonics by its own circuit topology [1]. Multilevel inverters are applied in many high to medium power industrial applications such as AC power supplies, static VAR compensators and drive systems. By synthesizing the AC output terminal voltage from several levels of DC voltages, staircase output waveform can be produced. This allows for higher output voltage and simultaneously lowers the switches' voltage stress. Multilevel inverters have become an effective and practical solution for reducing switching losses in high power applications [2]. Furthermore, as the number of voltage levels on the DC side increase, the synthesized output adds more steps, producing an output which approaches the sinusoidal wave with minimum harmonic distortion. Thus the requirement of output filter is reduced [3].

The results of a patent search show that multilevel inverter circuits have been around for more than 25 years [4]. The evolution of the multilevel inverters begins with the introduction of the neutral point clamped inverter topology by Nabae et. al. The resultant three-level output voltage waveform of this topology has considerably better spectral performance compared to that of the conventional inverter. The spectral structure of the output waveforms was then improved by Bhagwat and Stefanovic by using multiple levels. In addition to improving the waveform quality, these multilevel inverters substantially reduce voltage stress on the devices. Such inverters are generically known as diode-clamped multilevel inverters (DCMI). With this type of multilevel inverter, the required voltage blocking capability of the clamping diodes varies with the levels. An alternative to the DCMI is the flying capacitor multilevel inverter proposed by Meynard. Instead of clamping diodes, the voltage across an open switch in this inverter topology is constrained by clamping capacitors.

A much simpler multilevel inverter topology with less power devices requirement compared to the previously mentioned ones is known as the cascaded H-bridge multilevel inverter (CHMI). The main drawback of this topology is the

N. A. Azli is with the Energy Conversion Department (ENCON), Faculty of Electrical Engineering, Universiti Teknologi Malaysia, 81310 UTM Skudai, Malaysia (e-mail: naziha@ieee.org).

Y. C. Choong was a student at the Energy Conversion Department (ENCON), Faculty of Electrical Engineering, Universiti Teknologi Malaysia, 81310 UTM Skudai, Malaysia in 2005.

isolated DC power supply requirement for each of its stages which on the other hand makes it attractive for use in applications related to renewable or alternate energy sources that can offer readily available DC output. Various literatures in recent years have reported the utilization of the single-phase and three-phase CHMI in both static and drive applications. However, detail analysis on the performance of the three-phase CHMI in particular has not been clearly revealed.

Thus this paper presents some of the features of a three-phase CHMI that are identified in terms of various performance parameters based on the results of a simulation study. The following section briefly describes the three-phase CHMI circuit configuration and the different types of multi-carrier sinusoidal pulse width modulation (MSPWM) techniques. Then, the results of the simulation study are presented and analyzed before highlighting the main features of the three-phase CHMI as the conclusion of the paper.

II. THREE-PHASE CHMI CIRCUIT CONFIGURATION

For a three-phase system, the output of three identical structure of single-phase CHMI can be connected in either wye or delta configuration. Fig. 1 illustrates the schematic diagram of a wye-connected m-level CHMI with separate DC sources.

For a three-phase 5-level CHMI, two H-bridge cells with eight switches are needed per phase. Thus a total of six H-bridge cells involving 24 power switches are required for this circuit configuration. This means that twelve pairs of gating signals have to be generated to be fed to the switches. For each H-bridge cell, the switchings are designed in such a way that only one pair of switches operate at the carrier frequency while the other pair operates at the reference frequency, thus having two high-frequency switches and two low-frequency switches.

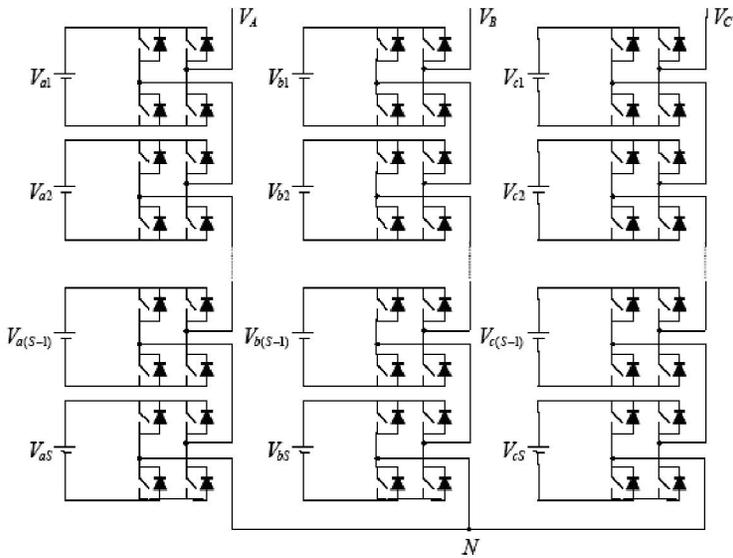


Fig. 1. A general three-phase wye configuration CHMI

From Fig. 1, V_{AN} is the voltage of phase A, which is the sum of V_{a1} , V_{a2} , ... $V_{a(s-1)}$ and V_{as} . The same idea applies to phase B and phase C. The line voltages are then expressed in terms

of two phase voltages. For example, the potential between phase A and B is V_{AB} , which can be computed from:

$$V_{AB} = V_{AN} - V_{BN} \tag{1}$$

where,

V_{AB} is the line voltage

V_{AN} is the voltage of phase A with respect to neutral point N

V_{BN} is the voltage of phase B with respect to neutral point N

III. MULTI-CARRIER SINUSOIDAL PULSE WIDTH MODULATION (MSPWM) TECHNIQUE

A. Basic principle

The principle of MSPWM is to use several triangular carrier signals with only one modulation signal per phase. For an m-level inverter, (m-1) triangular carriers of the same frequency f_c and amplitude A_c , are disposed so that the bands they occupy are contiguous. The zero reference is placed in the middle of the carrier set. The modulation signal is a sinusoidal of frequency f_m and amplitude A_m . At every instant each carrier signal is compared with the reference modulation signal. Each comparison switches the device on if the reference signal is greater than the triangular carrier assigned to that level. Otherwise, the device switches off [1].

For a three-phase 5-level CHMI, four carrier waveforms are needed and compared at every one time to a set of three reference waveforms, each 120° phase shifted apart [5]. Fig. 2 shows the MSPWM technique for a three-phase 5-level CHMI.

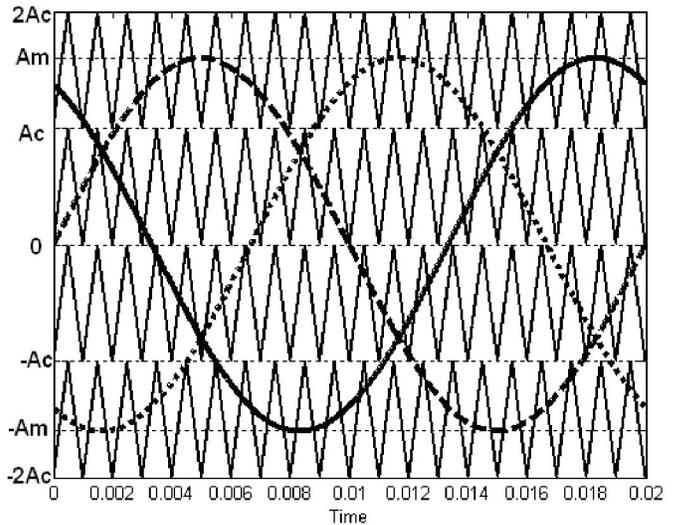


Fig. 2. MSPWM technique for a 3-phase 5-level CHMI

There are three main parameters that need to be considered in the MSPWM technique [5] which include the amplitude modulation index, m_a defined as,

$$m_a = \frac{A_m}{N'A_c} \tag{2}$$

where,

$$N' = \frac{(m-1)}{2} \quad (3)$$

where,

m is the number of levels of the multilevel inverter (odd)

A_m is the amplitude of the modulating signal

A_c is the peak to peak value of the carrier (triangular) signal

The frequency modulation index, m_f is defined as,

$$m_f = \frac{f_c}{f_m} \quad (4)$$

where,

f_c is the frequency of the carrier signal

f_m is the frequency of the modulating signal

The third parameter is the displacement angle between the modulating signal and the first positive triangular carrier signals. In this work, a zero displacement angle is applied.

B. Category and disposition methods

In general, the MSPWM technique can be categorized into Carrier Disposition (CD), Phase Shifted (PS) and hybrid (H) methods [7]. With the CD method, the reference waveform is sampled through a number of carrier waveforms displaced by contiguous increments of the reference waveform amplitude whereas for PS method, multiple carriers are phase shifted accordingly. On the other hand, H method is a combination of these two methods. In this work, the CD method will be employed to obtain the gating signals for the CHMI switches. With the CD method, three alternative carrier disposition schemes are available, namely Phase Disposition (PD), Phase Opposition Disposition (POD) and Alternative Phase Opposition Disposition (APOD) [6].

All the carrier signals as shown in Fig. 2 are in phase for the PD scheme. With the POD scheme, the carrier signals above the zero reference value are in phase. The carrier waveforms below the zero value are also in phase, but they are 180° phase shifted from those above zero. The APOD scheme on the other hand, requires each of the carrier signals to be phase shifted 180° alternately from its adjacent carrier [6]. Although in this work all three alternative carrier disposition schemes were applied to the three-phase CHMI, this paper emphasis more on the results based on the PD scheme in comparison to other schemes and the conventional three-phase bridge inverter employing SPWM technique.

IV. RESULTS AND ANALYSIS

The three-phase 5-level MSMI is simulated using MATLAB/Simulink. In the simulation study, it is assumed that the DC voltage input to each module is $E = 400V$, the output

voltage fundamental frequency is $f_m = 50$ Hz, while the inverter load is a pure resistive load. Analysis and comparison are done based on the results obtained from the line voltage of the three-phase CHMI employing the MSPWM technique (PD scheme), in terms of output voltage waveforms, output voltage harmonic spectrums, fundamental voltage and Total Harmonic Distortion (THD).

A. Effect of odd and even m_f on the line voltage waveforms

Fig. 3 and Fig. 4 show the waveforms of the line voltage for a three-phase 5-level CHMI, employing the PD scheme with $m_a = 0.8$ and $m_f = 39$ and $m_f = 60$ respectively.

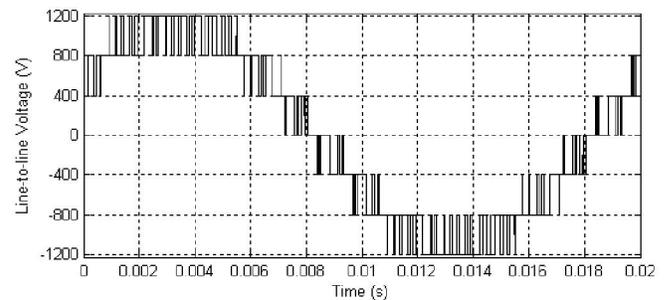


Fig. 3. Line voltage waveform for a three-phase CHMI with PD scheme ($m_f = 39$, $m_a = 0.8$)

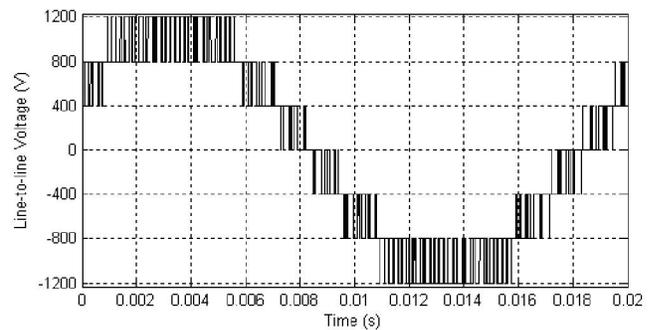


Fig. 4. Line voltage waveform for a three-phase CHMI with PD scheme ($m_f = 60$, $m_a = 0.8$)

From the figures, it can be noticed that the line voltage waveforms for the PD scheme are not symmetrical regardless of whether m_f is odd or even. When there is an increase in m_f while m_a remains constant, more switchings will appear in the waveforms. This is in accordance to (2). Since the fundamental frequency, f_m is always constant, when m_f increases, f_c also increases. As a result, there will be more intersections or comparisons between the modulating and the carrier signals.

B. Relationship between m_a and number of levels in the line voltage

Fig.5 to Fig. 8 show the line voltage waveforms for the three-phase 5-level CHMI, employing the PD scheme, with m_f fixed at 39 and varying m_a . Fig. 5 shows that the maximum

number of levels that can be synthesized by the line voltage is 9. Considering s as the number of DC sources per phase where $s = 2$ for the case of a 5-level CHMI, then in general, it can be deduced that the maximum achievable number of levels in the line voltage waveform is $4s + 1$.

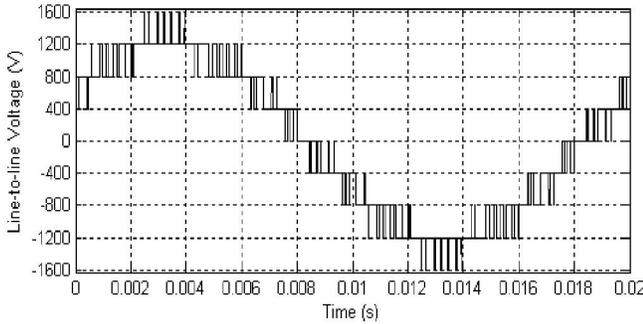


Fig. 5. Line voltage waveform for a three-phase CHMI with PD scheme ($m_r = 39, m_a = 0.9$)

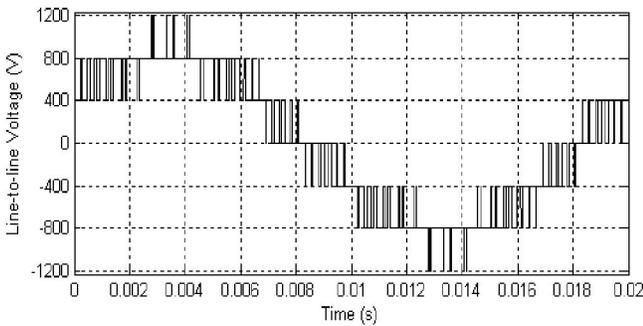


Fig. 6. Line voltage waveform for a three-phase CHMI with PD scheme ($m_r = 39, m_a = 0.6$)

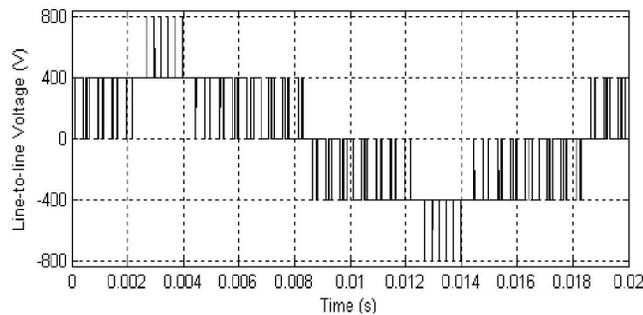


Fig. 7. Line voltage waveform for a three-phase CHMI with PD scheme ($m_r = 39, m_a = 0.3$)

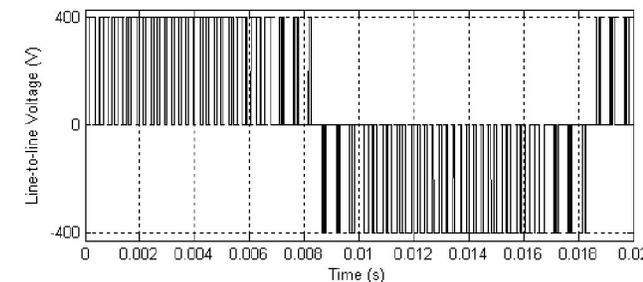


Fig. 8. Line voltage waveform for a three-phase CHMI with PD scheme ($m_r = 39, m_a = 0.2$)

Table 1 summarizes the results obtained from the simulation study. Compared to a single-phase 5-level CHMI with PD scheme which can only achieve two different levels of 3 and 5 in its output voltage waveform, the three-phase CHMI can achieve up to 9 levels. For higher levels three-phase CHMI, the synthesized line voltage waveforms are expected to become more similar to a sinusoidal with significant reduction in harmonic distortion. In addition the m_a for a three-phase CHMI can be adjusted much lower compared to a single-phase CHMI ($m_a < 0.6$) before it starts to function as a conventional 3-level inverter.

Table 1. Number of levels achieved by a three-phase CHMI with PD scheme ($m_r = 39$)

m_a	Number of levels
≥ 0.9	9
0.6 – 0.8	7
0.3 – 0.5	5
< 0.3	3

C. Harmonics analysis on the line voltage

Fig. 9 and Fig. 10 show the harmonic spectrums of line voltages of a 5-level three-phase CHMI employing the PD scheme. It is noticed from these figures that only odd harmonics occur for odd m_r while for even m_r both odd and even harmonics are detected. This characteristic is found to be similar to that of a single-phase CHMI. The harmonic spectrums of Fig. 9 and Fig. 10 do not indicate any highly significant harmonic due to the common mode cancellation between the inverter phase legs [8]. Instead, only the occurrence of the first significant harmonic is found to be the same as that of a single-phase 5-level CHMI (29 for $m_r = 39$, and 50 for $m_r = 60$). On the other hand, with m_r fixed to 39, as m_a is increased, the magnitude of the harmonics are found to decrease with the highest at only 5.1% of the fundamental component.

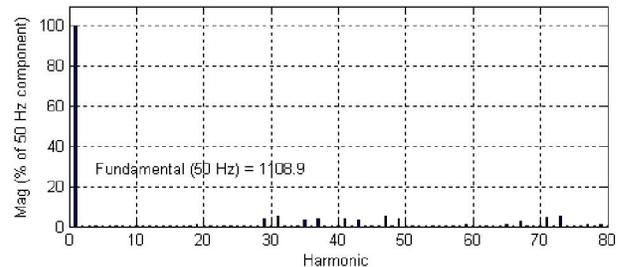


Fig. 9. Line voltage harmonic spectrum for a three-phase CHMI with PD scheme ($m_r = 39, m_a = 0.8$)

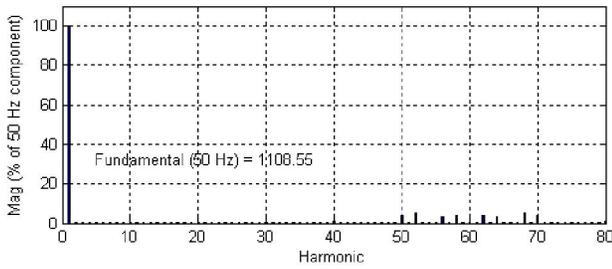


Fig. 10. Line voltage harmonic spectrum for a three-phase CHMI with PD scheme ($m_f = 60$, $m_a = 0.8$)

Fig. 11 and Fig. 12 show the line voltage harmonic spectrums for a three-phase 5-level CHMI employing the PD scheme with odd and triplen m_f (63) and odd m_f (65) respectively. The figures indicate similar harmonic pattern thus implying that there is no identifiable benefit in maintaining and odd and triplen m_f as compared to only add m_f . This is in contrast to the conventional three-phase SPWM inverter where by all the triplen harmonics are not present in the line voltage if m_f is chosen to be odd and triplen [9].

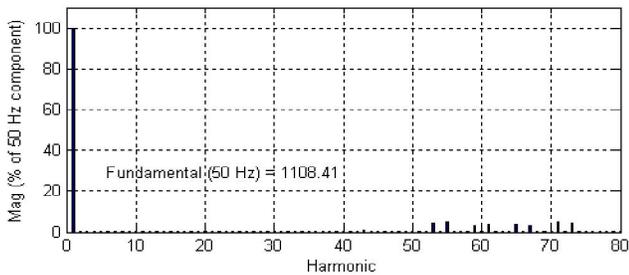


Fig. 11. Line voltage harmonic spectrum for a three-phase CHMI with PD scheme ($m_f = 63$, $m_a = 0.8$)

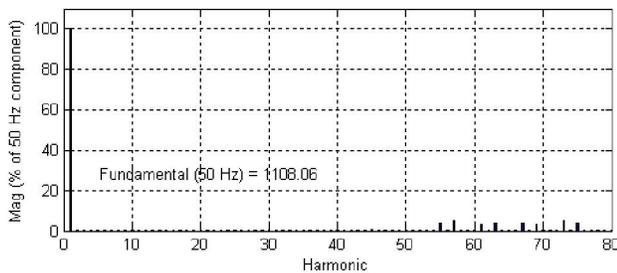


Fig. 12. Line voltage harmonic spectrum for a three-phase CHMI with PD scheme ($m_f = 65$, $m_a = 0.8$)

D. Relationship between m_a and inverter output voltage fundamental

Fig. 13 compares the output voltage fundamental of a three-phase 5-level CHMI employing the PD carrier disposition scheme, a single-phase 5-level CHMI with similar control scheme and a three-phase SPWM inverter. With the same DC voltage input, the CHMI output voltage fundamental (single-phase and three-phase) is very much higher compared to the conventional three-phase SPWM inverter which makes the

later attractive for high power applications. When m_a exceeds 1 (over-modulation), the output voltage fundamental no longer increases proportionally with m_a .

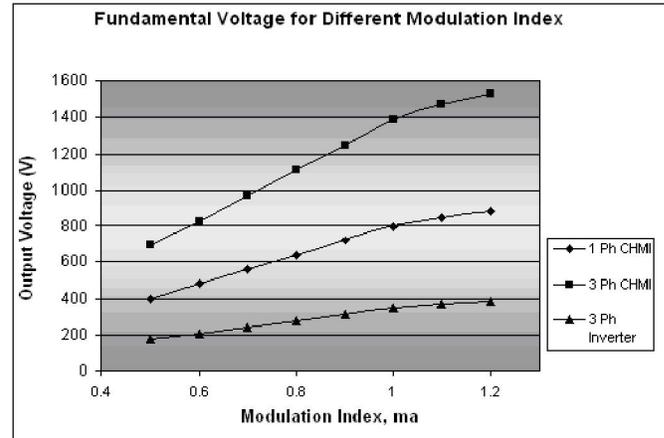


Fig. 13. Comparison of the output voltage fundamental

E. Total harmonic distortion (THD) of the line voltage

Fig. 14 shows the line voltage THD for the three-phase CHMI based on PD, APOD and POD carrier disposition schemes. From the results, it is found that PD scheme achieves the lowest line voltage THD compared to APOD and POD. The reason for this is related to the characteristic of the PD scheme mentioned earlier that involves cancellation of carrier harmonic between phase legs in the line voltage as can be inferred from the harmonic spectrums of Fig. 9 and Fig. 10.

Fig. 15 illustrates the phase voltage and line voltage THD performance of the PD scheme three-phase 5-level CHMI with different values of m_a . It can be depicted from the figure that the THD for the line voltage as well as phase voltage for the CHMI is inversely proportional to m_a . It is also shown as expected that at a particular m_a value, the line voltage THD is significantly much less than the phase voltage THD.

Fig. 16 compares the performance in THD when m_f varies for the PD scheme three-phase 5-level CHMI and the conventional three-phase SPWM inverter. Comparison is made for fundamental output voltage of 1108 V with m_a fixed at 0.8. In order to achieve the same fundamental output voltage, the DC input applied is 400V and 1600V for the CHMI and the conventional inverter respectively. From Fig. 16, it can be concluded that for the line voltage of the CHMI, the THD performance is nearly independent of m_f . This is because when m_f varies, the magnitude of the significant harmonics remains nearly the same, only the distance between the occurrence of the first significant harmonic will change according to the value of m_f . Thus, m_f does not actually play an important role in the THD performance of the inverters. Fig. 16 also proves that for the same fundamental output voltage, a three-phase CHMI achieves a much lower THD compared to the conventional three-phase inverter.

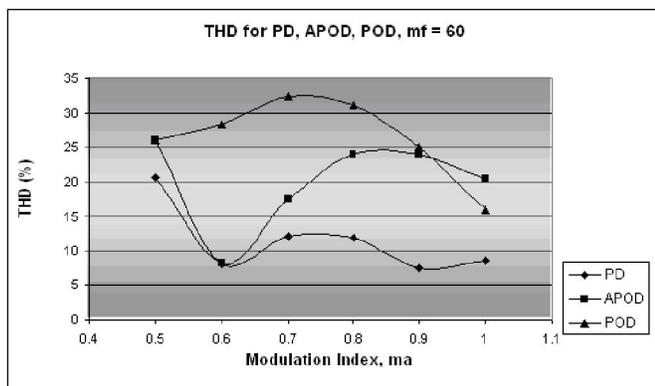


Fig. 14. Line voltage THD for three different carrier disposition schemes

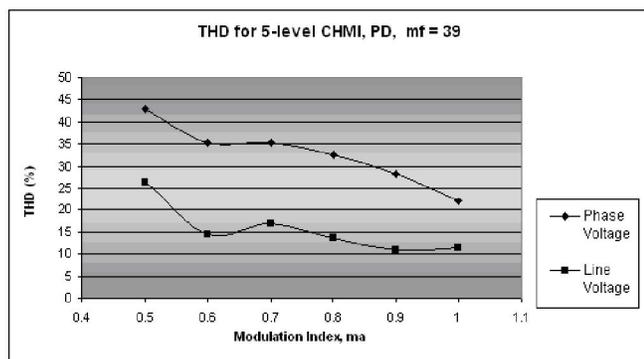


Fig. 15. THD performance for phase voltage and line voltage of a 5-level CHMI with PD scheme when m_a varies

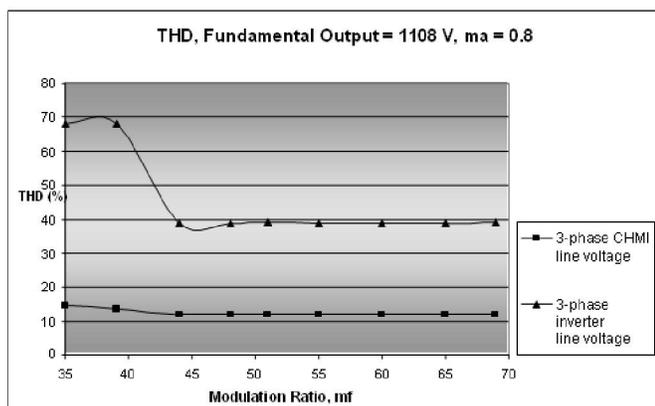


Fig. 16. THD performance at the same fundamental output voltage when m_f varies

V. CONCLUSIONS

From the simulation study conducted, several distinct features of the three-phase 5-level CHMI with PD scheme from the aspect of line voltage can be identified. The line voltage is able to synthesize more levels compared to the phase voltage, thus resembling a more desirable sinusoidal waveform. Besides that, the line voltage yields better spectral performance, hence reducing the need of an output filter. The three-phase CHMI is also able to produce line voltages with

higher fundamental but much lower THD as compared to the single-phase CHMI.

From the analysis, it can also be concluded that, in contrary to the conventional three-phase SPWM inverter, there is no particular benefit in the harmonic performance by applying an odd and triplen m_f to the 5-level CHMI. The PD scheme has advantages in three-phase applications due to the cancellation of the main carrier component between phase legs when the line voltages are formed. At high modulation index, the PD modulation strategy introduces the lowest line voltage THD.

As a conclusion, the results suggested that the three-phase CHMI is most suitable to operate at a high m_a not exceeding 1 and also a high m_f . High m_a promises a higher fundamental output voltage, more number of levels and also lower significant harmonics. On the other hand, a higher m_f ensures that the distance between the fundamental component and the first significant harmonic is greater, thus easing the filtering process.

VI. REFERENCES

- [1] H. Y. Wu, X. N. He, "Research on PWM Control of a Cascade Multilevel Converter", Proc. of the Third International Conference on Power Electronics and Motion Control, pp. 1099-1103, 2000.
- [2] J. A. Aziz and Z. Salam, "A PWM Strategy for the Modular Structured Multilevel Inverter Suitable for Digital Implementation.", Proc. of the IEEE International Power Electronics Congress, pp. 160-164, 2002.
- [3] Ye Ye Mon, W. W. L. Keerthipala, Tan Li San, "Multi-modular Multilevel Pulse Width Modulated Inverters.", Proc. of International Conference of Power System Technology, pp. 469-474, 2000.
- [4] J. Rodriguez, J-S. Lai and F. Z. Peng, "Multilevel Inverter: A Survey of Topologies, Controls and Applications." *IEEE Transactions on Industrial Electronics*, Vol. 49, No. 4, pp. 724-738, 2002.
- [5] G. Carrara, S. Gardella, M. Marchesoni, R. Salutari and C. Sciuotto, "A New Multilevel PWM Method: A Theoretical Analysis." *IEEE Transactions on Power Electronics*, Vol. 7, No. 3, pp. 497-505, 1992.
- [6] L. M. Tolbert, T. G. Habetler, "Novel Multilevel Inverter Carrier-Based PWM Method." *IEEE Transactions on Industry Applications*, Vol. 35, No. 5, 1098-1107, 1999.
- [7] M. Calais, J. B. Lawrence, V. G. Agelidis, "Analysis of Multicarrier PWM Methods for a Single Phase Five Level Inverter", Proc. of IEEE 32nd Annual Power Electronics Specialist Conference, pp. 1351-1356, 2001.
- [8] B. P. McGrath, D. G. Holmes, "A Comparison of Multicarrier PWM Strategies for Cascaded and Neutral Point Clamped Multilevel Inverters", Proc. of IEEE 31st Annual Power Electronics Specialist Conference, pp. 674-679, 2000.
- [9] Mohan, Undeland and Robbins, "Power Electronics : Converters, Applications and Design", 2nd Edition, John Wiley and Sons Inc., 1995.
- [10] K. Corzine and Y. Familiant, "A New Cascaded Multilevel H-Bridge Drive." *IEEE Transactions on Power Electronics*, Vol. 17, No. 1, pp. 125-131, 2002.
- [11] B. P. McGrath and D. G. Holmes, "Multicarrier PWM Strategies for Multilevel Inverters." *IEEE Transactions on Industrial Electronics*, Vol. 49, No. 4, pp. 858-867, 2002.
- [12] J. Lai and F. Z. Peng, "Multilevel Converters – A New Breed of Power Converters." *IEEE Transactions on Industry Applications*, Vol. 32, No. 3, pp. 509-517, 1996.
- [13] N. A. Azli and A. H. M. Yatim, "Modular Structured Multilevel Inverter (MSMI) for High Power AC Power Supply Applications", Proc. of IEEE International Symposium on Industrial Electronics, pp. 728-733, 2001.
- [14] P. M. Bhagwat and V. R. Stefanovic, "Generalized Structure of a Multilevel PWM Inverter." *IEEE Transactions on Industry Applications*, Vol. 19, No 6, pp. 1057-1069, Nov/Dec 1983
- [15] A. Nabae, A., Takahashi, I. and H. Akagi, "A Neutral Point Clamped PWM Inverter." *IEEE Transactions on Industry Applications*, Vol. 17, No. 5, pp. 518-523, 1981