Applying Coupled Inductor to Step-Up Converter Combining KY and Buck-Boost Converters

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***Abstract*— In this paper, a novel voltage-boosting converter is presented, which combines one charge pump and one coupled inductor. The corresponding voltage gain is greater than that of the existing step-up converter combing KY and buck-boost converters. Since the proposed converter possesses one output inductor, the output current is non-pulsating. As a result, both the output current ripple and the output voltage ripple can be reduced significantly. After some mathematical deductions, an experimental set-up with 12V input voltage, 72V output voltage, and 60W output power is used to verify the effectiveness of the proposed converter.**

I. INTRODUCTION

Because of the global warming, the demand of the green power has been increasing for decades. These kinds of green power facilities include solar cells, fuel cells, etc. In many applications, high voltage conversion converters play an important role in boosting the low output voltages of green power facilities to the high voltages which the loads need. Regarding the traditional non-isolated voltage-boosting converters [1], such as the traditional boost converter and buck-boost converter, their voltage gains are quite low. Up to now, many kinds of voltage-boosting techniques have been presented, including several inductors which are magnetized and then pumps the stored energy into the output with all inductors connected in series [2], [3], coupled inductors with turns ratios [4]-[9], voltage superposition based on switching capacitors [10], auxiliary transformers with turns ratios [11], [12], etc. In [3], [9], the output terminal is floating, thereby increasing in application complexity. In [2], [4]-[10], these converters contain too many components, thereby making the converters too complex. In [1]-[12], the output currents are pulsating, therefore causing the output voltage ripples to be large.

Based on the mentioned above, a novel step-up converter is presented. This converter combines one KY converter [13], one traditional synchronously rectified (SR) buck-boost converter, and one coupled inductor with turns ratio, which is used to improve the voltage gain. Therefore, the voltage gain is higher than that of the converter in [14]. In addition, the proposed step-up converter has one output inductor, so the output current and output voltage ripples are quite small. Furthermore, part of the leakage inductance energy can be recycled to the output capacitor of the SR buck-boost converter. In this paper, a detailed description along with some experimental results is given to provide the effectiveness of the proposed converter.

II. OVERALL SYSTEM CONFIGURATION

Fig. 1 shows the proposed converter, which contains two MOSFET switches S_1 and S_2, one coupled inductor composed of the primary winding with N_p turns and the secondary winding with N_s turns, one energy-transferring capacitor C_1, one charge pump capacitor C_2, one diode D_1, one output inductor L_o, one output capacitor C_o, and one output resistor R_o.

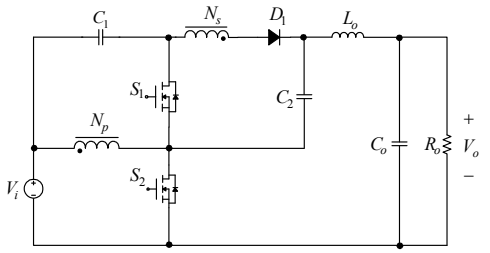

Figure 1. Proposed step-up converter.

III. BASIC OPERATING PRINCIPLES

For analysis convenience, there are some assumptions made as follows.

(1) The coupled inductor is modeled as an ideal transformer except that one magnetizing inductor L_m is connected in parallel with the primary winding.

(2) The proposed converter is always operated in the positive current mode, which means that the currents

flowing through the magnetizing inductor L_m and the output inductor L_o are always positive.

(3) The blanking times between the two MOSFET switches are omitted.

(4) The MOSFET switches and diodes are viewed as ideal components.

(5) The values of all the capacitors are large enough so that the voltages across themselves are kept constant at some values.

The following analysis contains the explanation of the power flow paths for each state, along with the corresponding equations and voltage gain. There are two operating states in the proposed converter, and the gate driving signals v_{gs1} and v_{gs2} of the two switches S_1 and S_2 are of the duty cycles of $(1-D)$ and D, respectively, where D is the dc quiescent duty cycle created from the proportional-integral (PI) controller. It is noted that this converter always operates in the continuous conduction mode (CCM). Furthermore, the key waveforms are shown in Fig. 2.

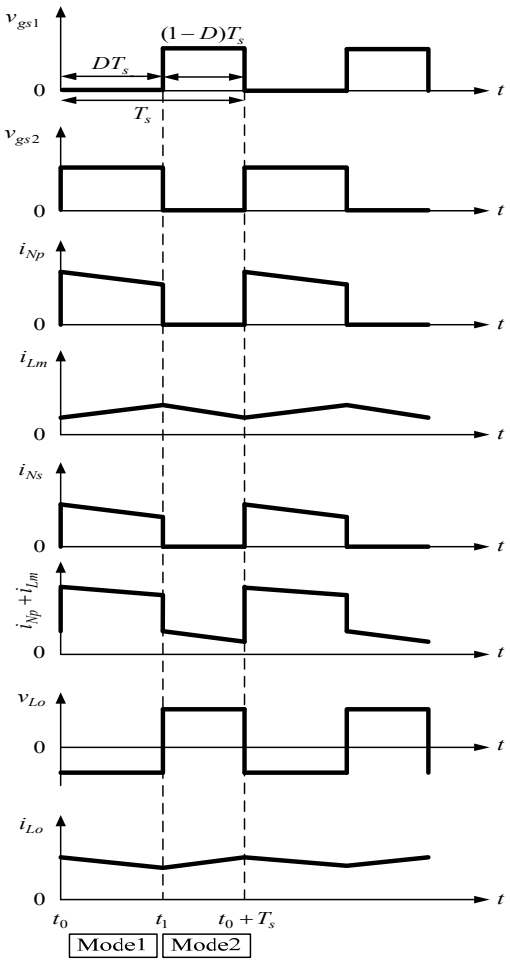

Figure 2. Key waveforms of the proposed converter.

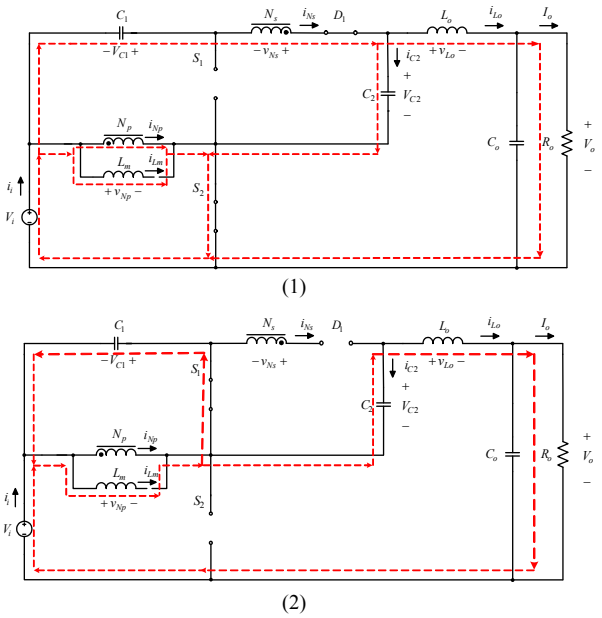

Figure 3. Power flows: (1) upper for mode 1; (2) lower for mode 2.

A. *Mode 1* $[t_0 \le t \le t_1]$

During this interval, as shown in the upper of Fig. 3, S_1 is turned off, but S_2 is turned on. Therefore, the input voltage V_i is imposed on the primary winding N_p, thereby causing the magnetizing inductor L_m to be magnetized and the voltage across the secondary winding N_s to be induced, equal to $V_i \times N_s / N_p$. In the meantime, D_1 becomes forward-biased, the voltage across C_2 is charged to $V_i + V_{C1} + V_i \times N_s / N_p$, and the voltage across L_o is a negative value, equal to $V_{C2} - V_o$, thus making L_o demagnetized. Hence, the input voltage V_i, together with the voltage V_{C1} plus the secondary-side induced voltage v_{Ns} plus the energy stored in L_o, provides energy to the load. The corresponding equations are shown below:

$$v_{Np} = V_i \tag{1}$$

$$v_{Lo} = V_{C2} - V_o \tag{2}$$

B. *Mode 2* $[t_1 \le t \le t_0 + T_s]$

During this interval, as shown in the lower of Fig. 3, S_1 is turned on, but S_2 is turned off. Therefore, the voltage $-V_{C1}$ is imposed on the primary winding N_p, thereby causing the magnetizing inductor L_m to be demagnetized, and the voltage across the secondary winding N_s to be induced, equal to $-V_{C1} \times N_s / N_p$. In the meantime, D_1 becomes reverse-biased, the voltage across L_o is a positive value, equal to $V_i + V_{C1} + V_{C2} - V_o$, thus causing L_o to be magnetized. Hence, the input voltage V_i, together with the energy stored in the

magnetizing inductor plus the voltage V_{C2}, provides energy to the load. The corresponding equations are shown below:

$$v_{Np} = -V_{C1} \tag{3}$$

$$v_{Lo} = V_i + V_{C1} + V_{C2} - V_o \tag{4}$$

By applying the voltage-second balance principle to the magnetizing inductor L_m over one switching period, the following equation can be obtained:

$$V_i \times D + (-V_{C1}) \times (1 - D) = 0 \tag{5}$$

By rearranging the above equation, the voltage across C_2 can be obtained as follows:

$$V_{C1} = \frac{D}{1-D} \times V_i \tag{6}$$

Likewise, by applying the voltage-second balance principle to the output inductor L_o over one switching period, the following equation can be obtained:

$$(V_{C2} - V_o) \times D + (V_i + V_{C1} + V_{C2} - V_o) \times (1 - D) = 0 \tag{7}$$

The capacitor voltage across C_2 can be represented by

$$V_{C2} = V_i + V_{C1} + V_i \times \frac{N_s}{N_p} \tag{8}$$

Next, based on (6), (7) and (8) the corresponding voltage gain can be expressed to be

$$\frac{V_o}{V_i} = \frac{2-D}{1-D} + \frac{N_s}{N_p} \tag{9}$$

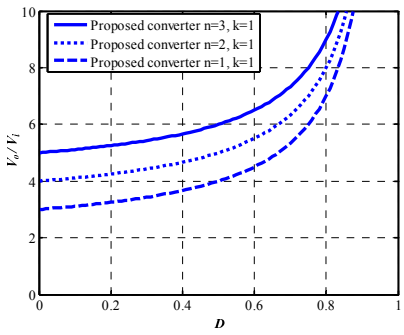

Figure 4. Curves of voltage gain versus duty cycle for the proposed converter with different values of turns ratio *n* but the same coupling coefficient *k*.

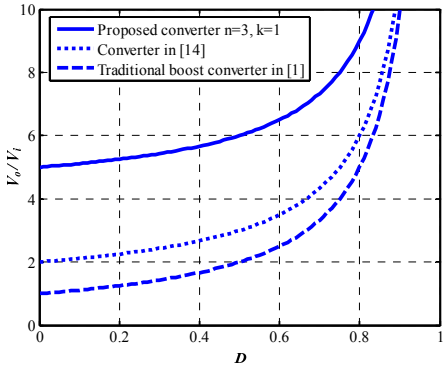

Figure 5. Comparison of voltage gain versus duty cycle for three converters.

Fig. 4 depicts the voltage gain of the proposed converter versus duty cycle, considering different turns ratios but the same coupling coefficient set to one. Fig. 5 illustrates the voltage gain of the proposed converter versus duty cycle of the proposed converter without negative output inductor current and negative magnetizing inductor current, as compared with the traditional boost converter in [1] and the converter in [14].

IV. Control Method Applied With Parameters Considerations

Fig. 6 shows the overall system block diagram. First of all, the voltage divider transfers the output voltage to a desired lower value, which is fed to the analog-to-digital converter (ADC) to create a corresponding digital signal. After this, this digital signal is sent to the filed programmable gate array (FPGA), which is the control kernel, containing a serial peripheral interface, a proportional-integral (PI) controller, and a digital pulse-width modulation (DPWM) generator. Eventually, the FPGA processes this digital signal, and accordingly produces two gate driving signals to drive the MOSFET switches. The system specifications and used component names of the proposed converter are shown in Tables I and II, respectively.

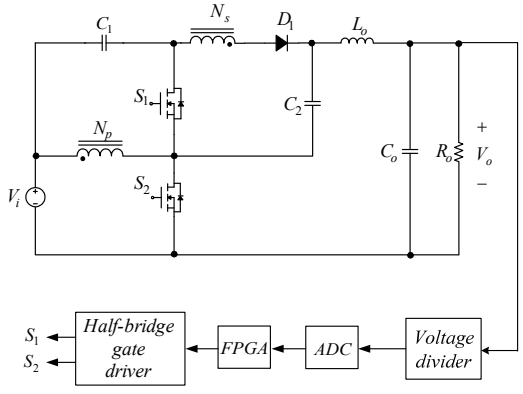

Figure 6. Proposed overall system block diagram.

TABLE I SYSTEM SPECIFICATIONS OF THE PROPOSED CONVERTER

System parameters	Specifications
Rated DC input voltage (V_i)	12V
Rated DC output voltage (V_o)	72V
Rated output current ($I_{o,rated}$)/power ($P_{o,rated}$)	0.833A/60W
Minimum output current ($I_{o,min}$)/power ($P_{o,min}$)	0.1A/7.2W
Switching frequency (f_s)	100kHz

TABLE II COMPONENTS USED IN THE PROPOSED CONVERTER

Components	Specifications
MOSFETs S_1, S_2	STP120NF, V_{DS}=100V, I_D=120A, R_{on}=10.5mΩ
Diode D_1	V20120C, V_{rms}=120V, $I_{F(AV)}$=20A, V_F=0.54V @ I_F=5A
Energy-transferring capacitor C_1	Two 680μF/50V Rubycon capacitors with positive terminals connected in series
Charge pump capacitor C_2	Two 470μF/100V MIEC capacitors connected in parallel
Output capacitor C_o	Two 470μF/100V MIEC capacitors connected in parallel
Coupled inductor	Core: PTS40/27/I 3C92, N_p:N_s=1:3, L_m=148.7μH, L_{l1}=0.3μH, k≒0.997
Output inductor L_o	188μH
FPGA	EP1C3T100
Half-bridge gate driver	IR2011
ADC	ADC7476

V. EXPERIMENTAL RESULTS

Figs. 7 to 9 show the waveforms at rated load, namely, I_o=0.833A. Fig. 7 shows the gate driving signal for S_1, v_{gs1}, the gate driving signal for S_2, v_{gs2}, the current passing through the primary side of the coupled inductor, i_{Np}+i_{Lm}, and the current passing through the secondary side of the coupled inductor, i_{Ns}. Fig. 8 shows the gate driving signal for S_1, v_{gs1}, the gate driving signal for S_2, v_{gs2}, the voltage across the output inductor L_o, v_{Lo} , and the current in the output inductor, i_{Lo}. Fig. 9 shows the gate driving signal for S_1, v_{gs1}, the gate driving signal for S_2, v_{gs2}, the voltage across C_1, V_{C1}, and the voltage across C_2, V_{C2}. From the waveforms mentioned above, the proposed converter can stably operate. Fig. 10 shows the curve of efficiency versus load current. From Fig. 10, it can be seen that the efficiency all over the load range is above 88%, and the maximum efficiency can be up to 95%.

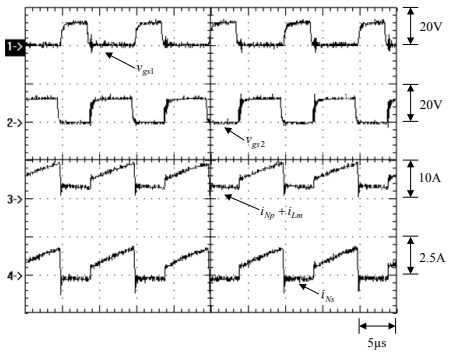

Figure 7. Waveforms at rated load: (1) v_{gs1}; (2) v_{gs2}; (3) i_{Np}+i_{Lm}; (4) i_{Ns}.

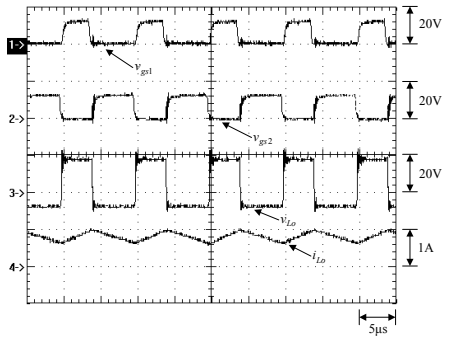

Figure 8. Waveforms at rated load: (1) v_{gs1}; (2) v_{gs2}; (3) v_{Lo}; (4) i_{Lo}.

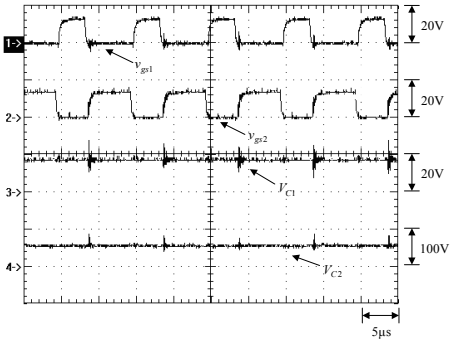

Figure 9. Waveforms at rated load: (1) v_{gs1}; (2) v_{gs2}; (3) V_{C1}; (4)V_{C2}.

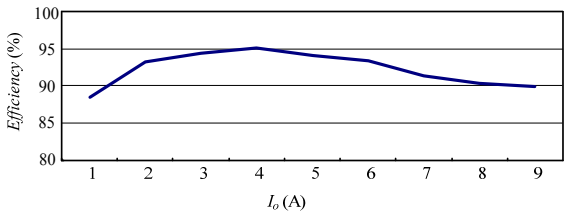

Figure 10. Efficiency versus load current.

VI. CONCLUSION

A novel high step-up converter is presented in this paper, which combining the coupled inductor with turns ratio and the switched capacitor makes the voltage gain higher than the step-up converter combining KY and buck-boost converters. Furthermore, the proposed converter has an output inductor, so the output current is non-pulsating, and hence the output voltage ripple is relatively small. Moreover, the structure of the proposed converter is quite simple and is very suitable for industrial applications.

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