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Topology and Modulation Scheme for Three-Phase Three-Level Modified Z-Source Neutral-Point-Clamped Inverter

Anh-Vu Ho and Tae-Won Chun, *Member*, *IEEE*

***Abstract*—This paper presents the topology and modulation technique of a three-phase three-level modified Z-source neutral-point-clamped (MZS-NPC) inverter, which combines a modified Z-source impedance network and a three-phase three-level NPC inverter. The boost factor of the proposed MZS-NPC inverter is twice as high as the three existing representative topologies combing an impedance network with a three-level NPC inverter. A modulation scheme for the proposed topology, based on a maximum boost control method, is designed to achieve the maximum voltage gain with simple implementation and to balance the dc-link neutral-point voltage. A closed loop control of the ac load voltage in the fuel-cell or photovoltaic applications based on the proposed inverter is realized, in order to supply a desired voltage to the critical load in islanding mode of a microgrid. The boosting ability and operation validity of the proposed topology and modulation technique are demonstrated with simulation and experimental results.**

***Index Terms*—Boost ability, modified Z-source impedance, modulation technique, neutral-point-clamped inverter.**

I. Introduction

NOWADAYS, multilevel inverters are an attractive choice for high-voltage and high-power applications because they can generate a smoother stepped output waveform of more than two voltage levels with a lower total harmonic distortion (THD). They can also reduce the voltage stress of inverter switching devices [1], [2]. There are three general topologies of multilevel inverters: neutral-point-clamped (NPC), cascaded H-bride (CHB), and flying capacitor (FC) inverters [3]. These multilevel inverters are applied to many applications, including photovoltaic (PV) generation systems and uninterruptible power supplies [4], [5]. However, the traditional multilevel inverter provides a buck operation. The peak ac output voltage of an NPC inverter cannot be higher than the dc input voltage. Although the total ac output voltage of a CHB inverter can be obtained by summing the output voltage of each individual H-bridge circuit, the peak ac output voltage of a CHB inverter is lower than the total dc source voltage. An additional dc-boost converter, used to raise the dc-link voltage of the multilevel inverter, is needed to achieve the desired ac output voltage [5], [6]. This extra dc-boost converter results in a higher cost and a lower efficiency of the power converter.

Topologies that have been proposed to solve the drawbacks of traditional multilevel inverters are the Z-source inverter (ZSI) or quasi-Z-source inverter (qZSI), which achieve buck-boost voltage operation with a single-stage power conversion [7]-[9]. The ZSI/qZSI can raise the dc-link voltage by applying the shoot-through state. Thus, they can reduce the power conversion stage and improve the reliability. Several techniques that combine the (quasi-)Z-source impedance network with multilevel inverters have been developed in order to integrate the merits of (q-)ZSI and multilevel inverters.

The comparison analysis of the two- and multi-level buck-boost inverters based on the impedance source networks is provide in [10], and the comparison is presented for the three-level NPC inverter with dc-dc boost converter and the three-level NPC-qZSI [11]. The three-phase three-level Z-source NPC inverter is designed by connecting a single Z-source impedance network between a split dc source and a three-level NPC inverter; this is done to minimize the component count [12], [13]. This design can reduce one Z-source impedance network and one dc source, but its boost gain is the same as the traditional ZSI. The modulation techniques of the three-level NPC inverter with a single Z-source impedance network are described by using carrier-based approaches to achieve the minimum number of device commutations per half-cycle of the carrier signal [14]-[16] and to balance the neutral-point voltage of the NPC inverter [17]. Controlling the Z-source NPC inverter via the space voltage modulation approach is suggested in order to yield better harmonics performance in the output voltage [18]. The fault-tolerant strategy under the switch fault condition and the adaptive closed loop control used to obtain the desired dynamic performances of the three-level Z-source NPC inverter are evaluated in [19] and [20], respectively. The operational analysis and modulation techniques of a five-level Z-source NPC inverter, designed with two Z-source impedance networks linked between two separate dc sources and the five-level NPC inverter are discussed [21].

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Anh-Vu Ho is with the School of Engineering, Eastern International University, Binh Duong, Vietnam (e-mail: vuanhhovn@yahoo.com.vn).

Tae-Won Chun is with the Department of Electrical Engineering, University of Ulsan, Ulsan, 44610, Korea (e-mail: twchun@mail.ulsan.ac.kr).

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Similar to the three-level ZS-NPC inverter, the control methods and modulation schemes for a three-level NPC-qZSI are introduced in [22]-[24], where two symmetrical quasi-Z-source networks with a split dc source are connected to a three-level NPC structure. This can provide a continuous dc source current and boost the multilevel output voltage. However, the boost factors of the three-level NPC-qZSI and the three-level NPC-ZSI are the same as traditional ZSI/qZSI, despite the fact that the three-level NPC-qZSI has two symmetrical quasi-Z-source networks. A three-level NPC-qZSI topology proposed in [25] can reduce the capacitor voltage stress. However, it requires two more capacitors, compared with an existing NPC-qZSI.

A quasi-Z-source cascaded multilevel inverter (qZS-CMI), which can be implemented by cascading the qZS H-bridge inverter module fed by the PV array, was applied to PV power systems [26]-[30]. These works use the control method to balance the dc-link peak voltage of all modules, the distributed maximum power point tracking method, modulation techniques, and parameter design of passive components of the qZS-CMI. These designs provide a continuous dc source current and easily increase the number of ac output voltage levels by cascading more modules per phase. However, many qZS H-bridge inverter modules are required because a separate module is connected to each PV panel.

The three-level LC-switching-based boost NPC inverter proposed in [31] and [32] utilizes fewer passive components with a single split dc source. However, this setup requires two extra switching devices and its boost ability is limited to that of a classic ZSI/qZSI. Transformer-based Z-source NPC inverters, where the inductors in the Z-source impedance network are replaced with coupled transformers, are presented in [33]. The desired voltage gain can be obtained by designing the turn ratio of a transformer; however, two coupled transformers and two separate dc sources are needed. A family of the three-level three-phase NPC inverter based on the inductor-capacitor-capacitor-transformer (LCCT) networks is described and compared [34].

This paper proposes a novel three-phase three-level modified Z-source neutral-point-clamped (MZS-NPC) inverter designed by integrating a modified Z-source impedance network, which was applied to a cascaded hybrid five-level inverter [35], with a the three-level NPC inverter. The proposed MZS-NPC inverter can raise the boost factor and produce a boosted five-level output voltage. A modified modulation technique based on the maximum boost control strategy is proposed to achieve the maximum voltage gain and allow for simple implementation. It can balance the dc-link neutral-point voltage for achieving the zero average neutral-point current condition. The performances of the proposed topology and modulation technique are confirmed based on the simulation and experimental results.

II. Introduction of Single-Stage Buck-Boost Three-Level NPC Inverters

Three representative topologies that combine an impedance network with a three-level NPC inverter are introduced in Fig. 1.

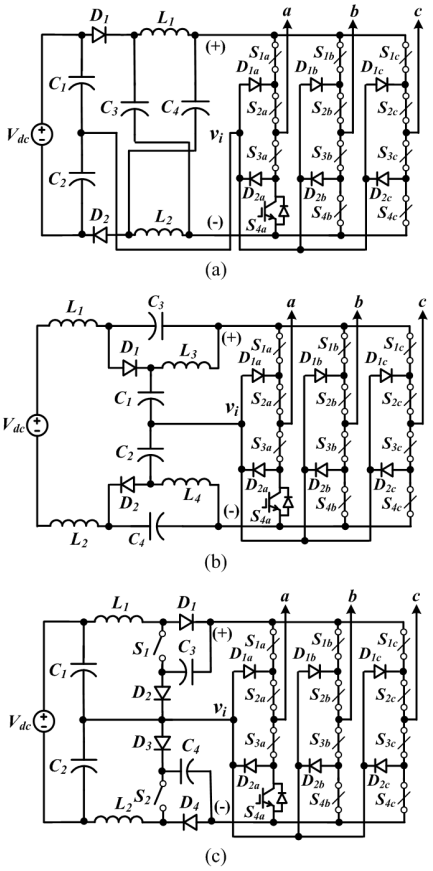

Fig. 1. Single-stage buck-boost three-level NPC inverters: (a) NPC-ZSI, (b) NPC-qZSI, (c) LC-switching boost NPC inverter.

Fig. 1(a) shows a three-level Z-source NPC inverter (NPC-ZSI) with a single Z-source impedance network, which reduces the number of passive components [12]-[20]. Two split dc sources can be produced by feeding a dc source parallel to two series capacitors. Fig. 1(b) shows a three-level NPC-qZSI that combine two symmetrical qZS networks with a three-level NPC inverter [22]-[24], and Fig. 1(c) shows a three-level LC-switching-based voltage boost NPC inverter that implements two symmetrical LC switching networks between two split dc sources and a three-level NPC inverter, as proposed in [31].

The boost factors B, defined as the ratio of the peak dc-link voltage of the inverter $\hat{v}_i$ to the dc input voltage V_{dc}, of the three-level NPC-ZSI/qZSI and the LC-switching-based voltage boost NPC inverter are the same as

$$B = \frac{\hat{v}_i}{V_{dc}} = \frac{1}{1-2(T_{ST}/T)} = \frac{1}{1-2D} \tag{1}$$

where T_{ST} is the shoot-through time during one switching interval T, and the shoot-through duty ratio D is defined as (T_{ST} / T). This boost factor is identical with the boost factor of a classic ZSI.

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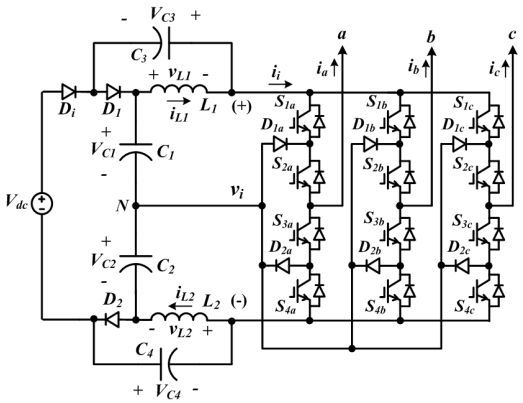

Fig. 2. Three-phase three-level modified Z-source impedance NPC inverter.

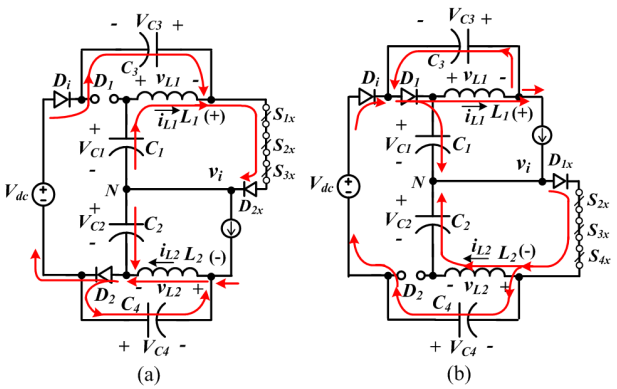

Fig. 3. Equivalent circuits of the three-level MZS-NPC inverter in the shoot-through state: (a) upper shoot-through state, (b) lower shoot-through state.

III. Operation of Three-Phase Three-Level Modified Z-Source NPC Inverter

Fig. 2 shows the topology of a three-phase three-level MZS-NPC inverter where the MZS can be implemented by removing two inductors from the symmetrical quasi-Z-source impedance networks in the three-level NPC-qZSI and attaching a diode between the dc source and the upper impedance network cell [35]. The MZS, which consists of two inductors, four capacitors, and three diodes, is linked to a three-level NPC inverter.

The proposed three-phase three-level MZS-NPC inverter has two operation modes, similar to a traditional ZSI: the non-shoot-through state and the shoot-through state. The equivalent circuits for both operation modes are utilized in order to obtain the mathematical model of the proposed topology. The operation of one phase leg of the proposed topology is described. By assuming $L_1 = L_2$, $C_1 = C_2$, and $C_3 = C_4$, we can assume $V_{L1} = V_{L2}$, $V_{C1} = V_{C2}$, and $V_{C3} = V_{C4}$ due to the symmetrical structure of the modified impedance network.

A. Shoot-Through State

There are three types of shoot-through state modes available for the three-level MZS-NPC inverters: a full shoot-through state, an upper shoot-through state (UST), and a lower shoot-through state (LST). The full shoot-through state, which causes a short circuit across the full dc-link by turning on all of the switches in any phase leg, results in zero output voltage. Alternatively, both the upper and lower shoot-through states provide an ac output voltage with enhanced waveform quality, and reduce the amount of switching. Both the upper and lower shoot-through states can be operated with the proposed topology due to the common neutral point N at the midpoint between the two series capacitors. In the upper shoot-through state during the time interval of T_{UST}, the switches S_{1x}, S_{2x}, and S_{3x} ($x = a$, b, or c) are switched on, and the diodes D_i, D_2, and D_{2x} are on, whereas diode D_1 is off, as shown in Fig. 3(a). The two inductor voltages and dc-link voltage are given by

$$v_{L1} = V_{C1} = V_{C1} + V_{C2} - V_{dc} - V_{C3}\ ,\ v_{L2} = -V_{C4} \tag{2}$$

$$v_i = V_{C2} + V_{C4}\,. \tag{3}$$

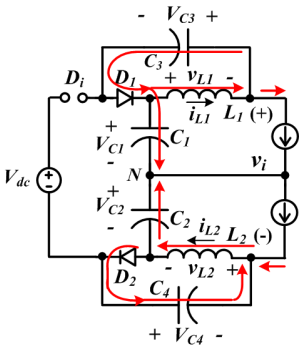

Fig. 4. Equivalent circuits of the three-level MZS-NPC inverter in the non-shoot-through state.

TABLE I
Switching States of Three-Level MZS-NPC Inverter ($x = a$, b, or c)

State type	ON switches	ON diodes	V_{XN}	Switching state
NST	S_{1x}, S_{2x}	D_1, D_2, D_{1x}, D_{2x}	$+ V_i/2$	P
NST	S_{3x}, S_{4x}	D_1, D_2, D_{1x}, D_{2x}	$- V_i/2$	N
NST	S_{2x}, S_{3x}	D_1, D_2, D_{1x}, D_{2x}	0	O
UST	S_{1x}, S_{2x}, S_{3x}	D_i, D_2, D_{2x}	0	UST
LST	S_{2x}, S_{3x}, S_{4x}	D_i, D_1, D_{1x}	0	LST

In the lower shoot-through state during the time interval of T_{LST}, the switching devices S_{2x}, S_{3x}, and S_{4x} are switched on and the diodes D_i, D_1, and D_{1x} are on, whereas diode D_2 is off, as shown in Fig. 3(b). The two inductor voltages and dc-link voltage are given by

$$v_{L1} = -V_{C3}\ ,\ v_{L2} = V_{C2} = V_{C1} + V_{C2} - V_{dc} - V_{C4} \tag{4}$$

$$v_i = V_{C1} + V_{C3}\,. \tag{5}$$

B. Non-Shoot-Through State

In the non-shoot-through state during the time interval of T_{NST}, diodes D_1 and D_2 are in the conduction state whereas

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diode D_i is off. The MZS-NPC inverter is operated as a traditional three-level NPC inverter. Fig. 4 shows the equivalent circuits of the three active states and zero state, where the inverter and ac load are represented by a current source. The two inductor voltages and the dc-link voltage v_i in the non-shoot-through state are given by

$$v_{L1} = -V_{C3}\ ,\ v_{L2} = -V_{C4} \tag{6}$$

$$v_i = V_{C1} + V_{C2} + V_{C3} + V_{C4} = \hat{v}_i\ . \tag{7}$$

Each phase leg has three possible voltages (i.e., $+V_i/2$, $-V_i/2$, and 0 V), which are controlled by the switches of each phase leg. The operation of each phase leg of a proposed topology in the non-shoot-through state is described by three switching states P, N, and O [18]. Table I describes the output phase leg voltage V_{xN} (x = a, b, or c) and the conducting switches according to the switching states of the three-level MZS-NPC inverter.

C. Boost Factor

The average values of T_{UST} and T_{LST} are identical over one-third period of the inverter frequency due to symmetrical operation of the upper and lower shoot-through states. Therefore, the upper and lower shoot-through states can be represented by $T_{UST} = T_{LST} = T_{ST}$. Based on the principle that the average voltage of inductor L_1 obtained from (2), (4), and (6) over switching cycle T is zero, and by using $V_{C1} = V_{C2}$ and $V_{C3} = V_{C4}$, the capacitor voltages can be derived as

$$V_{C1} = V_{C2} = \frac{1-D}{1-2D} V_{dc} \tag{8}$$

$$V_{C3} = V_{C4} = \frac{D}{1-2D} V_i\ . \tag{9}$$

By substituting (8) and (9) into (7), the boost factor B can be expressed as

$$B = \frac{\hat{v}_i}{V_{dc}} = \frac{2}{1-2D}\ . \tag{10}$$

IV. Modified Modulation Techniques and Load Voltage Control

A. Operations of Modified Modulation Technique for a Three-Level MZS-NPC Inverter

Fig. 5 shows a modified modulation technique based on an alternative phase opposition disposition (APOD) technique [16]. This modified APOD technique contains two triangular carriers with a 180° phase shift: V_{Tr1} and V_{Tr2}. The overall dc-ac voltage gain G is defined as

$$G = \frac{\hat{v}_o}{(V_{dc}/2)} = M \cdot B \tag{11}$$

where $\hat{v}_o$ and M are the peak output phase voltage and the modulation index, respectively. The relationship between M and B is dependent on modulation techniques. This paper adapts a maximum boost control method for the proposed topology to achieve the maximum voltage gain [37]. The maximum boost control strategy converts all zero states into a shoot-through state while leaving the active states unchanged. Also, a third harmonic voltage is injected into the three-phase sinusoidal reference voltages in order to increase the range of M from 1 to $(2/\sqrt{3})$.

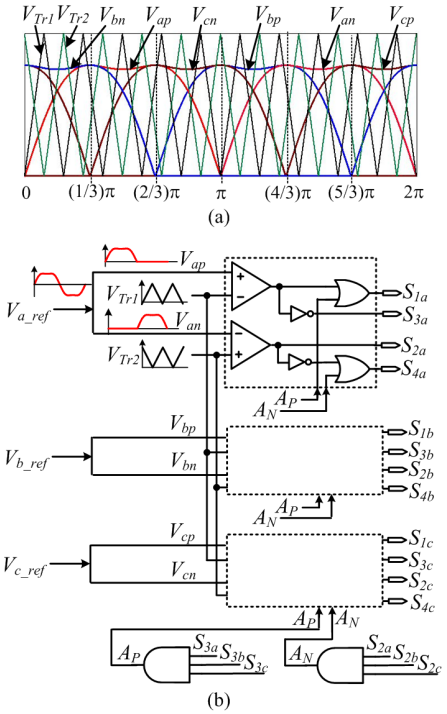

Fig. 5. Modified modulation strategy for the three-level MZS-NPC inverter: (a) three-phase modulation signals and carriers, (b) modulation logic circuit.

By using a three-phase reference voltage with a third harmonic component V_{x_ref} with x = a, b, or c, both the positive and negative three-phase modulation signals V_{xp} and V_{xn} with x = a, b, or c are expressed as

$$V_{xp} = \frac{1}{2}((abs(V_{x\_ref}) + V_{x\_ref}) \tag{12}$$

$$V_{xn} = \frac{1}{2}((abs(V_{x\_ref}) - V_{x\_ref}) \tag{13}$$

where x = a, b, c are shifted 120° from each other. The positive and negative three-phase modulation signals and two carriers are shown in Fig. 5(a).

Fig. 5(b) shows the logic circuit of the modified modulation strategy for the proposed topology. The positive and negative three-phase modulation signals can be obtained from the three-phase reference voltage. The PWM signals S_{1x}/S_{3x} are generated by comparing the positive modulation signal V_{xp} and a carrier signal V_{Tr1}. When the positive modulation signal is greater than the carrier signal V_{Tr1}, the switch S_{1x} is switched on. The signals S_{2x}/S_{4x} are generated by comparing the negative modulation signal V_{xn} and a carrier signal V_{Tr2}. When the

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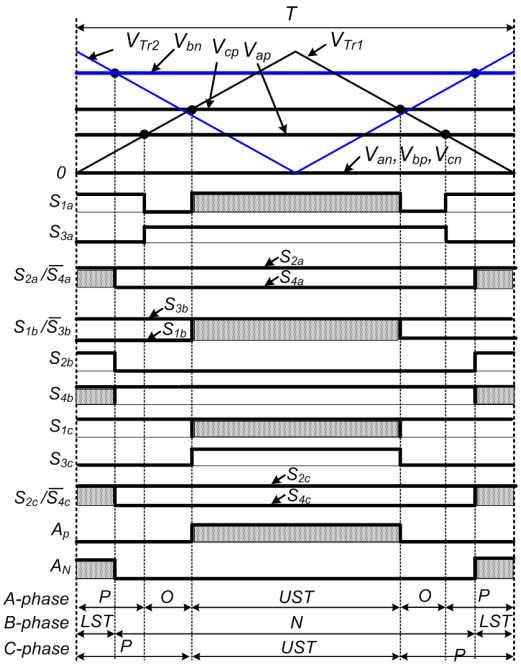
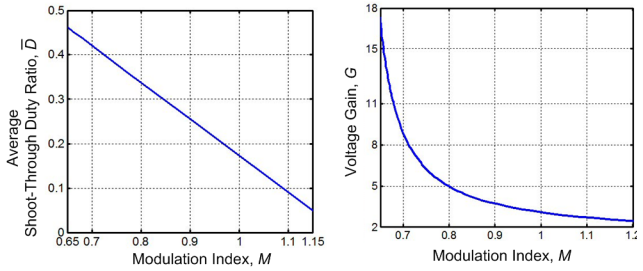


Fig. 6. Switching pattern of three-phase PWM signals at $0 \le \omega t < (6/\pi)$.



(a) (b)

Fig. 7. Plots of both the average shoot-through duty ratio and ac voltage gain with a variation of M: (a) plot of $\overline{D}$ (b) plot of G.

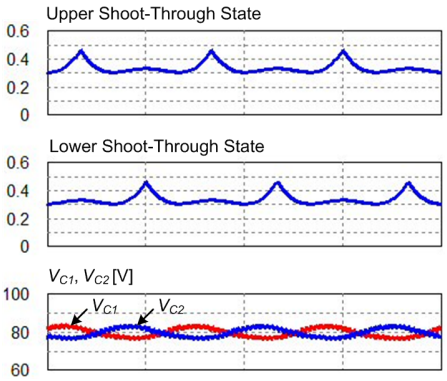


Fig. 8. Upper and lower shoot-through states and two series capacitor voltages.

negative modulation signal is greater than the carrier signal V_{Tr2}, the switch S_{2x} is switched on. The switches S_{3x} and S_{4x} are switched complementarily to S_{1x} and S_{2x}, respectively. The upper and lower shoot-through states can be produced by using two signals A_p and A_n, respectively.

All zero states are converted into the upper or lower shoot-through states to achieve the maximum voltage gain. The upper shoot-through state is generated when *max* (V_{ap}, V_{bp}, V_{cp}) $\ge V_{Tr1}$, and the lower shoot-through state is generated when *max* (V_{an}, V_{bn}, V_{cn}) $\ge V_{Tr2}$. Therefore, the upper shoot-through state is inserted by using the signal A_p when switches S_{3a}, S_{3b}, and S_{3c} are all on, and the lower shoot-through state is inserted by using the signal A_n when switches S_{2a}, S_{2b}, and S_{2c} are all on, as shown in Fig. 5(b).

Fig. 6 illustrates six modulation signals with two carriers, switching signals of three-phase switches, and the switching state of each phase during the period $0 \le \omega t < (\pi/6)$. As V_{cp} is the highest positive modulation signal among the three-phase positive modulation signals, the upper shoot-through state is generated by setting all S_{1x} switching signals to logic '1' in the period where the carrier V_{tri1} is higher than V_{cp}. The lower shoot-through state is generated by setting all S_{4x} switching signals to logic '1' in the period where the carrier V_{tri2} is higher than V_{bn}, which is the highest negative modulation signal.

Because the shoot-through duty ratio varies by a factor that is six times the inverter frequency, the average of the shoot-through duty ratio during $((\pi/6), (\pi/2))$ can be expressed as [37]

$$\overline{D} = 1 - \frac{3\sqrt{3}}{2\pi} M \ . \tag{14}$$

By substituting (10) and (14) into (11), the total dc-ac voltage gain G can be derived as a function of M as follows:

$$G = \frac{2}{\frac{3\sqrt{3}}{\pi} - \frac{1}{M}} \tag{15}$$

Fig. 7 shows the plots of $\overline{D}$ and G with a variation of M by using (14) and (15). It can be seen that both $\overline{D}$ and G decrease as M increases in the range from 0.65 to 1.15. When M has a maximum value by 1.15, $\overline{D}$ and G become 0.05 and 2.55, respectively. Therefore, the dc-link voltage and the peak ac output voltage can be boosted to 2.1 times and 2.55 times, respectively, at the maximum modulation index.

B. DC-Link Neutral-Point Voltage Balancing Scheme

The dc-link neutral-point voltage balancing in three-level NPC inverter can be achieved by balancing the two series capacitor voltages V_{C1} and V_{C2}. Fig. 8 shows the variations of the upper and lower shoot-through states and two series capacitor voltages V_{C1} and V_{C2} over one period of the inverter frequency. Because both shoot-through states repeat periodically over $(2/3)\pi$, they are varied at three times the inverter frequency. When the upper (or lower) shoot-through state increases, the lower (or upper) shoot-through state decreases. When the upper shoot-through state is higher than the lower shoot-through state, the capacitor voltage V_{C1} decreases whereas the capacitor voltage V_{C2} increases, as regarding Fig. 3. When the lower shoot-through state is higher

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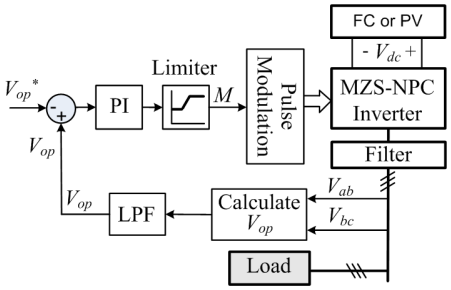

Fig. 9. Block diagram of ac load voltage controlled MZS-NPC inverter in islanding operation mode of a microgrid.

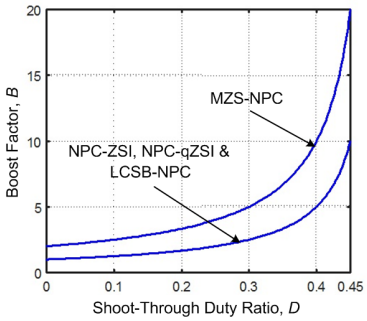

Fig. 10. Boost factor with variations in the shoot-through duty ratio.

than the upper shoot-through state, V_{C1} increases whereas V_{C2} decreases. Therefore, it can be noted that the two series capacitor voltages V_{C1} and V_{C2} are balanced while including the ripple components with three times the inverter frequency.

A modified modulation technique proposed by this paper can provide a higher voltage gain with a simple implementation, and it can achieve the zero average neutral-point current condition by balancing the two series capacitor voltages. However, it allows only the boost operation, and the capacitor voltages and inductor currents in the impedance network include the ripple components with three times the inverter frequency due to variations of the upper and lower shoot-through states.

C. AC Load Voltage Control in Islanding Operation Mode

The fuel-cell or PV applications based on the proposed MZS-NPC inverter are able to supply ac power in islanding mode of a microgrid, where the main grid is not present in the islands, rural or remote areas. The proposed inverter in islanding operation mode provides the desired voltage to the critical or local load by regulating the modulation index M, where the total dc-ac voltage gain G decrease as M increases as shown in Fig. 7(b).

The ac load voltage control of the proposed MZS-NPC inverter described in Fig. 9 is realized with a closed-loop control system to obtain a desired voltage across a critical or local load. The reference voltage V_{op}^*, which is the peak of the desired output voltage, determines on $110\sqrt{2}\,V$, in order to adjust the magnitude of the voltage across a critical load to 110 Vrms. The peak load voltage V_{op} is calculated by using two line-to-line voltages V_{ab} and V_{bc}. The polarities of the reference and peak load voltages in the voltage control loop are determined to reduce the value of M when the error between V_{op}^* and V_{op} is positive, due to the relationship between M and G shown in Fig. 7(b). The range of M is limited from 0.65 to 1.15.

TABLE II
NUMBER OF COMPONENTS USED IN THE IMPEDANCE NETWORK

Topologies	Inductors	Capacitors	Diodes	Active Switches
MZS-NPC	2	4	3	0
NPC-ZSI	2	4	2	0
NPC-qZSI	4	4	2	0
LCSB-NPC	2	4	4	2

V. COMPARISON WITH OTHER TOPOLOGIES

The performance of the proposed MZS-NPC inverter is compared with those of NPC-ZSI, NPC-qZSI, and LC-switching- voltage boost NPC (LCSB-NPC) inverter. This section describes a detailed comparison of the boost factor, the number of components used in the impedance network, and the voltage stress of components in the impedance network between the proposed MZS-NPC inverter and the other three

TABLE III
COMPARISON OF VOLTAGE STRESSES

	MZS-NPC	NPC-ZSI	NPC-qZSI	LCSB-NPC
Capacitors	$\frac{V_{C1}}{\hat{v}_o}=\frac{V_{C2}}{\hat{v}_o}=\frac{3\sqrt{3}}{2\pi}$ $\frac{V_{C3}}{\hat{v}_o}=\frac{V_{C4}}{\hat{v}_o}=\frac{1}{M}-\frac{3\sqrt{3}}{2\pi}$	$\frac{V_{C1}}{\hat{v}_o}=\frac{V_{C2}}{\hat{v}_o}=\frac{3\sqrt{3}}{\pi}-\frac{1}{M}$ $\frac{V_{C3}}{\hat{v}_o}=\frac{V_{C4}}{\hat{v}_o}=\frac{3\sqrt{3}}{\pi}$	$\frac{V_{C1}}{\hat{v}_o}=\frac{V_{C2}}{\hat{v}_o}=\frac{3\sqrt{3}}{2\pi}$ $\frac{V_{C3}}{\hat{v}_o}=\frac{V_{C4}}{\hat{v}_o}=\frac{1}{M}-\frac{3\sqrt{3}}{2\pi}$	$\frac{V_{C1}}{\hat{v}_o}=\frac{V_{C2}}{\hat{v}_o}=\frac{3\sqrt{3}}{\pi}-\frac{1}{M}$ $\frac{V_{C3}}{\hat{v}_o}=\frac{V_{C4}}{\hat{v}_o}=\frac{1}{M}$
Diodes	$\frac{V_{Di}}{\hat{v}_o}=\frac{V_{D1}}{\hat{v}_o}=\frac{V_{D2}}{\hat{v}_o}=\frac{1}{M}$	$\frac{V_{D1}}{\hat{v}_o}=\frac{V_{D2}}{\hat{v}_o}=\frac{1}{M}$	$\frac{V_{D1}}{\hat{v}_o}=\frac{V_{D2}}{\hat{v}_o}=\frac{1}{M}$	$\frac{V_{D1}}{\hat{v}_o}\cdots\frac{V_{D4}}{\hat{v}_o}=\frac{1}{M}$
Switches	-	-	-	$\frac{V_{S1}}{\hat{v}_o}=\frac{V_{S2}}{\hat{v}_o}=\frac{1}{M}$

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topologies.

A. Comparison of Boost Factor

Fig. 10 shows the plot of the boost factors of the proposed MZS-NPC inverter topology and the other three topologies with variations in the shoot-through duty ratio. It can be noted that the boost factor of the proposed MZS-NPC inverter is twice as high as the other three topologies over the entire shoot-through duty ratio range.

B. Comparison of the Number of Components

Table II shows a comparison of the number of passive components, diodes, and active switches used in the impedance networks of the proposed MZS-NPC inverter, NPC-ZSI, NPC-qZSI, and LCSB-NPC inverter.

From this table, the proposed topology requires two fewer inductors than NPC-qZSI. It also requires two fewer active switches and diodes than the LCSB-NPC inverter, although it needs one more diode compared to NPC-ZSI.

C. Comparison of Voltage Stresses

The voltage stress of the components in the impedance network varies with the dc input voltage and boost factor. To properly compare the voltage stresses of the four topologies, the ratio of voltage stress to the peak ac output voltage can represent the cost to generate a desired output voltage. Substituting (12) to (1) and (10), respectively, and using (11), the dc input voltage can be expressed as the ac output voltage and modulation index by (16) and (17), respectively.

$$V_{dc} = 2\left(\frac{3\sqrt{3}}{\pi} - \frac{1}{M}\right)\hat{v}_o \quad \text{for MZS-NPC inverter} \tag{16}$$

$$V_{dc} = \left(\frac{3\sqrt{3}}{\pi} - \frac{1}{M}\right)\hat{v}_o \quad \text{for other three topologies} \tag{17}$$

By using (15) and (16), the ratios of voltage stresses across capacitors, diodes, and switches to the peak ac output voltage of four topologies are summarized in Table III. The ratios of voltage stress across four capacitors to the peak ac output voltage of the proposed topology are identical with those of the NPC-qZSI. Two capacitors C_1 and C_2 of both the NPC-ZSI and LCSB-NPC have the lowest ratio of voltage stress, because the two capacitors C_1 and C_2 are used to produce two split dc sources. The ratios of voltage stress across diodes to the peak ac output voltage of four topologies are the same, and they are inversely proportional to the modulation index. The ratio of voltage stress across switching devices in the LCSB-NPC inverter is the same as that of the diodes.

VI. Simulation and Experimental Results

A. Simulation Results

The proposed topology is simulated using the PSIM program when the switching frequency of the inverter is 10 kHz and the dc input voltage V_{dc} is 40 V. A cut-off frequency of the LC output filter determines on 650 Hz by considering both the inverter frequency of 60 Hz and the switching frequency of 5 kHz. The circuit parameters used for the simulation and experiment are listed as follows:

- Z-source impedance network: $L_1 = L_2 = 1$ mH, $C_1 = C_2 = C_3 = C_4 = 1000$ μF
- LC output filter: $L_f = 0.6$ mH, $C_f = 100$ μF
- RL load: $R_L = 50$ Ω, $L_L = 1.2$ mH.

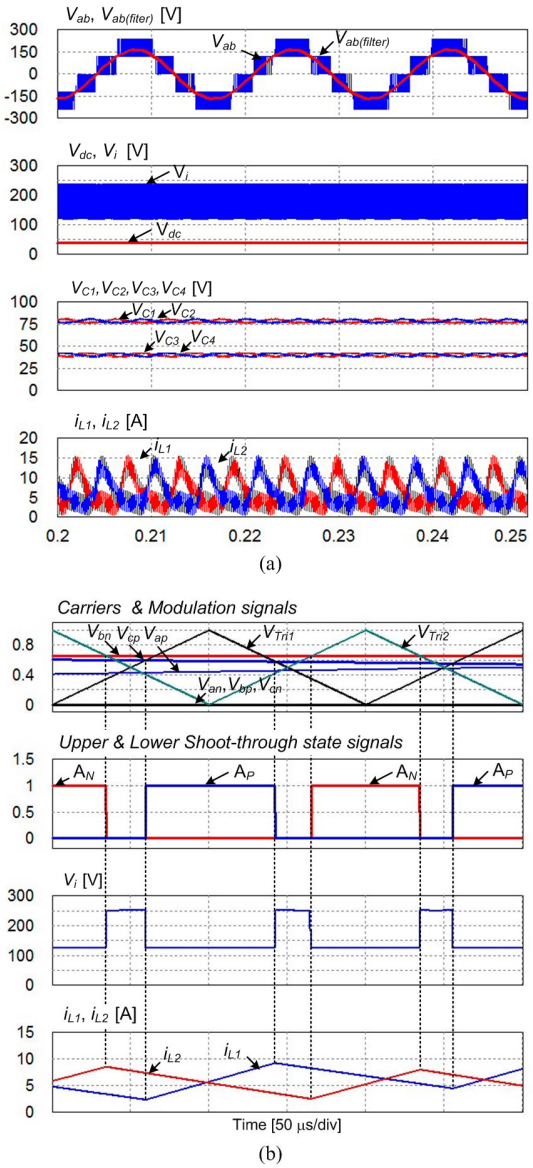

Fig. 11. Simulation results of the proposed MZS-NPC inverter when $M = 0.8$: (a) ac output voltage, dc-link and dc input voltages, capacitor voltages, and inductor currents, (b) carriers and modulation signals, dc-link voltage and inductor currents.

Fig. 11 shows the simulation results for the three-phase three-level MZS-NPC inverter at a modulation index of $M = 0.8$ while assuming that all of the passive components and devices are ideal. From Fig. 11(a), the ac output line-to-line voltage with five voltage levels can be produced, and the RMS value of the output line-to-line voltage filtered by the LC filter is about

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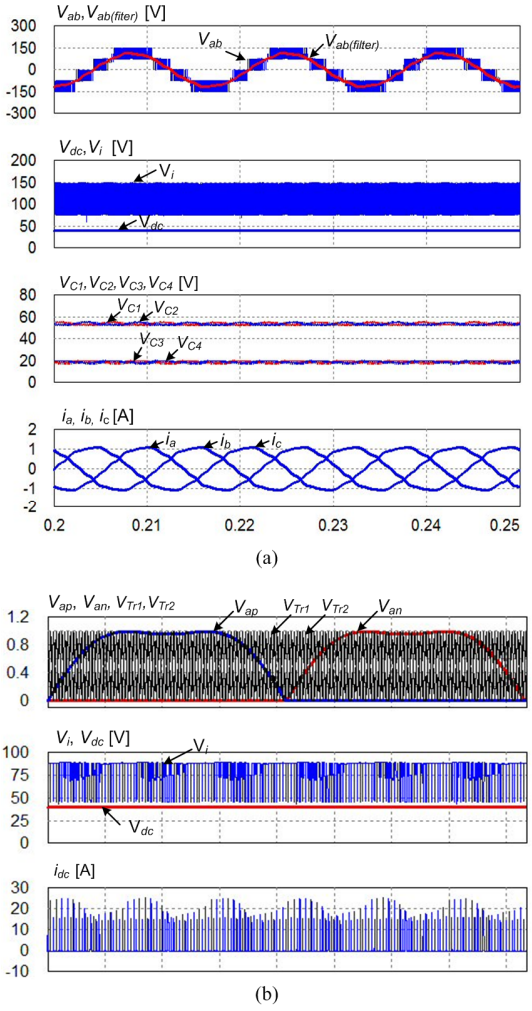

Fig. 12. Simulation results of the proposed inverter: (a) when M = 0.9, (b) when M = 1.15.

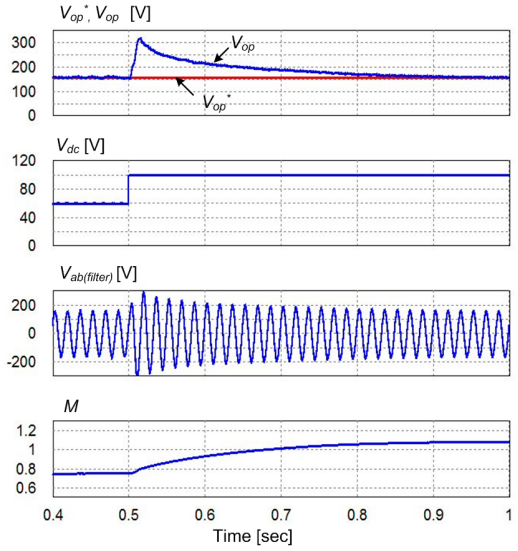

Fig. 13. Transient response of the load voltage in islanding operation mode of a microgrid.

110 V. The dc-link voltage can be boosted to 245 V, which is

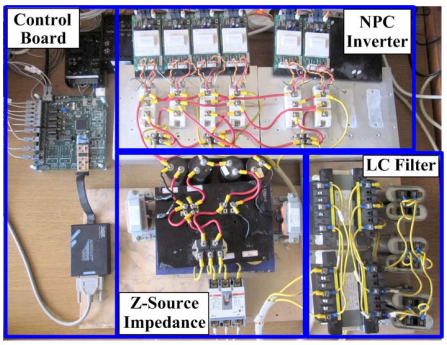

Fig. 14. Photograph of the MZS-NPC inverter prototype.

about 6.1 times that of the 40 V dc input voltage. The two series capacitor voltages V_{C1} and V_{C2} including the ripple components with 180 Hz frequency are balanced with 79 V, and the average values of the two capacitor voltages V_{C3} and V_{C4} are the same as 40 V. The simulation results shown in Fig. 11(a) are nearly identical with the theoretical analysis results. Fig. 11(b) shows the two carriers and three-phase modulation signals, upper and lower shoot-through state signals, dc-link voltage, and two inductor currents. The upper shoot-through state is generated by using the signal A_P when the carrier V_{Tr1} is higher than V_{cp} ,and the lower shoot-through state is generated by using the signal A_N when the carrier V_{Tr2} is higher than V_{bn}. The dc-link voltage is half of the peak voltage during both shoot-through states. The inductor currents i_{L1} and i_{L2} increase during the upper and lower shoot-through states, respectively.

Fig. 12(a) shows the simulation results when the modulation index M increases to 0.9 by considering the ESRs (equivalent series resistances) of both the inductors and capacitors in the Z-source impedance network and the voltage drops of devices. The RMS values of the output line-to-line voltage and the phase current are 85 V and 0.75 A, respectively, while the dc-link voltage is raised to 145 V. The dc-link voltage, output voltage and current are reduced as the shoot-through state decreases, and these values are slightly lower than those obtained by theoretical analysis. Fig. 12(b) shows a-phase modulation signals with two carriers, dc link and dc input voltages, and dc input current at M = 1.15, which is a maximum modulation index. Because the proposed inverter has the lowest shoot-through state under maximum modulation index, the dc source can supply the power during the shoot-through state and the dc-link voltage can be boosted to 85 V.

Fig. 13 shows the simulation results for the transient response of the load voltage, when the dc input voltage is changed from 60 V to 100 V in islanding operation mode. The peak load voltage is well regulated to its reference voltage $110\sqrt{2}\,V$, by increasing the modulation index M from 0.75 to 1.08 in order to reduce the dc-ac voltage gain for keeping the load voltage to 110 Vrms when the dc input voltage increases from 60 V to 100 V.

B. Experimental Results

Fig. 14 shows a photograph of the prototype of the proposed

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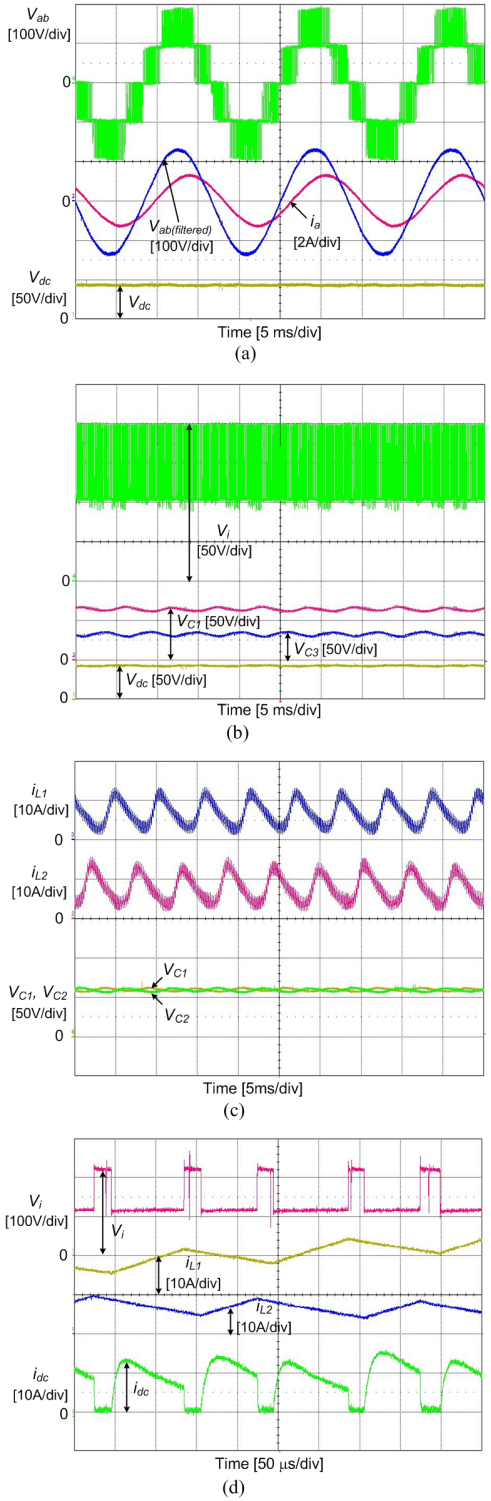

Fig. 15. Experimental results of the proposed MZS-NPC inverter when M = 0.8: (a) ac output voltage and current and dc input voltage, (b) dc-link and capacitor voltages, (c) inductor currents and two series capacitor voltages (d) dc-link voltage, inductor and dc input currents.

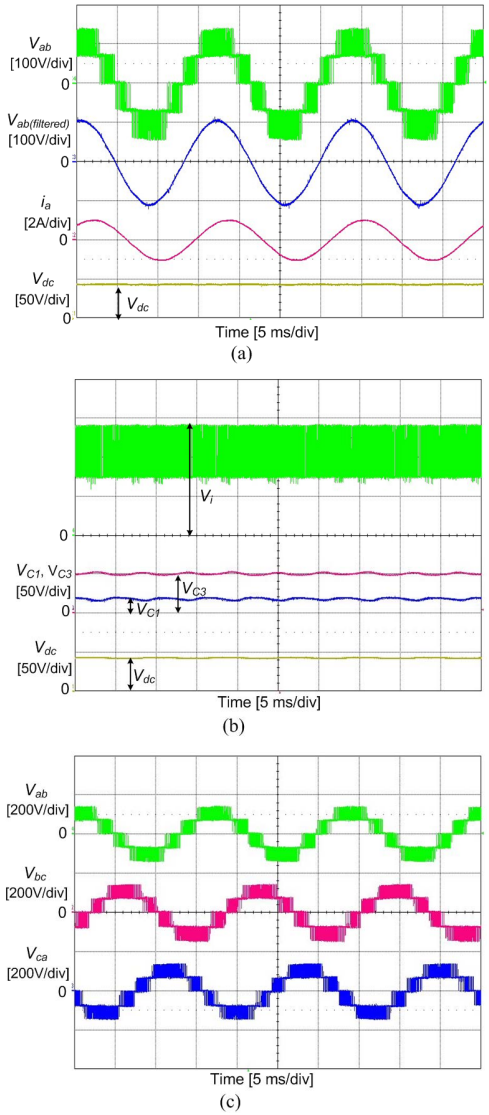

Fig. 16. Experimental results of the proposed topology when M = 0.9: (a) ac output voltage and current and dc input voltage, (b) dc-link, dc input, and capacitor voltages, (c) three-phase output voltage.

MZS-NPC inverter designed and constructed in the laboratory; this was fabricated to validate the operational analysis and simulation results. The prototype consists of a modified Z-source impedance network, a three-phase three-level NPC inverter, a three-phase LC filter, and a control board with a 32-bit DSP-type TMS320F28335. Three resistive-inductive loads with R_L = 50 Ω (400 W), L_L = 1.2 mH (220 V / 10 A), which are the same load used in the simulation, are connected at the three-phase ac output terminal. The 4-channel 12-bit D/A converter, DAC 8420 is used for investigating the experimental waveforms of the reference peak voltage, the peak load voltage, and M through the digital oscilloscope. The semiconductor types used in the experimental prototype are given as follows:

- Control processor (DSP): TMS320F28335 (Clock frequency = 150 MHz)
- IGBT module: SKM50GB063D (600 V / 50 A)
- Diode module: STTH60L06TV (600 V / 40 A)

Fig. 15 shows the experimental results of the proposed topology when M = 0.8 using the same operating conditions as

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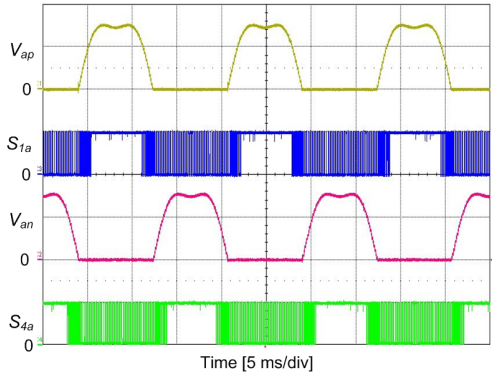

Fig. 17. A-phase modulation and PWM signals when $M = 0.8$.

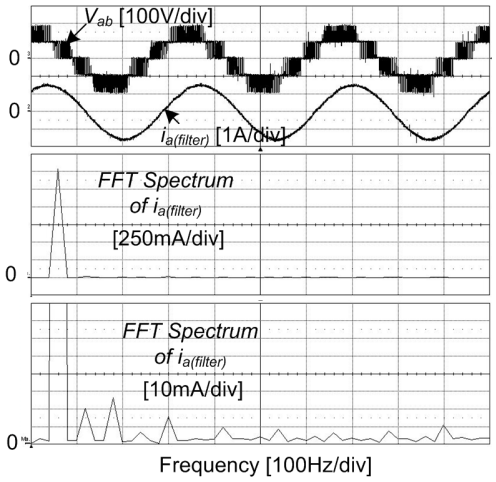

Fig. 18. FFT spectrum analysis of the filtered ac load current when $M = 0.8$.

for simulation results shown in Fig. 11. The RMS value of the filtered output line-to-line voltage is about 102 V, and the dc-link voltage can be boosted to about 205 V. The average values of the two capacitor voltages V_{C1} and V_{C3} are 65 V and 35 V, respectively. From Fig. 15(c), the two series capacitor voltages V_{C1} and V_{C2} are balanced, and the two series capacitor voltages and the two inductor currents have some ripple components with three times frequency of the inverter frequency. The output, dc-link, and capacitor voltages of the experimental results shown in Fig. 15 are slightly lower than those of the simulation results shown in Fig. 11(a) and the theoretical analysis results; this is due to the ESRs of the inductors and capacitors as well as the voltage drops of diodes and IGBTs. From Fig. 15(d), the inductor currents i_{L1} and i_{L2} increase during the upper and lower shoot-through states, respectively. During the non-shoot-through state, the dc-link voltage of the NPC inverter is the peak voltage and the dc input current is zero because diode D_i is off as shown in Fig. 4.

Fig. 16 shows the experimental results when M increases from 0.8 to 0.9. It can be seen that the output, capacitor, and dc-link voltages are nearly the same as those of the simulation results shown in Fig. 12, where the ESRs of both the inductors and capacitors in the Z-source impedance network and voltage

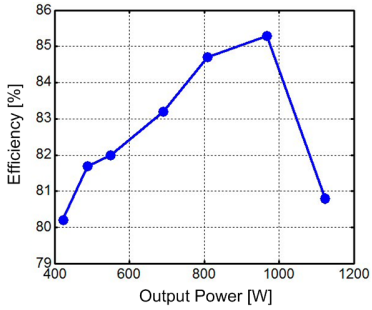

Fig. 19. Efficiency of proposed topology when $M = 0.8$.

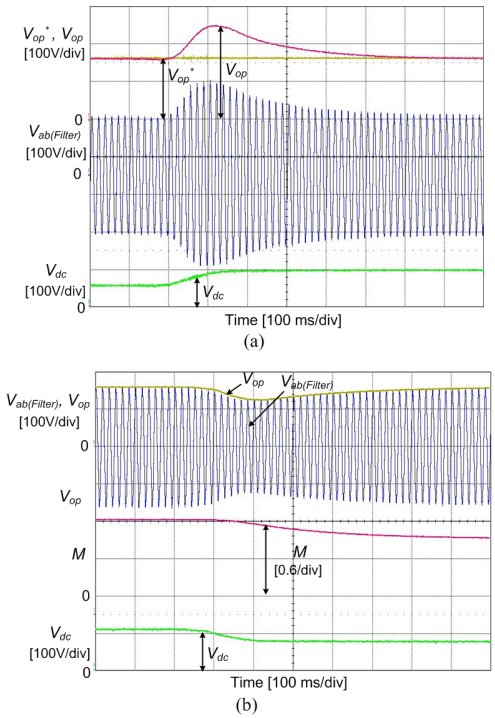

Fig. 20. Experimental results for transient responses of the load voltage: (a) when the dc input voltage increases from 60 V to 100 V, (b) when the dc input voltage decreases from 110 V to 80 V.

drops of the diodes are considered. From Fig. 16(c), the three-phase output voltages are balanced with a 120° phase shift. Fig. 17 shows a-phase modulation signals V_{ap} and V_{an} and two PWM signals S_{1a} and S_{4a}. The switching signal S_{1a} is set to logic '1' when V_{ap} is the highest among the three-phase positive modulation signals, and the switching signal S_{4a} is set to logic '1' when V_{an} is the highest among the three-phase negative modulation signals.

The FFT spectrum analysis of the filtered a-phase load current when $M = 0.8$ is shown in Fig. 18. The THD of the filtered load current is a low value of 1.3 %, despite of the fact that the load current has the low-order harmonics caused by the low-frequency ripple components of the capacitor voltages. Fig. 19 describes the efficiency of the proposed MZS-NPC inverter, which ranges between 80.2 % and 85.3 % according to the output power variations, where the output power is adjusted by

changing the load resistance value at the resistive load while the ac output voltage remains constant.

Fig. 20 shows the transient response of the ac load voltage when the dc input voltage is changed in islanding mode of a microgrid. The peak load voltage is well regulated to its reference voltage $110\sqrt{2}V$, when the dc input voltage increases from 60 V to 100 V and it decreases from 110 V to 80 V. From 20 (b), the modulation index *M* decreases in order to raise the dc-ac voltage gain for keeping the load voltage to 110 Vrms, when the dc input voltage decreases from 110 V to 80 V.

VII. Conclusion

This paper proposed a novel topology of a three-phase three-level modified Z-source NPC (MZS-NPC) inverter, which combines a modified Z-source impedance network and a three-phase three-level NPC inverter. The boost factor of the proposed MZS-NPC inverter is twice as high as the other three topologies over the entire shoot-through duty ratio range. A modified modulation scheme based on a maximum boost control method for the proposed topology is implemented with a simple logic circuit, in order to achieve the maximum voltage gain. The zero average neutral-point current condition can be achieved by balancing the two series capacitor voltages. As demonstrated by simulation and experimental results, the dc-link voltage is boosted to 205 V and a line-to-line output voltage of 102 Vrms can be generated under a dc input voltage of 40 V when *M* is 0.8. The proposed topology provides the ac output current with a low THD of 1.3 %. With the proposed load voltage closed-loop control approach in islanding operation mode of a microgrid, the load voltage is well regulated to the desired voltage 110 Vrms when the dc input voltage is varied. The proposed three-level MZS-NPC inverter is suitable for the fuel-cell or PV applications in islanding operation mode of a microgrid, regarding ability to provide a high voltage gain.

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Anh-Vu Ho was born in Vietnam in 1981. He received B.S. and M.S. degrees in Electrical Engineering from the Ho Chi Minh City University of Technical Education, Ho Chi Minh City, Vietnam, in 2005 and 2009, respectively. He received a Ph.D. degree in Electrical Engineering from the University of Ulsan, Ulsan, Korea, in 2015. He is presently working as a Lecturer in the School of Engineering, Eastern International University, Binh Duong, Vietnam. His current research interests are power converters/inverters, power quality, and renewable energy systems.

Tae-Won Chun (S'85 - M'88) was born in Korea in 1959. He received the B.S. degree in Electrical Engineering from Pusan National University in 1981, and received the M.S. and Ph.D. degrees in Electrical Engineering from Seoul National University in 1983 and 1987, respectively. Since 1986, he has been a member of the faculty of the Department of Electrical Engineering, Ulsan University, where he is currently a full Professor. He was with the Department of Electrical and Computer Engineering, University of Tennessee, USA as a visiting scholar. From 2005 to 2006, he also served as a visiting scholar with the Department of Electrical and Computer Engineering, Virginia Polytechnic Institute and State University, USA. His current research interests are the grid-connected inverter system and ac motor control.