Integrated DC-DC Converter Based Grid-Connected Transformerless Photovoltaic Inverter with Extended Input Voltage Range

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***Abstract*—Owing to low cost, small size and low weight, transformerless inverters became prominent in single-phase grid connected photo-voltaic systems. Key issues pertaining to these inverters include suppression of common mode leakage current and improvement of conversion efficiency. Achieving higher efficiency in single-phase grid-connected photo-voltaic systems depends on the number of stages involved in feeding power to the grid, predominantly, if the photovoltaic (PV) array voltage is less than peak value of the grid voltage. In this paper, an integrated dc-dc converter based grid-connected transformerless PV inverter is proposed which is aimed at maintaining a high efficiency even if the PV array voltage falls below the peak value of grid voltage (efficient operation at an extended input voltage range). A modulation strategy is discussed in order to minimize the flow of common-mode leakage current. Further, the efficiencies of certain transformerless inverter topologies are analyzed and compared with that of the proposed topology. Detailed simulation studies are carried out in MATLAB/Simulink environment to verify the analysis. Experimental results for a scaled down laboratory prototype are included as a proof-of-concept to validate the claims.**

***Keywords*—Common Mode Leakage Current, Extended Input Voltage, High Efficiency, Grid-Connected Transformerless PV Inverter, PV inverter topology, PV system efficiency, Single-phase PV system, Single-stage PV system**

I. Introduction

In grid-connected photo-voltaic (PV) systems, the energy yield and payback time are greatly dependent on the initial cost and efficiency of the inverter. Other important factors in single-phase grid-feeding inverters are its weight and size. Therefore, the use of transformerless single-phase grid-feeding inverters with high conversion efficiency is desirable. In case of transformerless systems, there is no galvanic isolation between the PV panels and the grid which may lead to the appearance of high frequency common-mode (CM) voltage, and consequently, a CM leakage current may flow through parasitic capacitance of the PV panels. This is undesirable and should be limited to a low value as described in standard DIN VDE 0126-1-1 [1].

In order to minimize the ground leakage current and improve the efficiency of the system, several grid-connected transformerless solar PV inverter topologies are discussed in literature [2]–[11]. A full-bridge inverter along with a ac bypass (FB-ACBP) is discussed in [12] which is called as Highly Efficient and Reliable Inverter Concept (HERIC) topology. A fluctuating CM voltage could be observed since the freewheeling path potiential is not clamped. However, the ground leakage current is minimized to an acceptable level. SMA Solar Technology Ag. suggested the use of a H5 topology [13]. This topology is further improved in [14] where an additional switch is used to eliminate the CM current. A midpoint coupled H6 topology is discussed in [2] which offers reduced switching losses. Based on this topology several midpoint coupled grid-feeding transformerless topologies are presented in [15].

A family of flying capacitor transformerless inverters is proposed in [16] which addresses the issue of leakage currents. Highly efficient topologies are proposed in [8], [10], [17]–[20]. In [8], a single-phase transformerless inverter is proposed which is composed of two step-down converters. A high level of efficiency and reliability is achieved by using only four semiconductor devices. In [10], high efficiency of the inverter is achieved by naturally keeping the body diodes of the switches inactive. Cho et. al. [18] suggested a highly efficient and power dense inverter. It consists of a dual-paralled-buck inverter and two auxiliary circuits are provided for zero-current switching turn-off of the diodes, thus improving the system efficiency. In [19], the use of superjuction MOSFETs and SiC diodes enables a high inverter efficiency. In renewable power generation systems (like solar), the input dc voltage of the converter may vary greatly. For example, the output dc voltage of a solar panel changes with different temperature conditions [9]. Partial shading of the PV modules connected in a string also causes wide variations in the Maximum Power Point (MPP) voltage [21]. Degradation of the panel over the years also reduces the output voltage significantly [22]. These topologies [8], [10], [16]–[20] do not discuss about the efficiency at lower input voltages. The addition of a boost stage for lower input PV voltages reduces the efficiency of the system. Commercially available inverters (eg. REFUsol AE 1TL) address this issue

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by employing the REFUsol's topology [23]. A single-stage circuit is employed when the input voltage is above the critical level and a step-up converter is used when the PV array voltage falls below it. This topology however, requires a higher input voltage (almost double compared to previous topologies), due to its similarity with half bridge inverter. Single-stage topologies such as the Z-source inverter, $quasi-Z$ source inverter or the split source inverter eliminate the additional dc-dc converter by utilizing a passive boosting stage [24]. However, with conventional modulation techniques, they are not suitable for transformerless inverter operation on account of having a variable common mode voltage, and consequently, a high leakage current [25]. In addition, the capacitors and inductors for the single-phase Z-source topologies have to be rated for twice the dc-link voltage and the rated current due to its inherent design structure [26].

In summary, the design of the inverter should be aimed towards higher efficiency (for a wide PV voltage range) and low CM leakage current. In order to simultaneously address these challenges, a novel topology is proposed in this paper, which contains a dc-dc converter that is energized only when the PV array voltage drops below the critical voltage. The proposed topology has the following features:

1) No double stage conversion - Improves the efficiency of the overall system.
2) Multi-levels in the inverter output voltage when the dc-dc converter is active - Reduces the distortion of the grid current.
3) Minimized CM leakage current - Suitable for grid-connected transformerless PV systems.

The rest of the paper is organized as follows. Section II describes the operation and control of the proposed inverter topology. A modulation strategy is provided which suppresses the flow of CM leakage current. Section III gives the simulation and experimental results to validate the claims. Simulations are carried out using MATLAB/Simulink. A comparison is terms of efficiency has been made between three transformerless inverter topologies (proposed topology, HERIC + boost topology and H5 + boost topology). A scaled down laboratory prototype of the proposed inverter is developed and results are discussed. Finally, conclusions are drawn in section IV.

II. Operation and Control of the Proposed Inverter Topology

The proposed inverter topology is depicted in Fig. 1. It incorporates a HERIC inverter configuration (S_1-S_6) with two additional semiconductor switches (S_7 and S_8) respectively. The circuit is designed to work in two distinct modes of operation namely three-level mode and five-level mode.

When the PV array output voltage is greater than the peak grid voltage, S_7 is kept on and S_8 is kept off. This enables the circuit to operate as a HERIC inverter using switches S_1-S_6. The dc-dc converter (consisting of S_9, L_{dc} and D_{10}) remains off during this mode. This enables the three-level mode of operation, similar to a HERIC inverter. In case the PV array output voltage falls below the peak grid voltage, the dc-dc converter is energized. This leads to a transfer of power from the PV to the second dc-link capacitor C_{dc2} such that total dc-link voltage ($V_{dc1}+V_{dc2}$) becomes more than the peak grid voltage. This mode of operation gives a five-level inverter voltage output which shows the multilevel operation of the proposed circuit while operating under low PV voltage conditions. The voltage across C_{dc2} is V_{dc2} and is used by the inverter only when the instantaneous grid voltage is more than the PV array voltage (V_{dc1}), as shown in Fig. 2. During the period when the instantaneous grid voltage is less then the PV voltage, V_{dc1}, power is directly used from PV. Therefore, the dc-dc converter only processes a fraction of the total PV power. Most of the power flows directly from PV to the inverter, thereby leading to higher efficiency even at low PV voltage as compared to the use of dc-dc boost converter in cascade with conventional inverters. This concept is represented using block diagram as shown in Fig. 3. The conventional structure is shown in Fig. 3(a) and the partial power processing structure is shown in Fig. 3(b). Details of the operation of the inverter are discussed thereafter.

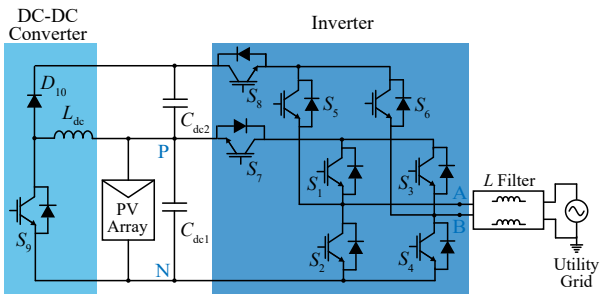


Fig. 1: Circuit Diagram of the proposed inverter topology. (Anti-parallel diodes of the switches S_1-S_9 are labeled as D_1-D_9 respectively)

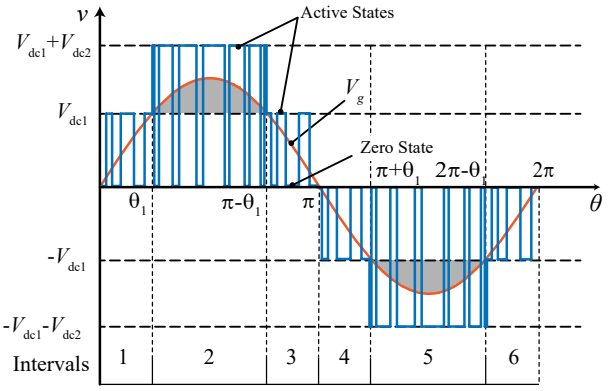


Fig. 2: Working Principle of the Proposed Inverter Topology.

A. Operation

The operating principle for the five-level mode of operation is explained in detail. It should be noted that the three-level mode of operation is similar to the operation of a grid-connected HERIC inverter. The reference grid voltage is divided into six

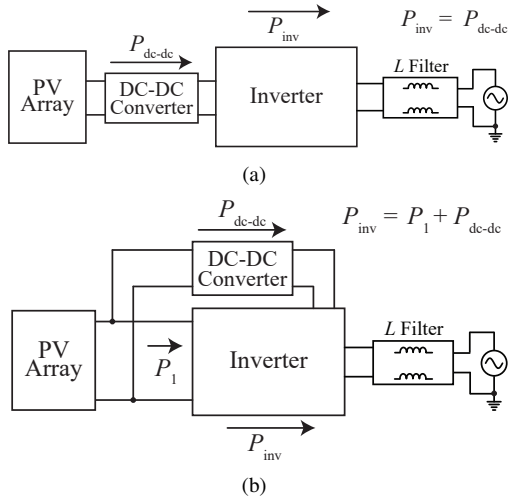


Fig. 3: Power processed by the dc-dc converter and the inverter in (a) Conventional Toplogies (b) Proposed Topology.

different intervals of operation, as shown in Fig. 2.

Interval 1 ($0 < \theta < \theta_1$): In this interval, the inverter output voltage is realized using an active (V_{dc1}) state and a zero state. The active state is achieved by turning on the devices S_1, S_4 and S_7. The path for the flow of current in this state is shown in Fig. 4(a). In order to achieve the zero state S_5 and S_6 are turned on and the grid current freewheels through the devices (S_5, D_6 or S_6, D_5) as shown in Fig.4(c). The dc-dc converter remains non-energized. During this interval, S_5 and S_7 are continuously kept on, thereby avoiding switching loss in these devices.

Interval 2 ($\theta_1 < \theta < \pi - \theta_1$): During this interval, the inverter output voltage lies between the zero state and the active state ($V_{\text{dc1}} + V_{\text{dc2}}$). Zero state is realized by turning on S_5 and S_6 as shown in Fig. 4(c). To realize the active state of $V_{\text{dc1}} + V_{\text{dc2}}$, switches S_4, S_5 and S_8 are turned on, as shown in Fig. 4(b). Since the capacitor C_{dc2} is used, the voltage across it is maintained by the boost converter (S_9, D_{10}, L_{dc}).

Interval 3 ($\pi - \theta_1 < \theta < \pi$): The operation of the topology in interval 3 is same as that in Interval 1. Active state (shown in Fig. 4(a) and zero state (shown in Fig.4(c)) are used.

Interval 4 ($\pi < \theta < \pi + \theta_1$): In this interval, the reference signal lies between zero and $-V_{\text{dc1}}$. The zero state is realized as shown in Fig. 4(c). For the active state $-V_{\text{dc1}}$, S_2, S_3 and S_7 are turned on, as shown in Fig. 4(d). The dc-dc converter remains off in this mode.

Interval 5 ($\pi + \theta_1 < \theta < 2\pi - \theta_1$): In this mode, an active state ($-V_{\text{dc1}} - V_{\text{dc2}}$) and a zero state are used. The active state is realized by turning on the switches S_2, S_6 and S_8, as shown in Fig. 4(e). The dc-dc converter maintains voltage across C_{dc2} during this mode.

Interval 6 ($2\pi - \theta_1 < \theta < 2\pi$): The operation of the topology in interval 6 is same as that in interval 4. Active state (shown in Fig.4(d) and zero state (shown in Fig.4(c)) are used.

B. Modulation Strategy

The modulation strategy is based on the Phase Opposition Disposition (POD) sinusoidal PWM technique as shown in Fig. 5. Carriers C_1 and C_3 have peak values of ($V_{\text{dc1}} + V_{\text{dc2}}$) and ($-V_{\text{dc1}} - V_{\text{dc2}}$), where as the peak value of C_2 and C_4 are V_{dc1} and $-V_{\text{dc1}}$, respectively. C_2 is compared with a sinusoidal reference in the positive half cycle during Intervals 1 and 3 to generate switching signals for S_1, S_4 and S_7 where as C_1 is compared with the reference signal in Interval 2 to generate the switching signal for S_8. The switching signals for S_5 and S_6 are complementary of S_2 and S_4, respectively. Similarly, during the negative half cycle C_4 is compared with the reference signal during Intervals 4 and 6 to generate switching signals for S_2, S_3 and S_7. C_3 is compared with the reference signal in Interval 5 to generate switching signal for S_8. This strategy enables a multilevel (five level) operation of the inverter.

It should be noted that, this modulation strategy ensures a low leakage current in the PV system, which is imperative for grid-connected applications. In [27], a simplified equivalent model of the common-mode resonant circuit is derived. The CM voltage (u_{cm}) as defined in [27] is given by

$$u_{cm} = \frac{u_{AN} + u_{BN}}{2} \tag{1}$$

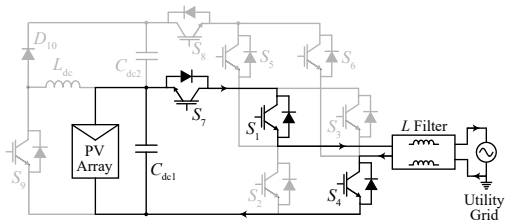
where, u_{AN} is the voltage between Node A and Node N, and u_{BN} is the voltage between Node B and Node N as shown in Fig. 1. The CM voltages for each state is derived and provided in Fig. 5. It is concluded that since the CM voltages for both the states is an interval are equal, there would not be any high frequency oscillations in the CM voltage. This would suppress the flow of leakage current. This is further justified by simulation and experimental results in Section III.

C. Control Technique

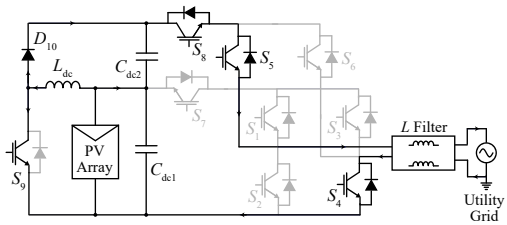
The control objectives of the system are

- The PV array voltage (V_{dc1}) is maintained equal to its Maximum Power Point (MPP) value, as determined by the Maximum Power Point Tracking (MPPT) controller.
- When the inverter runs in five-level mode, V_{dc2} is maintained such that the total dc-link voltage ($V_{\text{dc1}} + V_{\text{dc2}}$) remains more than the peak voltage of the grid

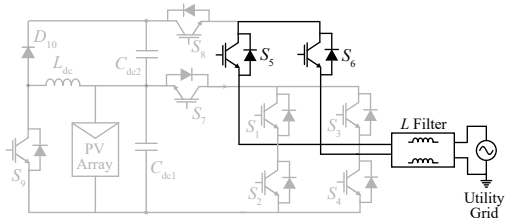
In order to achieve these objectives, V_{dc1} is controlled by the inverter and V_{dc2} is controlled by the boost converter. The complete control block diagram for the proposed topology is shown in Fig. 6. The PV voltage (V_{pv}) and the PV current (I_{pv}) are sensed and given as inputs to the MPPT block which generates the reference value of the dc-link voltage



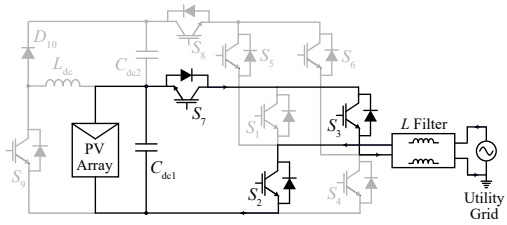
(a) Active State in Mode 1/ Mode 3.



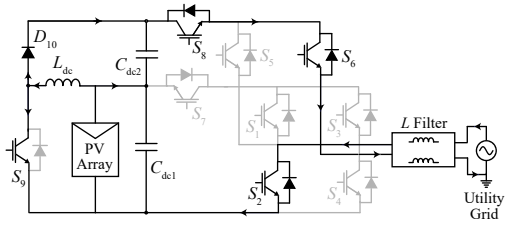
(b) Active State in Mode 2.



(c) Zero State in all modes (The current direction depends on the mode of operation).

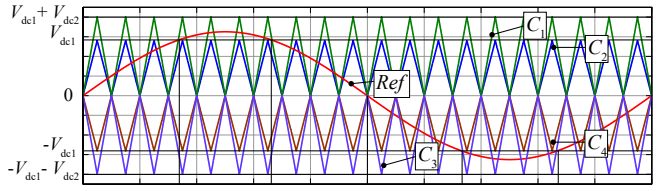


(d) Active State in Mode 4/ Mode 6.



(e) Active State in Mode 5.

Fig. 4: Equivalent circuits for different states and modes of operation in the proposed inverter topology for unity power factor operation.



Active Switches						
	Mode 1	**Mode 2**	**Mode 3**	**Mode 4**	**Mode 5**	**Mode 6**
Active State	S_7, S_1, S_4	S_8, S_5, S_4	S_7, S_1, S_4	S_7, S_3, S_2	S_8, S_6, S_2	S_7, S_3, S_2
Zero State	S_5, S_6	S_6, S_7	S_5, S_6	S_5, S_6	S_5, S_6	S_5, S_6

Common Mode Voltages						
	Mode 1	**Mode 2**	**Mode 3**	**Mode 4**	**Mode 5**	**Mode 6**
Active State	$\frac{V_{dc1}}{2}$	$\frac{V_{dc1}+V_{dc2}}{2}$	$\frac{V_{dc1}}{2}$	$\frac{V_{dc1}}{2}$	$\frac{V_{dc1}+V_{dc2}}{2}$	$\frac{V_{dc1}}{2}$
Zero State	$\frac{V_{dc1}}{2}$	$\frac{V_{dc1}+V_{dc2}}{2}$	$\frac{V_{dc1}}{2}$	$\frac{V_{dc1}}{2}$	$\frac{V_{dc1}+V_{dc2}}{2}$	$\frac{V_{dc1}}{2}$

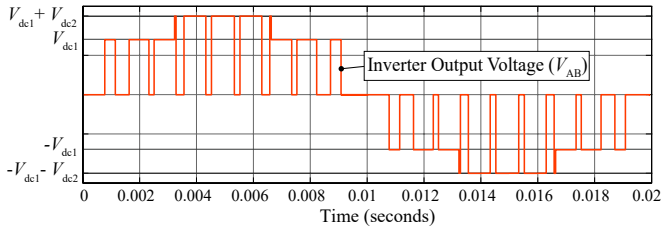


Fig. 5: Modulation Strategy used for the proposed topology (Carrier frequency of 1 kHz is shown for illustrative purpose. Actual carrier frequency is 20 kHz). Active switches in each cycle is also provided here along with the common mode voltages for each mode.

(V^*_{dc1}). The outer voltage control loop of the inverter employs a Proportional Integral (PI) controller which generates the in-phase component of the current reference. A suitable PI controller is designed for the inner current control loop to control the grid current. The reference signal is generated from the inner current controller which is given to the Pulse Width Modulation (PWM) block. The switching signals are thus generated for S_1-S_8.

In case V^*_{dc1} is less than the peak value of the grid voltage, the inverter goes into a five-level mode of operation. The reference voltage V^*_{dc2} is generated such that,

$$V^*_{dc2} = V_{dc,critical} - V^*_{dc1} \quad (2)$$

where, $V_{dc,critical}$ is a value greater than the grid voltage peak value. The dc-dc converter is used to regulate the voltage V_{dc2}, as shown in Fig. 6. The scheme includes voltage and current controller in cascaded configuration to generate the gate signal for switch S_9.

III. Simulation & Experimental Results

A. Simulation Results

The specifications of the inverter used are shown in Table I. The inverter topology is simulated in MATLAB/Simulink environment. The dc-link capacitor is designed based on [28] and the filter inductors are designed based on [29]. A common-mode filter, based on a coupled inductor, is employed on grid side for electromagnetic compatibility (EMC). The value of parasitic capacitance used in the simulation is 500 nF (200 nF/kW) [30]. A higher value of parasitic capacitance than the worst case scenario (about 150 nF/kW) is chosen to test the effectiveness of the proposed topology. The actual characteristics of a PV source is modeled in MATLAB/Simulink. A total

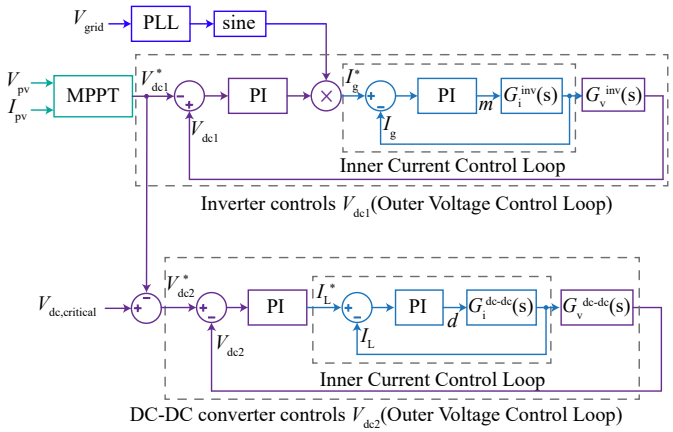


Fig. 6: Complete closed loop control technique of the inverter.

dc-link voltage of 400 V is considered. The PV source voltage is set at a MPP voltage of 280 V and the dc-dc converter is used to generate the extended input voltage of 120 V.

TABLE I: Specification for the Proposed PV inverter

Parameter	Values Used	
	Simulation	Experimental
Input Voltage, V_{dc1}	280 V	70 V
Extended Input Voltage, V_{dc2}	120 V	30 V
Grid Voltage/frequency	230 V/50 Hz	56 V/50 Hz
Rated Power, S	2.5 kVA	220 VA
Carrier Frequency, F_c	20 kHz	20 kHz
DC bus capacitors C_{dc1}/C_{dc2}	1.5 mF/470 μF	1 mF/470 μF
DC-DC converter inductor, L_{dc}	0.6 mH	1.5 mH
AC Filter inductor, L_i	1.3 mH×2	0.9 mH×2
PV parasitic capacitance, C_p	500 nF	40 nF
Common Mode Choke, L_{cm}	L_{cm}: 670 μH; L_{dm}: 5 μH	L_{cm}: 670 μH; L_{dm}: 5 μH
Switches, $S_1 - S_9$	-	IKW50N65F5
Diode, D_{10}	-	RURG8060F085
Digital Controller	-	TMS320F2808

The simulated waveforms for the five-level mode of operation is shown in Fig. 7(a). Inverter voltage waveforms confirm the five-level operation. Grid voltage and current are sinusoidal and in the same phase. The three level mode of operation closely resembles the operation of a HERIC inverter as shown in Fig. 7(b). Fig. 8 shows the voltages across the parasitic capacitances, PC_1 (connected between positive terminal of solar PV and ground) and PC_2 (connected between negative terminal of solar PV and ground) and the total leakage current. It is seen that the high frequency components in the parasitic capacitor voltages are insignificant. This ensures that the leakage current flowing through these capacitors is minimized. The total RMS current through the combination of both the parasitic capacitors is found to be 18.05 mA in the three-level mode of operation and 18.13 mA the five level mode of operation, respectively.

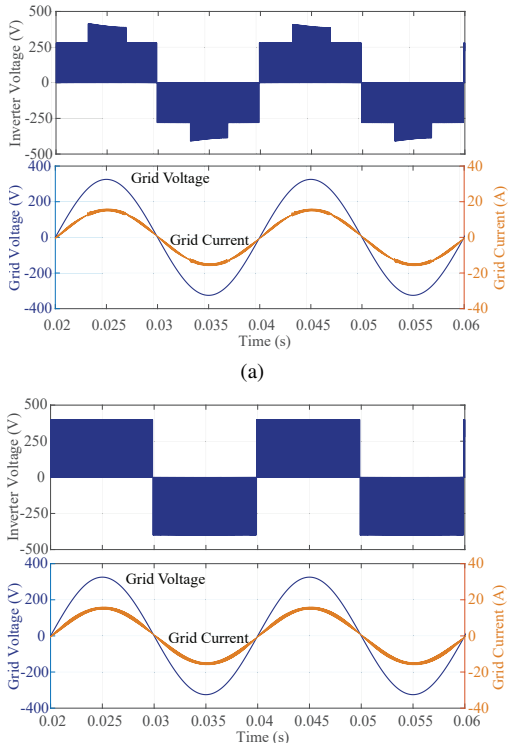


Fig. 7: Simulation results for (a) Five-level mode of operation at unity power factor (c) Three-level mode of operation at unity power factor.

A theoretical efficiency analysis is carried out to compare the performance of the proposed topology with two well known commercialized inverter topologies namely H5 and HERIC. In case of H5 and HERIC a dc-dc converter is included at the input side to allow operation at low PV voltages. The specifications of the inverter used for the calculation is provided in Table I(same as simulated parameters). All the switches and diode specifications are used from Infineon's IKW50N65F5 (IGBTs) and Fairchild's RURG8060F085, respectively. Fig. 9 gives a comparison between the efficiency of the three different topologies based on various types of losses for a PV voltage of 280 V. It is observed that the conduction losses are slightly more in the proposed topology as compared to the HERIC topology. This is mainly due to addition of more number of switches/diodes in the conduction path. However, due to the use of partial power processing instead of full power processing and use of multilevel topology, the switching and therefore theoverall losses in the proposed topology is found to be less than the HERIC + boost topology at PV voltage of 280 V.

Fig. 10 compares the efficiency of the three topologies with varying voltages. It is observed that both H5 and HERIC gives higher efficiency in case of high PV voltage (more than the peak of ac voltage). The additional loss in the proposed scheme is mainly due to more switches in conduction path, leading to higher conduction loss. However, as the PV voltage reduces,

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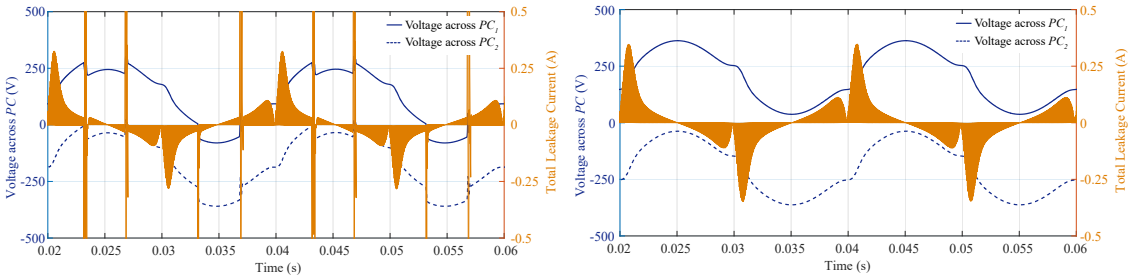

Fig. 8: Simulation results for voltage and currents across the parasitic capacitances for (a) Five-level mode of operation (RMS value of total leakage current: 18.13 mA) (b) Three-level mode of operation (RMS value of total leakage current: 18.05 mA).

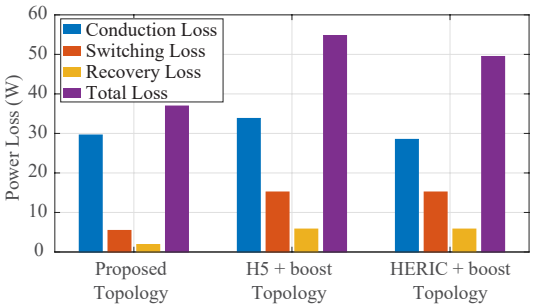

Fig. 9: Total power loss for three different topologies: Proposed topology, H5 + boost topology and HERIC + boost topology for a PV voltage of 280 V and a power of 2.5 kW.

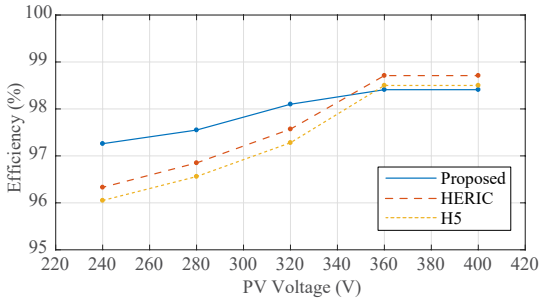

Fig. 10: Comparison between efficiency (simulated) of the proposed topology with H5 + boost and HERIC + boost topologies for different voltage levels (Boost converter gets energized at 320 V) for a power output of 2.5 kW. The efficiency vs power plot is not provided since it is similar to HERIC for PV array voltage levels above the critical value. This graph highlights the higher efficiency of the proposed topology at lower voltage levels.

the efficiency reduction in the HERIC + boost topology and the H5 + boost topology is significant. On the other hand the drop in the efficiency of the proposed scheme is much smaller. At lower voltage levels, the proposed inverter offers higher efficiency as compared to the other two topologies. This is due to the fact that the dc-dc converter has to process a fraction of the total power in the proposed topology unlike H5 + boost or HERIC + boost topology.

B. Experimental Results

A scaled down laboratory prototype is built in order to validate the operation of the proposed inverter. Table I gives the parameters used for the experimental setup. Fig. 11 shows the laboratory prototype of the proposed inverter.

The prototype is tested for both the modes of operation. Fig. 12(a) shows the experimental results for unity power factor operation in the five-level mode. It should be noted that the three-level mode is similar to HERIC inverter operation and is shown in Fig.12(b). In addition, the parasitic capacitor voltage and current flowing thorough it (leakage current) are provided in Fig. 13. It should be noted that the parasitic capacitance is modeled as two capacitances (20 nF connected from the positive terminal to ground, and 20 nF connected from the negative terminal to ground). A higher value of parasitic capacitance (180 nF/kW) than the worst case scenario

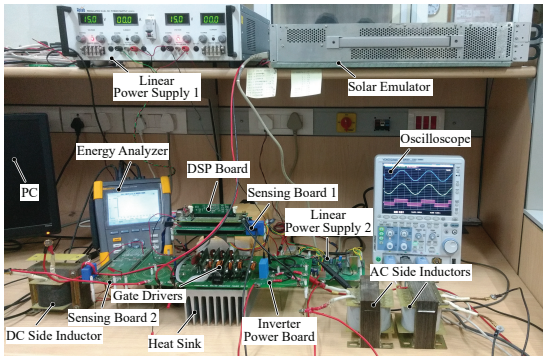

Fig. 11: Experimental Prototype of the Proposed Inverter.

(about 150 nF/kW) is chosen to test the effectiveness of the proposed topology. The voltage across parasitic capacitor had only low frequency ac and dc components. It does not have high frequency components. Therefore, the leakage current value is expected to be small. The total RMS leakage current is found to be 16.2 mA for the five-level mode of operation and 12.9 mA in three-level mode of operation, which is well within the safety limit of 30 mA [31].

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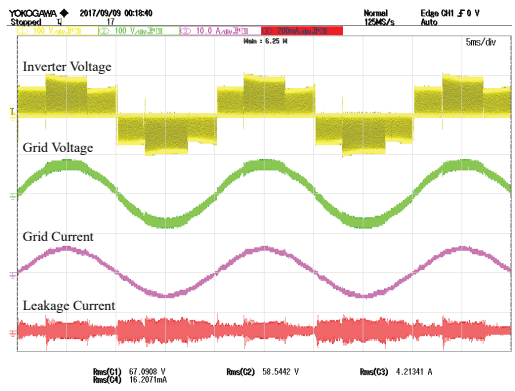
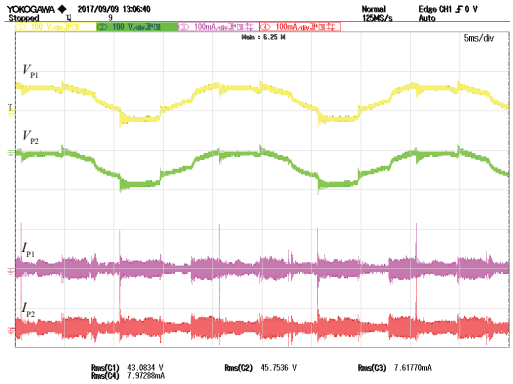


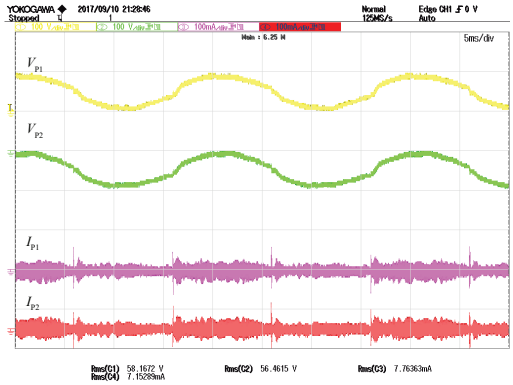
(a)

(b)

Fig. 12: Experimental Results for (a) Five-level mode of operation (RMS value of leakage current: 16.2071 mA) (b) Three-level mode of operation (RMS value of leakage current: 12.9696 mA).[Inverter Voltage: 100 V/div, Grid Voltage: 100 V/div, Grid Current: 10 A/div, Leakage Current: 200 mA/div, Time: 5ms/div].



(a)



(b)

Fig. 13: Voltages across the parasitic capacitors and leakage currents for (a) Five-level mode of operation (RMS value of leakage current (I_{P1}): 7.61 mA; RMS value of leakage current (I_{P2}): 7.97 mA) (b) Three-level mode of operation (RMS value of leakage current (I_{P1}): 7.76 mA; RMS value of leakage current (I_{P2}): 7.15 mA) (V_{P1} and I_{P1} gives the voltage and current across the parasitic capacitor modeled from Node P to the ground. V_{P2} and I_{P2} gives the voltage and current across the parasitic capacitor modeled from Node N to the ground) [V_{P1}: 100 V/div, V_{P2}: 100 V/div, I_{P1}: 100 mA/div, I_{P2}: 100 mA/div, Time: 5ms/div].

The Total Harmonic Distortion (THD) is measured using Fluke 430-II Power Analyzer. Fig. 14 gives the THD plot for the current fed to the grid for both the operating modes. The THD of the grid current is found to be 2.9% for the five-level mode of operation and 4.2% for the three-level mode of operation. This is within the limits specified in the IEEE-519-2014 standards.

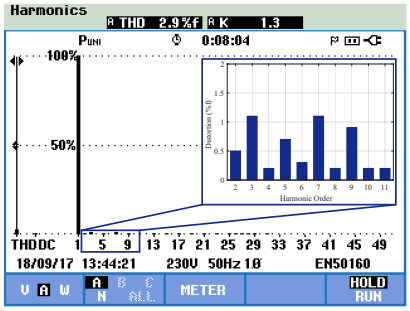
The efficiency of the proposed converter at PV voltage of 80 V and total dc-link voltage of 100 V is found to be 93.72% (for P_{out} = 110 W) and 94.86% (for P_{out} = 220 W). In case of three-level operation, when PV voltage is 100 V the efficiency is observed to be 95.22% (for P_{out} = 110 W) and 96.13% (for P_{out}) = 220 W.

IV. Conclusions

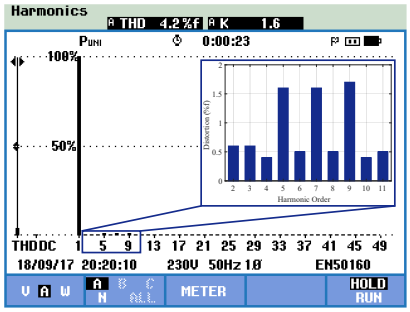
An integrated dc-dc converter based transformerless PV inverter with a wide input voltage range is presented in this paper. The main characteristics of the proposed inverter are summarized as follows:

1) Higher efficiency at low solar radiations as compared to HERIC + boost and H5 + boost topologies, since there is no double stage conversion of power.
2) Multi-levels in the inverter output voltage is achieved when the dc-dc converter is energized, which improves the quality of the grid current.
3) Low CM leakage current flows through the system by employing corresponding modulation strategy, thereby meeting leakage current standards.

Simulation results shows the effectiveness of the proposed inverter. The experimental results tested on a scaled down prototype circuit verify the operation of the proposed inverter. The grid current THD is found to be 2.9% for the five-level mode of operation and 4.2% for the three-level mode of operation, which is within the IEEE-519-2014 standards. Further, the total leakage current is found to be 16.2 mA for the five-level mode of operation and 12.9 mA in three-level mode of operation, which is well within the safety limit of 30 mA [31]. The proposed inverter topology is suitable for grid-connected transformerless single-phase PV applications,



(a)



(b)

Fig. 14: Harmonic Spectrum of the grid current for the proposed topology for (a) Five-level mode of operation (THD = 2.9%) (b) Three-level mode of operation (THD = 4.2%). The lower order harmonics are zoomed and shown in the inset.

especially for wide variations in solar PV voltage.

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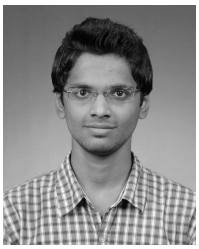

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