Transformerless DC–DC Converters With High Step-Up Voltage Gain

Lung-Sheng Yang, Tsorng-Juu Liang, *Member, IEEE*, and Jiann-Fuh Chen, *Member, IEEE*

***Abstract*—Conventional dc–dc boost converters are unable to provide high step-up voltage gains due to the effect of power switches, rectifier diodes, and the equivalent series resistance of inductors and capacitors. This paper proposes transformerless dc–dc converters to achieve high step-up voltage gain without an extremely high duty ratio. In the proposed converters, two inductors with the same level of inductance are charged in parallel during the switch-on period and are discharged in series during the switch-off period. The structures of the proposed converters are very simple. Only one power stage is used. Moreover, the steady-state analyses of voltage gains and boundary operating conditions are discussed in detail. Finally, a prototype circuit is implemented in the laboratory to verify the performance.**

***Index Terms*—DC–DC boost converter, high step-up voltage gain, power stage.**

I. Introduction

A DC–DC converter with a high step-up voltage gain is used for many applications, such as high-intensity-discharge lamp ballasts for automobile headlamps, fuel-cell energy conversion systems, solar-cell energy conversion systems, and battery backup systems for uninterruptible power supplies. Theoretically, a dc–dc boost converter can achieve a high step-up voltage gain with an extremely high duty ratio [1]–[3]. However, in practice, the step-up voltage gain is limited due to the effect of power switches, rectifier diodes, and the equivalent series resistance (ESR) of inductors and capacitors. Moreover, the extremely high duty-ratio operation will result in a serious reverse-recovery problem. Many topologies have been presented to provide a high step-up voltage gain without an extremely high duty ratio [4]–[24]. A dc–dc flyback converter is a very simple structure with a high step-up voltage gain and an electrical isolation, but the active switch of this converter will suffer a high voltage stress due to the leakage inductance of the transformer. For recycling the energy of the leakage inductance and minimizing the voltage stress on the active switch, some energy-regeneration techniques have been proposed to clamp the voltage stress on the active switch and to recycle the leakage-inductance energy [4]–[6]. The coupled-inductor techniques provide solutions to achieve a high voltage gain, a low voltage stress on the active switch, and a high efficiency without the penalty of high duty ratio [7]–[15]. Literature includes some research of the transformerless dc–dc converters, which include the cascade boost type [16], the quadratic boost type [17], the voltage-lift type [18]–[20], the capacitor-diode voltage multiplier type [21], [22], and the boost type integrating with switched-capacitor technique [23]. However, these types are all complex and have a higher cost. The modified boost type with switched-inductor technique is shown in Fig. 1 [24]. The structure of this converter is very simple. Only one power stage is used in this converter. However, this converter has two issues: 1) Three power devices exist in the current-flow path during the switch-on period, and two power devices exist in the current-flow path during the switch-off period, and 2) the voltage stress on the active switch is equal to the output voltage.

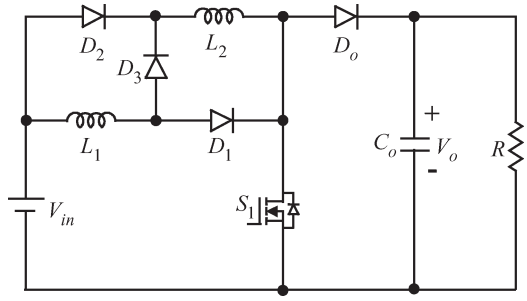

Fig. 1. Transformerless dc–dc high step-up converter [24].

A transformerless dc–dc high step-up converter is proposed in this paper, as shown in Fig. 2(a). Compared with the converter in [24], the proposed converter I has the following merits: 1) Two power devices exist in the current-flow path during the switch-on period, and one power device exists in the current-flow path during the switch-off period; 2) the voltage stresses on the active switches are less than the output voltage; and 3) under the same operating conditions, including input voltage, output voltage, and output power, the current stress on the active switch during the switch-on period is equal to the half of the current stress on the active switch of the converter in [24]. For getting higher step-up voltage gain, the other dc–dc converters are also presented in this paper, as shown in Fig. 2(b) and (c). These three proposed dc–dc converters utilize the switched-inductor technique, in which two inductors with same level of inductance are charged in parallel during the switch-on period and are discharged in series during the switch-off period, to achieve high step-up voltage gain without the extremely high duty ratio. The operating principles and steady-state analysis are discussed in the following sections. To analyze the steady-state characteristics of the proposed converters, some conditions are assumed as follows: 1) All components are ideal—the ON-state resistance $R_{\mathrm{DS(ON)}}$ of the active switches, the forward voltage drop of the diodes, and the ESRs of the inductors and capacitors are ignored—and 2) all capacitors are sufficiently

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The authors are with the Department of Electrical Engineering, National Cheng Kung University, Tainan 701, Taiwan (e-mail: yanglungsheng@yahoo.com.tw; tjliang@mail.ncku.edu.tw; chenjf@mail.ncku.edu.tw).

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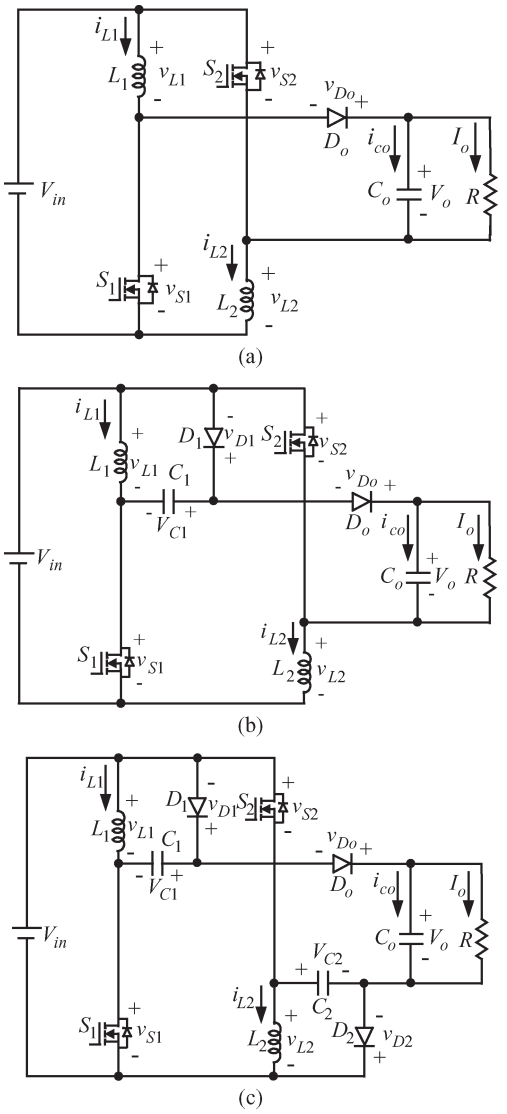

Fig. 2. Proposed high step-up dc–dc converters. (a) Converter I. (b) Converter II. (c) Converter III.

large, and the voltages across the capacitors can be treated as constant.

II. Proposed Converter I

Fig. 2(a) shows the circuit configuration of the proposed converter I, which consists of two active switches (S_1 and S_2), two inductors (L_1 and L_2) that have the same level of inductance, one output diode D_o, and one output capacitor C_o. Switches S_1 and S_2 are controlled simultaneously by using one control signal. Fig. 3 shows some typical waveforms obtained during continuous conduction mode (CCM) and discontinuous conduction mode (DCM). The operating principles and steady-state analysis of CCM and DCM are presented in detail as follows.

A. CCM Operation

The operating modes can be divided into two modes, defined as modes 1 and 2.

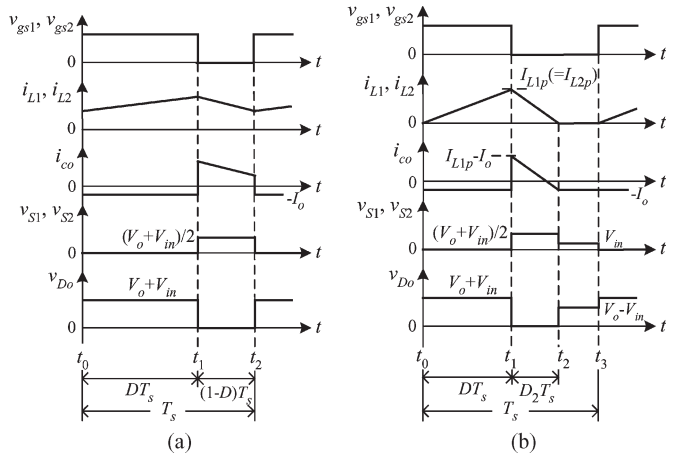

Fig. 3. Some typical waveforms for the proposed converter I. (a) CCM operation. (b) DCM operation.

1) Mode 1 $[t_0, t_1]$. During this time interval, switches S_1 and S_2 are turned on. The equivalent circuit is shown in Fig. 4(a). Inductors L_1 and L_2 are charged in parallel from the dc source, and the energy stored in the output capacitor C_o is released to the load. Thus, the voltages across L_1 and L_2 are given as

$$\nu_{L1} = \nu_{L2} = V_{\text{in}}. \tag{1}$$

2) Mode 2 $[t_1, t_2]$. During this time interval, S_1 and S_2 are turned off. The equivalent circuit is shown in Fig. 4(b). The dc source, L_1, and L_2 are series connected to transfer the energies to C_o and the load. Thus, the voltages across L_1 and L_2 are derived as

$$\nu_{L1} = \nu_{L2} = \frac{V_{\text{in}} - V_o}{2}. \tag{2}$$

By using the volt–second balance principle on L_1 and L_2, the following equation can be obtained:

$$\int_0^{DT_s} V_{\text{in}}\, dt + \int_{DT_s}^{T_s} \frac{V_{\text{in}} - V_o}{2}\, dt = 0. \tag{3}$$

By simplifying (3), the voltage gain is given by

$$M_{\text{CCM}} = \frac{V_o}{V_{\text{in}}} = \frac{1+D}{1-D}. \tag{4}$$

From Fig. 3(a), the voltage stresses on S_1, S_2, and D_o are derived as

$$\begin{cases} V_{S1} = V_{S2} = \frac{V_o + V_{\text{in}}}{2} \\ V_{Do} = V_o + V_{\text{in}}. \end{cases} \tag{5}$$

B. DCM Operation

The operating modes can be divided into three modes, defined as modes 1, 2, and 3.

1) Mode 1 $[t_0, t_1]$. The operating principle is the same as that for mode 1 of the CCM operation. The two peak currents

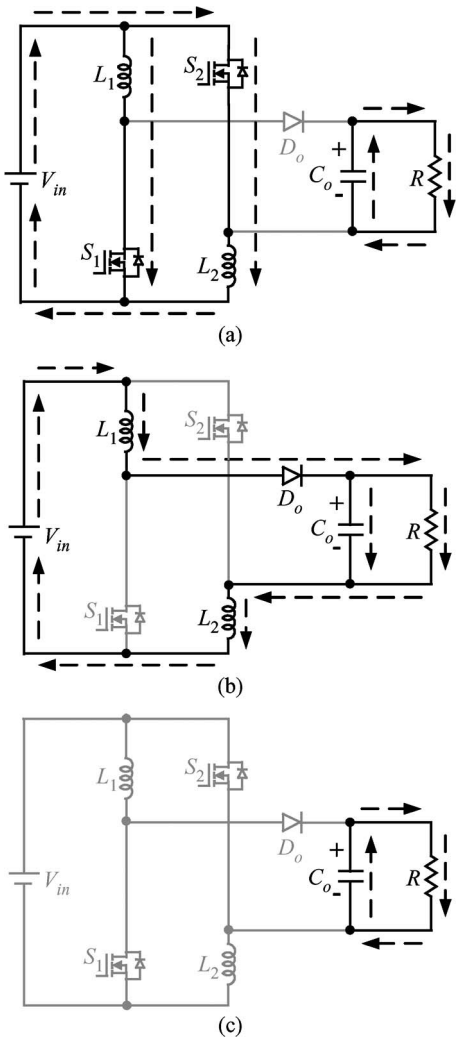

Fig. 4. Equivalent circuits of the proposed converter I. (a) Switches ON. (b) Switches OFF. (c) Switches OFF in DCM operation.

of L_1 and L_2 can be found as

$$I_{L1p} = I_{L2p} = \frac{V_{\rm in}}{L} DT_s \tag{6}$$

where L is the inductance of L_1 and L_2.

2) Mode 2 $[t_1, t_2]$. During this time interval, S_1 and S_2 are turned off. The equivalent circuit is shown in Fig. 4(b). The dc source, L_1, and L_2 are series connected to transfer the energies to C_o and the load. Inductor currents i_{L1} and i_{L2} are decreased to zero at $t = t_2$. Another expression of I_{L1p} and I_{L2p} is given as

$$I_{L1p} = I_{L2p} = \frac{V_o - V_{\rm in}}{2L} D_2 T_s. \tag{7}$$

3) Mode 3 $[t_2, t_3]$. During this time interval, S_1 and S_2 are still turned off. The equivalent circuit is shown in Fig. 4(c). The energies stored in L_1 and L_2 are zero. Thus, only the energy stored in C_o is discharged to the load.

From (6) and (7), D_2 is derived as follows:

$$D_2 = \frac{2DV_{\rm in}}{V_o - V_{\rm in}}. \tag{8}$$

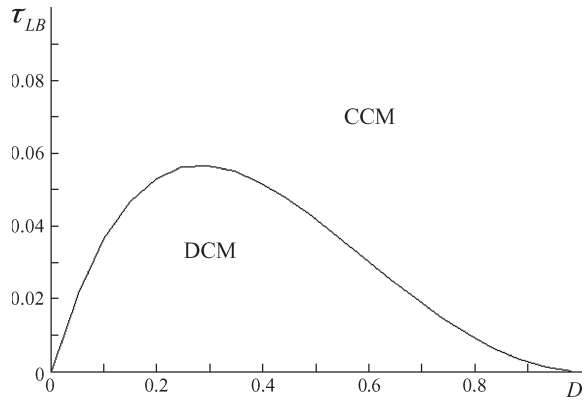

Fig. 5. Boundary condition of the proposed converter I.

From Fig. 3(b), the average value of the output-capacitor current during each switching period is given by

$$I_{co} = \frac{\frac{1}{2} D_2 T_s I_{L1p} - I_o T_s}{T_s} = \frac{1}{2} D_2 I_{L1p} - I_o. \tag{9}$$

Substituting (6) and (8) into (9), I_{co} is derived as

$$I_{co} = \frac{D^2 V_{\rm in}^2 T_s}{L(V_o - V_{\rm in})} - \frac{V_o}{R}. \tag{10}$$

Since I_{co} is equal to zero under steady state, (10) can be rewritten as follows:

$$\frac{D^2 V_{\rm in}^2 T_s}{L(V_o - V_{\rm in})} = \frac{V_o}{R}. \tag{11}$$

Then, the normalized inductor time constant is defined as

$$\tau_L \equiv \frac{L f_s}{R} \tag{12}$$

where f_s is the switching frequency ($f_s = 1/T_s$).

Substituting (12) into (11), the voltage gain is given by

$$M_{\rm DCM} = \frac{V_o}{V_{\rm in}} = \frac{1}{2} + \sqrt{\frac{1}{4} + \frac{D^2}{\tau_L}}. \tag{13}$$

C. Boundary Operating Condition Between CCM and DCM

If the proposed converter I is operated in boundary conduction mode (BCM), the voltage gain of the CCM operation is equal to the voltage gain of the DCM operation. From (4) and (13), the boundary normalized inductor time constant τ_{LB} can be derived as follows:

$$\tau_{LB} = \frac{D(1-D)^2}{2(1+D)}. \tag{14}$$

The curve of τ_{LB} is shown in Fig. 5. If τ_L is larger than τ_{LB}, the proposed converter I is operated in CCM.

III. Proposed Converter II

Fig. 2(b) shows the circuit configuration of the proposed converter II, which is the proposed converter I with one voltage-lift

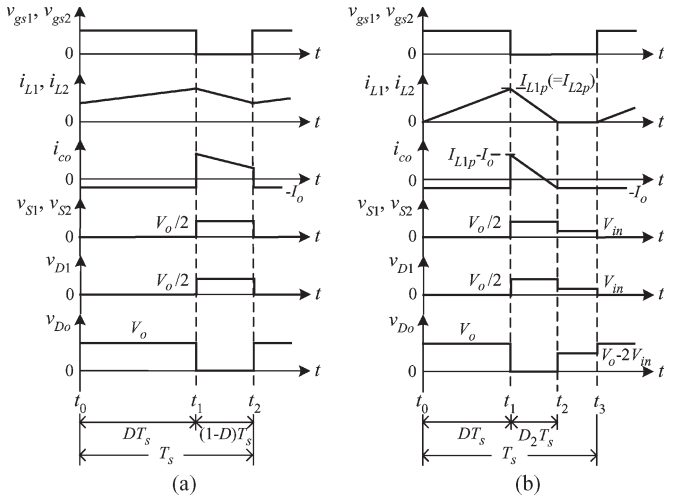

Fig. 6. Some typical waveforms for the proposed converter II. (a) CCM operation. (b) DCM operation.

circuit [18]–[20]. Thus, two inductors (L_1 and L_2) with the same level of inductance are also adopted in this converter. Switches S_1 and S_2 are controlled simultaneously by one control signal. Fig. 6 shows some typical waveforms of CCM and DCM. Moreover, the operating principles and steady-state analysis of CCM and DCM are presented as follows.

A. CCM Operation

The operating modes can be divided into two modes, defined as modes 1 and 2.

1) Mode 1 $[t_0, t_1]$. During this time interval, S_1 and S_2 are turned on. The equivalent circuit is shown in Fig. 7(a). L_1 and L_2 are charged in parallel from the dc source, and the energy stored in C_o is released to the load. Moreover, capacitor C_1 is charged from the dc source. Thus, the voltages across L_1, L_2, and C_1 are given as

$$\nu_{L1} = \nu_{L2} = V_{C1} = V_{\rm in}. \tag{15}$$

2) Mode 2 $[t_1, t_2]$. During this time interval, S_1 and S_2 are turned off. The equivalent circuit is shown in Fig. 7(b). The dc source, L_1, C_1, and L_2 are series connected to transfer the energies to C_o and the load. Thus, the voltages across L_1 and L_2 are derived as

$$\nu_{L1} = \nu_{L2} = \frac{V_{\rm in} + V_{c1} - V_o}{2} = \frac{2V_{\rm in} - V_o}{2}. \tag{16}$$

By using the volt–second balance principle on L_1 and L_2, the following can be obtained:

$$\int_0^{DT_s} V_{\rm in}\, dt + \int_{DT_s}^{T_s} \frac{2V_{\rm in} - V_o}{2}\, dt = 0. \tag{17}$$

By simplifying (17), the voltage gain is given by

$$M_{\rm CCM} = \frac{V_o}{V_{\rm in}} = \frac{2}{1-D}. \tag{18}$$

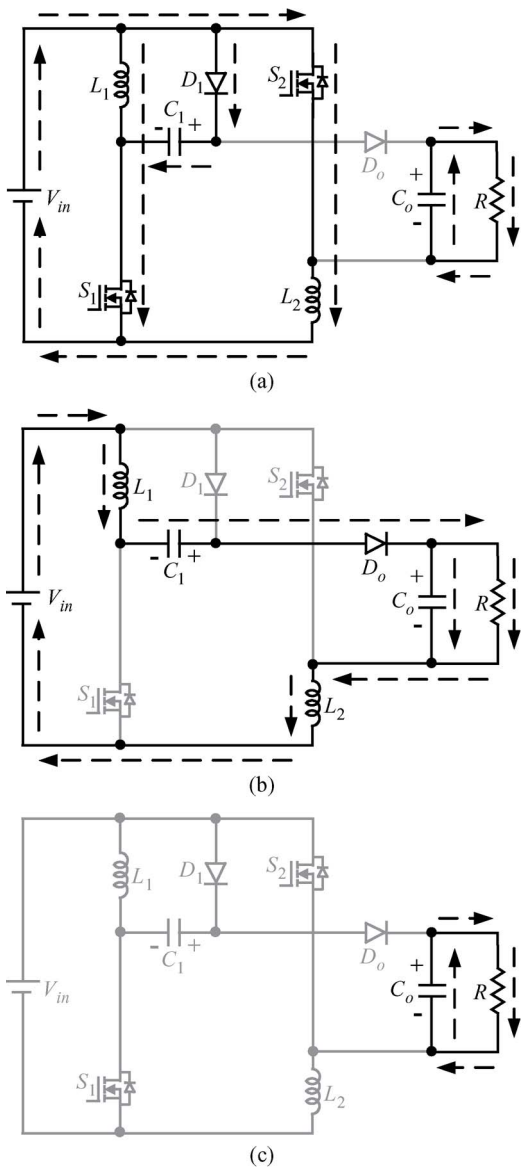

Fig. 7. Equivalent circuits of the proposed converter II. (a) Switches ON. (b) Switches OFF. (c) Switches OFF in DCM operation.

From Fig. 6(a), the voltage stresses on S_1, S_2, D_1, and D_o are derived as

$$\begin{cases} V_{S1} = V_{S2} = V_{D1} = \frac{V_o}{2} \\ V_{Do} = V_o. \end{cases} \tag{19}$$

B. DCM Operation

The operating modes can be divided into three modes, defined as modes 1, 2, and 3.

1) Mode 1 $[t_0, t_1]$. The operating principle is the same as that for mode 1 of the CCM operation. The two peak currents of L_1 and L_2 can be found as

$$I_{L1p} = I_{L2p} = \frac{V_{\rm in}}{L} DT_s. \tag{20}$$

2) Mode 2 $[t_1, t_2]$. During this time interval, S_1 and S_2 are turned off. The equivalent circuit is shown in Fig. 7(b).

The dc source, L_1, C_1, and L_2 are series connected to transfer the energies to C_o and the load. The values for i_{L1} and i_{L2} are decreased to zero at $t = t_2$. Another expression for I_{L1p} and I_{L2p} is given as

$$I_{L1p} = I_{L2p} = \frac{V_o - V_{\rm in} - V_{c1}}{2L} D_2 T_s = \frac{V_o - 2V_{\rm in}}{2L} D_2 T_s. \tag{21}$$

3) Mode 3 $[t_2, t_3]$. During this time interval, S_1 and S_2 are still turned off. The equivalent circuit is shown in Fig. 7(c). The energies stored in L_1 and L_2 are zero. Thus, only the energy stored in C_o is discharged to the load.

From (20) and (21), D_2 is derived as follows:

$$D_2 = \frac{2DV_{\rm in}}{V_o - 2V_{\rm in}}. \tag{22}$$

From Fig. 6(b), the average output-capacitor current during each switching period is given by

$$I_{co} = \frac{\frac{1}{2} D_2 T_s I_{L1p} - I_o T_s}{T_s} = \frac{1}{2} D_2 I_{L1p} - I_o. \tag{23}$$

By substituting (20) and (22) into (23), I_{co} is derived as

$$I_{co} = \frac{D^2 V_{\rm in}^2 T_s}{L(V_o - 2V_{\rm in})} - \frac{V_o}{R}. \tag{24}$$

Since I_{co} is equal to zero under steady state, (24) can be rewritten as follows:

$$\frac{D^2 V_{\rm in}^2 T_s}{L(V_o - 2V_{\rm in})} = \frac{V_o}{R}. \tag{25}$$

Thus, the voltage gain is given by

$$M_{\rm DCM} = \frac{V_o}{V_{\rm in}} = 1 + \sqrt{1 + \frac{D^2}{\tau_L}}. \tag{26}$$

C. Boundary Operating Condition Between CCM and DCM

If the proposed converter II is operated in BCM, the voltage gain of the CCM operation is equal to the voltage gain of the DCM operation. From (18) and (26), the boundary normalized inductor time constant τ_{LB} can be derived as

$$\tau_{LB} = \frac{D(1-D)^2}{4}. \tag{27}$$

The curve of τ_{LB} is shown in Fig. 8. If τ_L is larger than τ_{LB}, the proposed converter II is operated in CCM.

IV. Proposed Converter III

Fig. 2(c) shows the circuit configuration of the proposed converter III, which is the proposed converter I with two voltage-lift circuits. Thus, two inductors (L_1 and L_2) with the same level of inductance are also adopted in this converter. Switches S_1 and S_2 are controlled simultaneously by one control signal. Fig. 9 shows some typical waveforms of CCM and DCM.

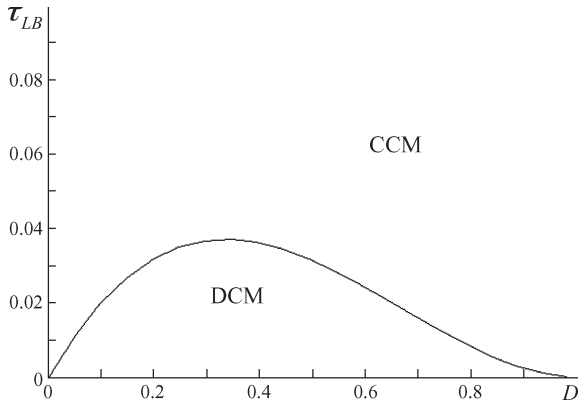

Fig. 8. Boundary condition of the proposed converter II.

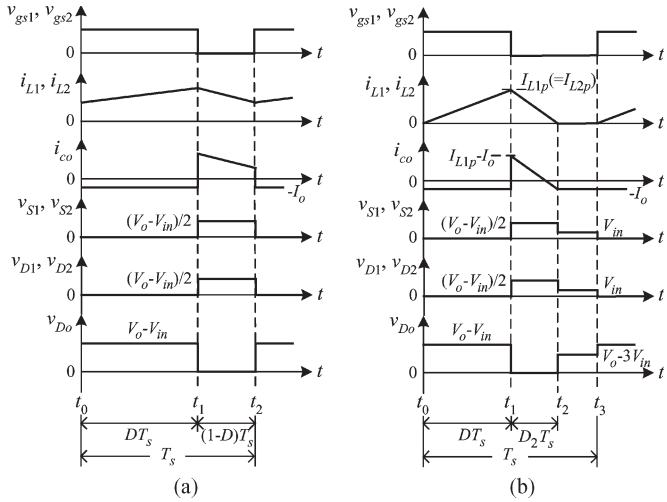

Fig. 9. Some typical waveforms for the proposed converter III. (a) CCM operation. (b) DCM operation.

Moreover, the operating principles and steady-state analysis of CCM and DCM are presented as follows.

A. CCM Operation

The operating modes can be divided into two modes, defined as modes 1 and 2.

1) Mode 1 $[t_0, t_1]$. During this time interval, S_1 and S_2 are turned on. The equivalent circuit is shown in Fig. 10(a). L_1 and L_2 are charged in parallel from the dc source, and the energy stored in C_o is released to the load. Moreover, capacitors C_1 and C_2 are charged from the dc source. Thus, the voltages across L_1, L_2, C_1, and C_2 are given as

$$\nu_{L1} = \nu_{L2} = V_{C1} = V_{C2} = V_{\rm in}. \tag{28}$$

2) Mode 2 $[t_1, t_2]$. During this time interval, S_1 and S_2 are turned off. The equivalent circuit is shown in Fig. 10(b). The dc source, L_1, C_1, C_2, and L_2 are series connected to transfer the energies to C_o and the load. Thus, the voltages across L_1 and L_2 are derived as

$$\nu_{L1} = \nu_{L2} = \frac{V_{\rm in} + V_{c1} + V_{c2} - V_o}{2} = \frac{3V_{\rm in} - V_o}{2}. \tag{29}$$

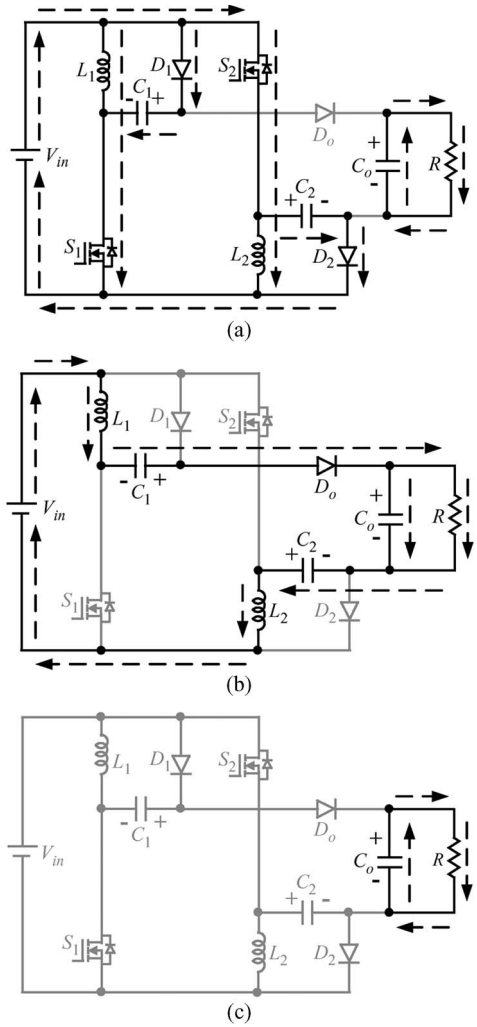

Fig. 10. Equivalent circuits of the proposed converter III. (a) Switches ON. (b) Switches OFF. (c) Switches OFF in DCM operation.

By using the volt–second balance principle on L_1 and L_2, the following can be obtained:

$$\int_0^{DT_s} V_{\rm in}\,dt + \int_{DT_s}^{T_s} \frac{3V_{\rm in}-V_o}{2}\,dt = 0. \tag{30}$$

By simplifying (30), the voltage gain is given by

$$M_{\rm CCM} = \frac{V_o}{V_{\rm in}} = \frac{3-D}{1-D}. \tag{31}$$

From Fig. 9(a), the voltage stresses on S_1, S_2, D_1, D_2, and D_o are derived as

$$\begin{cases} V_{S1} = V_{S2} = V_{D1} = V_{D2} = \frac{V_o - V_{\rm in}}{2} \\ V_{Do} = V_o - V_{\rm in}. \end{cases} \tag{32}$$

B. DCM Operation

The operating modes can be divided into three modes, defined as modes 1, 2, and 3.

1) Mode 1 $[t_0, t_1]$. The operating principle is the same as that for mode 1 of CCM operation. The two peak currents of L_1 and L_2 can be found as

$$I_{L1p} = I_{L2p} = \frac{V_{\rm in}}{L} DT_s. \tag{33}$$

2) Mode 2 $[t_1, t_2]$. During this time interval, S_1 and S_2 are turned off. The equivalent circuit is shown in Fig. 10(b). The dc source, L_1, C_1, C_2, and L_2 are series connected to transfer the energies to C_o and the load. The values for i_{L1} and i_{L2} are decreased to zero at $t = t_2$. Another expression for I_{L1p} and I_{L2p} is given as

$$\begin{aligned} I_{L1p} = I_{L2p} &= \frac{V_o - V_{\rm in} - V_{c1} - V_{c2}}{2L} D_2 T_s \\ &= \frac{V_o - 3V_{\rm in}}{2L} D_2 T_s. \end{aligned} \tag{34}$$

3) Mode 3 $[t_2, t_3]$. During this time interval, S_1 and S_2 are still turned off. The equivalent circuit is shown in Fig. 10(c). The energies stored in L_1 and L_2 are zero. Thus, only the energy stored in C_o is discharged to the load.

From (33) and (34), D_2 is derived as follows:

$$D_2 = \frac{2DV_{\rm in}}{V_o - 3V_{\rm in}}. \tag{35}$$

From Fig. 9(b), the average output-capacitor current during each switching period is given by

$$I_{co} = \frac{\frac{1}{2} D_2 T_s I_{L1p} - I_o T_s}{T_s} = \frac{1}{2} D_2 I_{L1p} - I_o. \tag{36}$$

By substituting (33) and (35) into (36), I_{co} is derived as

$$I_{co} = \frac{D^2 V_{\rm in}^2 T_s}{L(V_o - 3V_{\rm in})} - \frac{V_o}{R}. \tag{37}$$

Since I_{co} is equal to zero under steady state, (37) can be rewritten as follows:

$$\frac{D^2 V_{\rm in}^2 T_s}{L(V_o - 3V_{\rm in})} = \frac{V_o}{R}. \tag{38}$$

Thus, the voltage gain is given by

$$M_{\rm DCM} = \frac{V_o}{V_{\rm in}} = \frac{3}{2} + \sqrt{\frac{9}{4} + \frac{D^2}{\tau_L}}. \tag{39}$$

C. Boundary Operating Condition Between CCM and DCM

If the proposed converter III is operated in BCM, the voltage gain of CCM operation is equal to the voltage gain of DCM operation. From (31) and (39), the boundary normalized inductor time constant τ_{LB} can be derived as follows:

$$\tau_{LB} = \frac{D(1-D)^2}{2(3-D)}. \tag{40}$$

The drawing of τ_{LB} is shown in Fig. 11. If τ_L is larger than τ_{LB}, the proposed converter III is operated in CCM.

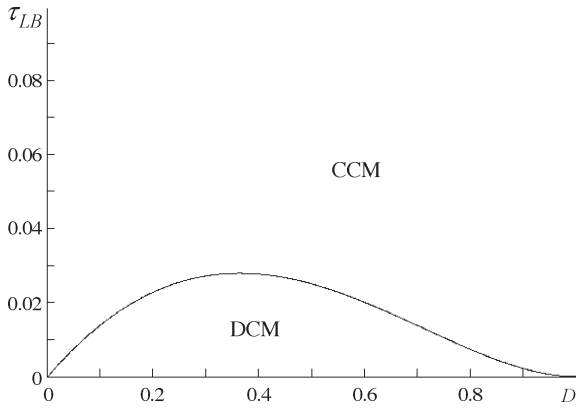

Fig. 11. Boundary condition of the proposed converter III.

TABLE I
COMPARISON OF VOLTAGE GAIN AND VOLTAGE STRESS ON ACTIVE SWITCH FOR BOOST CONVERTER AND THREE PROPOSED CONVERTERS

	M_{CCM}	Voltage stress
Boost converter	$\frac{1}{1-D}$	V_o
Proposed converter I	$\frac{1+D}{1-D}$	$\frac{V_o+V_{in}}{2}$
Proposed converter II	$\frac{2}{1-D}$	$\frac{V_o}{2}$
Proposed converter III	$\frac{3-D}{1-D}$	$\frac{V_o-V_{in}}{2}$

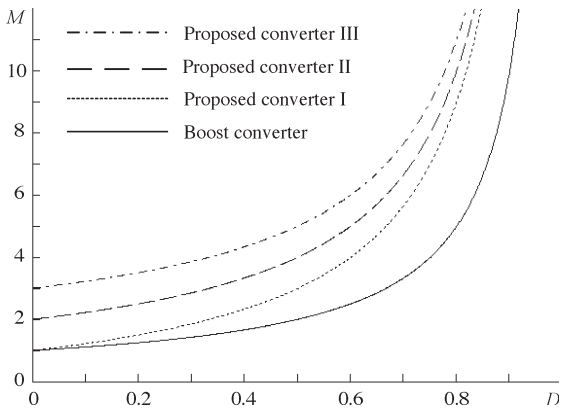

Fig. 12. Voltage gain versus duty ratio for the boost converter and the three proposed converters.

V. COMPARISON OF PROPOSED CONVERTERS AND BOOST CONVERTER

The voltage stresses on the active switch and the voltage gains of the boost converter and the proposed converters are summarized in Table I. The voltage stresses on the active switch of the three proposed converters are less than the voltage stress on the active switch of the boost converter, and thus, the active switches with low voltage ratings and low ON-state resistance levels $R_{DS(ON)}$ can be selected. Moreover, the curves of the voltage gain of the boost converter and the proposed converters are shown in Fig. 12. As illustrated, the proposed converters can achieve high step-up voltage gain.

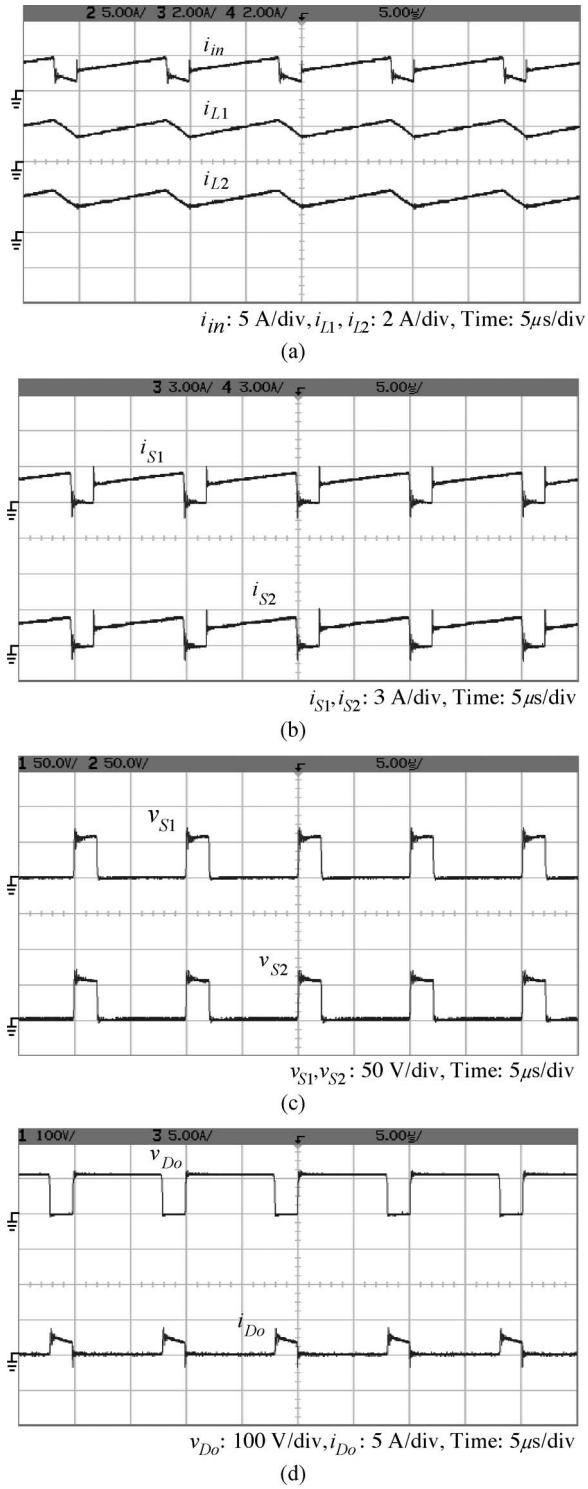

Fig. 13. Some experimental waveforms of the proposed converter I. (a) $i_{\rm in}$, i_{L1}, and i_{L2}. (b) i_{S1} and i_{S2}. (c) ν_{S1} and ν_{S2}. (d) ν_{Do} and i_{Do}.

VI. EXPERIMENTAL RESULTS

To verify the theoretical analyses of the proposed converter I, a 40-W prototype circuit is built in the laboratory for use in an automobile headlamp application. The circuit specifications

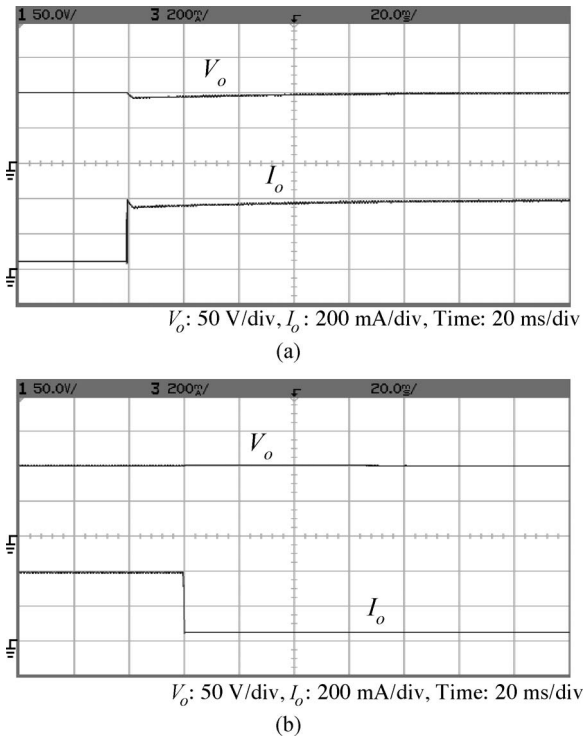

Fig. 14. Dynamic response of the proposed converter I. (a) P_o is charged from 5 to 40 W. (b) P_o is charged from 40 to 5 W.

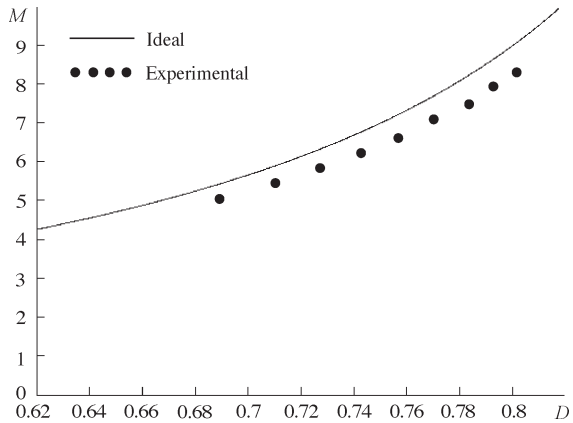

Fig. 15. Ideal and experimental voltage gains of the proposed converter I under $V_{\rm in} = 12$ V, $V_o = 60 - 100$ V, and $P_o = 40$ W.

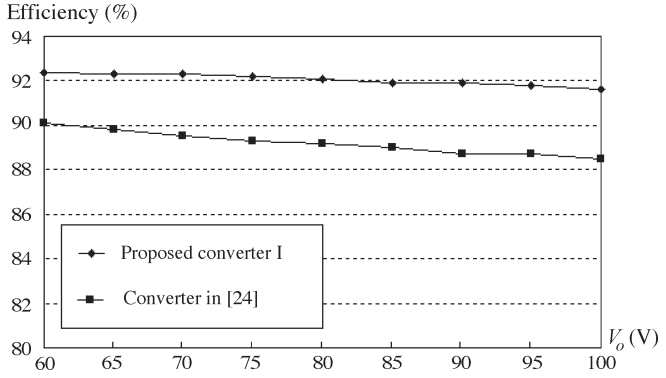

Fig. 16. Experimental efficiency of the proposed converter I and the converter in [24] under $V_{\rm in} = 12$ V, $V_o = 60 - 100$ V, and $P_o = 40$ W.

and components are selected as $V_{\rm in} = 12$ V, $V_o = 60 - 100$ V, $f_s = 100$ kHz, $P_o = 40$ W, $L_1 = L_2 = 100$ μH, and $C_o = 68$ μF. Moreover, MOSFET NTY100N10 is selected for switches S_1 and S_2, and the Schottky diode MBR20200CT is selected for diode D_o.

Under the conditions $V_{\rm in} = 12$ V, $V_o = 100$ V, and $P_o = 40$ W, some experimental results are shown in Fig. 13. Fig. 13(a) shows that i_{L1} is equal to i_{L2}. Moreover, the input current is equal to twice the level of the inductor current during the switch-on period and is equal to the inductor current during the switch-off period. Fig. 13(b) shows the current waveforms i_{S1} and i_{S2}. As can be seen in Fig. 13(c), the voltage stresses on S_1 and S_2 are equal to $(V_o + V_{\rm in})/2$. Fig. 13(d) shows the voltage and current of the output diode. Fig. 14 shows the dynamic response under the output power variation between 5-W light load and 40-W full load. One can see that the output voltage is well regulated. Fig. 15 shows the ideal and experimental voltage gains under $V_{\rm in} = 12$ V, $V_o = 60 - 100$ V, and $P_o = 40$ W. Fig. 16 shows the experimental efficiency of the proposed converter I and the converter in [24] under $V_{\rm in} = 12$ V, $V_o = 60 - 100$ V, and $P_o = 40$ W. It is seen that the proposed converter I has higher efficiency than the converter in [24].

VII. Conclusion

This paper has studied three novel transformerless dc–dc converters with high step-up voltage gain. The structures of the proposed converters are very simple. Since the voltage stresses on the active switches are low, active switches with low voltage ratings and low ON-state resistance levels $R_{\rm DS(ON)}$ can be selected. The steady-state analyses of the voltage gain and the boundary operating condition are discussed in detail. Finally, to illustrate the theoretical analysis, a 40-W prototype circuit of the proposed converter I is built in the laboratory. The experimental results confirm that high step-up voltage gain can be achieved.

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Lung-Sheng Yang was born in Tainan, Taiwan, in 1967. He received the B.S. degree in electrical engineering from the National Taiwan Institute of Technology, Taipei, Taiwan, the M.S. degree in electrical engineering from the National Tsing-Hua University, Hsinchu, Taiwan, and the Ph.D. degree in electrical engineering from the National Cheng Kung University, Tainan, in 1990, 1992, and 2007, respectively.

He is currently with the Department of Electrical Engineering, National Cheng Kung University, Tainan. His research interests are power-factor correction, dc–dc converters, renewable energy conversion, and electronic ballasts.

Tsorng-Juu Liang (S'91–M'95) was born in Kaohsiung, Taiwan. He received the B.S. degree in electrophysics from the National Chiao-Tung University, Hsinchu, Taiwan, in 1985, and the M.S. and Ph.D. degrees in electrical engineering from the University of Missouri, Columbia, in 1990 and 1993, respectively.

From June 1987 to May 1989, he was a Research and Design Engineer with TECO Electric and Machinery Company, Taipei, Taiwan. From 1990 to 1993, he was a Research Assistant with the Power Electronics Research Center, University of Missouri. From 1993 to 1998, he was an Assistant Professor with the Department of Electrical Engineering, Kaohsiung Polytechnic Institute, Kaohsiung. Since 1998, he has been with the Department of Electrical Engineering, National Cheng Kung University (NCKU), Tainan, Taiwan, where he is currently a Professor. Moreover, he was the Director of Electrical Laboratories at NCKU from 2001 to 2004. His research interests are inverter design, electronic ballasts, dc to dc converters, switching power supply, back light inverters, renewable energy conversion, power integrated circuits, and high-power applications.

Dr. Liang is a member of the IEEE Power Electronics, Industrial Electronics, Circuits and System, and Industry Applications Societies.

Jiann-Fuh Chen (S'79–M'80) was born in Chung-Hua, Taiwan, in 1955. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from the National Cheng Kung University (NCKU), Tainan, Taiwan, in 1978, 1980, and 1985, respectively.

Since 1980, he has been with the Department of Electrical Engineering, NCKU, where he is currently a Professor and the Director of the department. His research interests are power electronics and energy conversion.