Combined Sliding-Mode Control for the IFDBC Interfaced DC Mircogrids with Power Electronic Loads

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Abstract-The interleaved floating dual boost converter (IFDBC) is well known for its high voltage gain and low current and voltage ripples. Besides, thanks to its interleaved structure, this topology is quite suitable for high-power applications, such as the solar photovoltaic or energy storage systems that are employed to feed or buffer the DC microgrid (MG). In modern MGs, tightly regulated power electronic loads, which behave like constant power loads (CPLs), are penetrating. Such loads exhibit negative incremental impedance and thus, threaten the DC bus voltage stability in MGs. To stabilize the DC bus voltage of IFDBC fed MG in presence of rapid and large load disturbances, this paper proposes a new nonlinear disturbance observer (NDO) based sliding mode control. The proposed method guarantees global stability of DC bus voltage regulation and provides fast dynamic responses. In addition, to simplify the design of the proposed approach, a generalized reduced order model of IFDBC is developed. Simulation and experiment results are presented to verify the effectiveness of the proposed control approach.

Index Terms– Interleave boost converter, sliding-mode control, constant power load, nonlinear disturbances

I. Introduction

DUE to their eco-friendly nature, the renewable energy sources (RESs) are increasingly used in modern power systems to mitigate the environmental problems and energy crisis [1]. Since many RESs, such as PV generations and fuel cells, are DC in nature, they can be integrated into the DC microgrids (MGs) without extra AC/DC or DC/AC power conversion. However, because of the low and varying terminal voltage produced by RESs, it is infeasible to connect the RESs to the MG DC bus directly [2]. To solve this problem, high boost ratio DC/DC converters are generally needed [3]–[5].

The conventional DC/DC boost converter can not provide high enough voltage gain owing to the inevitable parasitics in practical circuits [6]. To obtain high voltage gain, plenty of high voltage gain DC/DC converters have been proposed in last decades, such as Luo series converters [7], multilevel converter [8], diode-capacitor-based converter [6] and etc. Nevertheless, due to the inductor magnetic saturation problem, these high gain converters are not suitable for the high-power applications [9]. To simultaneously obtain high voltage gain and high power operation ability simultaneously, the interleaved floating dual boost converter (IFDBC) is proposed [10], [11]. Thanks to its interleaved structure, both the input and output current/voltage ripples are suppressed, which allows small size inductor and capacitor to be adopted to increase the system power density and enhance system reliability.

In the modern DC MG, the power electronic loads are increasingly used [12], [13]. Since the tightly regulated power electronic loads are constant power loads (CPLs) in steady-state and may vary rapidly in the large signal sense during transients, they are called as CPLs in this paper for simplicity. Since the CPLs show the characteristics of negative incremental impedance and nonlinearity, the stability of the DC MG is severely threatened [14], [15]. Consequently, controlling the interface converters, such as the IFDBC, to ensure the stability of DC MG systems becomes a challenging issue.

To meet the increasing demands of stabilizing the DC MG with CPLs, many control strategies have been proposed in recent years [15] - [27]. These control strategies can be categorized into linear approaches and non-linear approaches. Among the linear approaches, passive damping method is widely used to enhance the system stability. By introducing the passive components to the system, the negative incremental impedance can be fully compensated [16]. However, the passive damping methods introduce extra physical components, such as capacitors and resistors, which increases system costs and power losses. To avoid these disadvantages, some active damping methods have been presented. The main idea active damping is to inject virtual impedance to shape the system loop gain and achieve system stability. In [15] and [17], a virtual resistance is injected into the source converter to keep the system dominant poles in the left-half complex plane. A source-side series virtual impedance control method is presented in [18]. Such active damping technique not only provides the system a satisfying stability margin, but also improves its dynamic response. However, since the linear approaches are applied based on the linearized small-signal system model, the resulting system stabilities are only valid

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in the neighbourhood around a certain system equilibrium. As such, large-signal perturbations at the load side, which can frequently occur in the DC MGs, may destabilize the entire system [19].

In contrast to the linear control approaches, their non-linear counterparts are able to stabilize the system even in presence of large signal disturbances. In [20], the model predictive control (MPC) technique combined with a high-order sliding mode observer (HOSMO) has been adopted for the DC MG system which feeds CPL. Due to the use of the HOSMO, the negative effects of the system uncertainties and external disturbances on the tracking performance are significantly alleviated. However, the required extremely high computational burden limits its value for practical application. The feedback linearization methods have been presented in [21], [22] to eliminate the non-linearity and negative effects introduced by CPLs. However, as compared with other non-linear control schemes, this method usually provides relatively slow system dynamics [19]. In [23], an input-output linearization scheme is proposed for the boost converter which feeds CPLs. Through transfer the non-minimum phase boost converter system to a minimum phase system, the system large-signal stability is achieved. However, this method is circuit parameters sensitive. The system uncertainties and un-modeled disturbances deteriorate the control performance. Recently, a disturbance observer based backstepping controller has been developed for the conventional boost converter with CPLs [24]. With the help of the disturbance observer, both accurate tracking and large-signal stability are achieved by the backstepping stabilizer. However, the restrictive assumption on the disturbances excludes a large class of practical disturbances, which makes the controller less attractive in terms of practical implementation. A passivity-based control scheme for the DC/DC converter has been reported in [25]. The negative incremental impedance caused by the CPL is damped by shaping the system energy dissipation function. However, there exist a compromise between the tracking accuracy and the system transient response, if the system model is not accurate enough. Since the interface converters operate in variable structures, the sliding-mode control (SMC) scheme is pretty attractive in stabilizing the MG system with CPLs. In [14], a fixed-frequency SMC has been designed for a buck converter feeding CPL. The stability in the sense of large signal is guaranteed. However, it requires extra output current sensor which increases the hardware cost and output impedance. A robust SMC for a conventional DC/DC boost converter with CPL has been presented in [26]. Since the controller design is based on the assumption of constant source voltage, the control performance is sensitive to the source voltage disturbances which are unavoidable in practical applications. Another novel SMC for a boost converter which feeds CPL has been proposed in [27]. Since a relatively large switching gain is required to ensure the system stability, the consequent severe chattering problem makes it less attractive. In addition, afore-mentioned control strategies are mainly designed for the conventional DC/DC converters. The large-signal stability of the advanced converters, such as the IFDBC, with CPLs is rarely discussed [28], [29].

To overcome the afore-mentioned challenges and stabilize

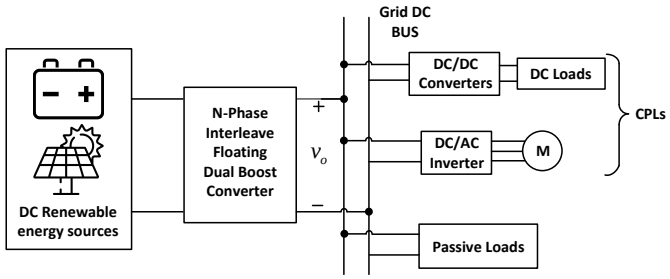

Fig. 1. Generic DC microgrid fed by a N-phase IFDBC

MG system fed by IFDBC in the large-signal sense, a combined non-linear controller is presented in this paper. The main contribution of this paper can be listed as:

1. A generalized reduced-order model of the IFDBC has been derived. Based on this reduced-order model, a new state-variable coordinate system for the IFDBC has been developed to simplify the controller design and the system stability analysis.
2. A nonlinear disturbance observer (NDO) based sliding mode controller (SMC) has been developed for the IFDBC to prevent the large-signal stabilities of both the IFDBC and DC bus voltage from being deteriorated by the CPLs.

Thanks to NDO's rapid and accurate estimations of the circuit uncertainties and output current, fast dynamic responses are achieved in presence of rapidly varying disturbances without using extra current sensor [30]. In addition, an inter-phase current balancing compensator is adopted to keep the current equally shared among different phases.

The rest of this paper is organized as follows. In Section II, a generalized model for the N-phase IFDBC is develpoed. Section III describes the design of the combined controller for the IFDBC system. In addtion, The large signal stability of the closed-loop system is demonstrated. Simulation and experimental results are given in Section IV and Section V, respectively, to show the effectiveness of proposed controller. Finally, conclusions are drawn in Section VI.

II. Generalized Model of Interleaved Floating Dual Boost Converter

A generic schematic of the DC MG fed by a N-phase IFDBC is shown in Fig. 1. As can be seen from the figure that plenty of DC and AC loads are indirectly fed by the IFDBC through the DC bus. Once these converters are tightly controlled, they behavior as CPLs. Such loads introduce severe nonlinearity and negative incremental impedance effect to the DC MG, which deteriorates the DC bus voltage stability [31]. To simply the system analysis, a lumped schematic of the DC MG fed by IFDBC is given in Fig. 2. Among this figure, V_{in} represents the input voltage of IFDBC, which is provided by the RESs; i_{Li} indicates the current flowing through the input side inductor L_i $(i = 1, 2, 3, ..., N)$; the total output voltage is defined as v_o. v_{c1} and v_{c2}, respectively, represent the voltages across C_1 and C_2. In addition, the resistive loads and CPLs are lumped and expressed as R_L and P_{CPL}, respectively.

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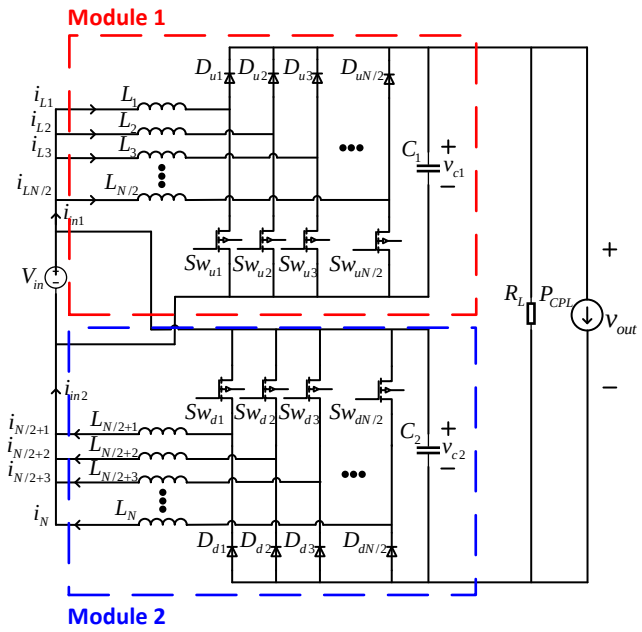

Fig. 2. Simplified schematic of the DC microgrid fed by an N-phase IFDBC

A. Reduced-Order Averaged State-Space Model

Using Kirchhoff's laws and model averaging technique, the averaged model of Module 1 shown in Fig. 2 can be derived as,

$$\begin{aligned} L_i \tfrac{di_{Li}}{dt} &= V_{in} - (1-u_i)\, v_{c1} \\ C_1 \tfrac{dv_{c1}}{dt} &= \sum_{i=1}^{N/2} i_{Li}\,(1-u_i) - i_{out} \end{aligned} \tag{1}$$

where $i_{out} = (v_{out}/R_L + P_{CPL}/v_{out})$ is the converter output current, and u_i $(i = 1, 2 \ldots N/2)$ indicates the duty ratio of the ith phase of the IFDBC.

Assuming that the inductors in different phases possess the same inductance due to system symmetry [10], and using identical duty ratio ($u_i = u_{m1}$ for $i = 1, 2 \ldots N/2$) with appropriate phase shifts to generate PWM switching signal for each phase, a generalized reduced-order model of the Module 1 of the N-phase IFDBC can be derived from (1) as,

$$\begin{aligned} L_{eq} \tfrac{di_{in1}}{dt} &= [V_{in} - (1-u_{m1})\, v_{c1}] \\ C_1 \tfrac{dv_{c1}}{dt} &= i_{in1}\,(1-u_{m1}) - i_{out} \end{aligned} \tag{2}$$

where $i_{in1} = \sum_{i=1}^{N/2} i_{Li}$ is the total input current of Module 1 and $L_{eq} = 2L/N$ is the equivalent input side inductance.

Similarly, the generalized reduced-order model of Module 2 can be derived as,

$$\begin{aligned} L_{eq} \tfrac{di_{in2}}{dt} &= [V_{in} - (1-u_{m2})\, v_{c2}] \\ C_2 \tfrac{dv_{c2}}{dt} &= i_{in2}\,(1-u_{m2}) - i_{out} \end{aligned} \tag{3}$$

where $i_{in2} = \sum_{i=N/2+1}^{N} i_{Li}$ is the total input current of Module 2 and $u_i = u_{m2}$ for $i = \frac{N}{2}+1, \frac{N}{2}+2 \ldots N$.

Combining (2) and (3) and considering the circuit parameter uncertainties, the generalized reduced-order model of the N-phase IFDBC can be obtained as,

$$\begin{aligned} (L_{eq} + \Delta L_1)\, \tfrac{di_{in1}}{dt} &= [V_{in} - (1-u_{m1})\, v_{c1}] \\ (L_{eq} + \Delta L_2)\, \tfrac{di_{in2}}{dt} &= [V_{in} - (1-u_{m2})\, v_{c2}] \\ (C_1 + \Delta C_1)\, \tfrac{dv_{c1}}{dt} &= i_{in1}\,(1-u_{m1}) - i_{out} \\ (C_2 + \Delta C_2)\, \tfrac{dv_{c2}}{dt} &= i_{in2}\,(1-u_{m2}) - i_{out} \end{aligned} \tag{4}$$

where ΔL_1, ΔL_2, ΔC_1 and ΔC_2 are the uncertainties in inductance and capacitance, respectively.

According to [10], the following relation can be derived,

$$v_{out} = v_{c1} + v_{c2} - V_{in} \tag{5}$$

Hence, the main control objective is to regulate the voltage of each module (v_{c1} and v_{c2}), individually, to achieve $v_{out} = V_{ref}$. Then the desired converter total output voltage (DC bus voltage) can be obtained as,

$$V_{ref} = 2V_{cref} - V_{in} \tag{6}$$

where V_{cref} $(V_{cref} = (V_{ref} + V_{in})/2)$ represents the desired steady-state value of the capacitor voltages v_{c1} and v_{c2}, which is determined by V_{ref} and V_{in}.

III. Controller Design

In this section, an NDO based SMC is designed for the N-phase IFDBC with CPL to ensure the DC bus voltage v_{out} tracks its reference value V_{ref} even in presences of large signal disturbances.

A. Canonical form transformation

Motivated by [32], to design the NDO based SMC to regulate the IFDBC system, the proposed model given in (4) is transferred into a linear canonical form first. To obtain the linear canonical system model, according to the work in [31], [33], a new set of state variables which can describe the IFDBC systems is given as,

$$\begin{aligned} x_1 &= \tfrac{1}{2} L_{eq} i_{in1}^2 + \tfrac{1}{2} C_1 v_{c1}^2 \\ x_2 &= V_{in} i_{in1} \\ x_3 &= \tfrac{1}{2} L_{eq} i_{in2}^2 + \tfrac{1}{2} C_2 v_{c2}^2 \\ x_4 &= V_{in} i_{in2} \end{aligned} \tag{7}$$

where x_1 and x_3 represent the total energy stored in the Module 1 and Module 2 in the IFDBC, respectively, and x_2 and x_4 stand for the input power of Module 1 and Module 2 in the IFDBC, respectively.

Using (7), the time derivative of the new state variables can be obtained as,

$$\begin{cases} \dot{x}_1 = L_{eq} i_{in1} \dot{i}_{in1} + C_1 v_{c1} \dot{v}_{c1} \\ \dot{x}_2 = V_{in} \dot{i}_{in1} \\ \dot{x}_3 = L_{eq} i_{in2} \dot{i}_{in2} + C_2 v_{c2} \dot{v}_{c2} \\ \dot{x}_4 = V_{in} \dot{i}_{in2} \end{cases} \tag{8}$$

Substituting (4) into (8) yields (9) which is given at the bottom of next page. Then, by expressing,

$$\begin{aligned} d_1 = -v_{c1} i_{out} &- \frac{\Delta L_1 i_{in1}}{L_{eq} + \Delta L_1} [V_{in} - (1-u_{m1})\, v_{c1}] \\ &- \frac{\Delta C_1 v_{c1}}{C_1 + \Delta C_1} [i_{in1}\,(1-u_{m1}) - i_{out}] \end{aligned}$$

$$d_2 = \frac{-V_{in}\Delta L_1}{L_{eq}\left(L_{eq}+\Delta L_1\right)}\left[V_{in}-\left(1-u_{m1}\right)v_{c1}\right]$$

$$\begin{aligned} d_3 = -v_{c2}i_{out} &- \frac{\Delta L_2 i_{in2}}{L_{eq}+\Delta L_2}\left[V_{in}-\left(1-u_{m2}\right)v_{c2}\right] \\ &- \frac{\Delta C_2 v_{c2}}{C_2+\Delta C_2}\left[i_{in2}\left(1-u_{m2}\right)-i_{out}\right] \end{aligned} \quad (10)$$

$$d_4 = \frac{-V_{in}\Delta L_2}{L_{eq}\left(L_{eq}+\Delta L_2\right)}\left[V_{in}-\left(1-u_{m2}\right)v_{c2}\right]$$

$$k_1 = \frac{V_{in}^2}{L_{eq}} - \frac{\left(1-u_{m1}\right)V_{in}v_{c1}}{L_{eq}}$$

$$k_2 = \frac{V_{in}^2}{L_{eq}} - \frac{\left(1-u_{m2}\right)V_{in}v_{c2}}{L_{eq}}$$

the state-variable dynamics (9) can be rewritten as,

$$\begin{aligned} \dot{x}_1 &= x_2 + d_1 \\ \dot{x}_2 &= k_1 + d_2 \\ \dot{x}_3 &= x_3 + d_3 \\ \dot{x}_4 &= k_2 + d_4 \end{aligned} \quad (11)$$

where k_1 and k_2 are the virtual control laws for Module 1 and Module 2, respectively. It is noted that (11) is a diffeomorphism form of the reduced-order model given in (4).

Based on the operation mechanism of the IFDBC [10], it is easy to obtained that, as compared to the values of module output power $v_{c1}i_{out}$ and $v_{c3}i_{out}$, those of $\left[V_{in}-\left(1-u_{m1}\right)v_{c1}\right]$, $\left[V_{in}-\left(1-u_{m2}\right)v_{c2}\right]$, $\left[i_{in1}\left(1-u_{m1}\right)-i_{out}\right]$ and $\left[i_{in2}\left(1-u_{m2}\right)-i_{out}\right]$ are quite small. Hence, the disturbances d_1 and d_3 can be reasonably simplified as,

$$\begin{aligned} d_1 &= -v_{c1}i_{out} \\ d_3 &= -v_{c3}i_{out} \end{aligned} \quad (12)$$

Using (10), the actual control laws u_{m1} and u_{m2} are derived as,

$$u_{m1} = 1 - \frac{V_{in}^2 - L_{eq}k_1}{V_{in}v_{c1}} \quad (13)$$

$$u_{m2} = 1 - \frac{V_{in}^2 - L_{eq}k_2}{V_{in}v_{c2}} \quad (14)$$

After the diffeomorphism coordinate transformation, the main control objective of driving v_{out} to track V_{ref} is transformed to driving stored energies x_1 and x_3 to converge to their corresponding reference value x_{1ref} and x_{3ref} asymptotically. The expressions of x_{1ref} to x_{4ref} are given as,

$$\begin{aligned} x_{1ref} &= \tfrac{1}{2}L_{eq}I_{ref1}^2 + \tfrac{1}{2}C_1V_{cref}^2 \\ x_{2ref} &= V_{in}I_{ref1} \\ x_{3ref} &= \tfrac{1}{2}L_{eq}I_{ref2}^2 + \tfrac{1}{2}C_2V_{cref}^2 \\ x_{4ref} &= V_{in}I_{ref2} \end{aligned} \quad (15)$$

where x_{2ref} and x_{4ref} are the reference values of x_2 and x_4, respectively, and I_{ref1} and I_{ref2} denotes the references of the i_{in1} and i_{in2}.

Considering the input/output power balance, I_{ref1} and I_{ref2} can be derived as,

$$I_{ref1} = I_{ref2} = \frac{V_{cref}I_{out}}{V_{in}} \quad (16)$$

where I_{out} represents the total output current at steady-state.

It is worth noting that the disturbance terms d_i $(i \in \{1,2,3,4\})$ are strongly related to the converter output current and physical system uncertainties. Therefore, taking the practical situation into account, these disturbances and their derivatives are bounded. Considering the above-mentioned situation, the following assumption can be made,

Assumption 1: The disturbance term d_i and its derivative $\dot{d}_i$ are bounded and defined by,

$$d_{i\max} = \sup_{t>0}\left|d_i\left(t\right)\right|, \bar{d}_{i\max} = \sup_{t>0}\left|\dot{d}_i\left(t\right)\right|, i \in \{1,2,3,4\}$$

B. Traditional SMC design

In this subsection, an SMC for the N-phase IFDBC system is proposed. Since there exist two control laws in the model given in (11), considering (11) and (15), two independent sliding surfaces are designed as,

$$s_1 = a_1e_{x1} + e_{x2} - \dot{x}_{1ref} \quad (17)$$

$$s_2 = a_2e_{x3} + e_{x4} - \dot{x}_{3ref} \quad (18)$$

where $e_{xi} = x_i - x_{iref}$ for $(i \in \{1,2,3,4\})$ are defined as the state errors; $\dot{x}_{jref}$ denotes the derivative of x_{jref} for $(j \in \{1,3\})$; $a_1 > 0$ and $a_2 > 0$ are user defined controller gains.

According to (15) and (16), all the references of the state variables are related to the steady-state load current I_{out}. However, since I_{out} is determined by the system loads which's information is usually difficult to be obtained, the actual value of the references x_{jref} for $(j \in \{1,2,3,4\})$ are unknown in many cases. Hence, here, the nominal values of x_{jref} $(j \in \{1,2,3,4\})$, which are constants, are used to design the sliding surface (17) and (18), and the derivatives of x_{jref} are zero.

Using (11), the derivative of the sliding surface s_1 can be obtained as,

$$\dot{s}_1 = k_1 + a_1\left(x_2 + d_1\right) + d_2 \quad (19)$$

$$\begin{cases} \dot{x}_1 = V_{in}i_{in1} - v_{c1}i_{out} - \frac{\Delta L_1 i_{in1}}{L_{eq}+\Delta L_1}\left[V_{in}-\left(1-u_{m1}\right)v_{c1}\right] - \frac{\Delta C_1 v_{c1}}{C_1+\Delta C_1}\left[i_{in1}\left(1-u_{m1}\right)-i_{out}\right] \\ \dot{x}_2 = \frac{V_{in}}{L_{eq}}\left[V_{in}-v_{c1}\left(1-u_{m1}\right)\right] - \frac{V_{in}\Delta L_1}{L_{eq}\left(L_{eq}+\Delta L_1\right)}\left[V_{in}-\left(1-u_{m1}\right)v_{c1}\right] \\ \dot{x}_3 = V_{in}i_{in2} - v_{c2}i_{out} - \frac{\Delta L_2 i_{in2}}{L_{eq}+\Delta L_2}\left[V_{in}-\left(1-u_{m2}\right)v_{c2}\right] - \frac{\Delta C_2 v_{c2}}{C_2+\Delta C_2}\left[i_{in2}\left(1-u_{m2}\right)-i_{out}\right] \\ \dot{x}_4 = \frac{V_{in}}{L_{eq}}\left[V_{in}-v_{c2}\left(1-u_{m2}\right)\right] - \frac{V_{in}\Delta L_2}{L_{eq}\left(L_{eq}+\Delta L_2\right)}\left[V_{in}-\left(1-u_{m2}\right)v_{c2}\right] \end{cases} \quad (9)$$

Letting $k_1 = -a_1 x_2 - K_{s1}\mathrm{sgn}(s_1) - K_{s2}s_1$, Eq. (19) can be rewritten as,

$$\dot{s}_1 = a_1 d_1 + d_2 - K_{s1}\mathrm{sgn}(s_1) - K_{s2}s_1 \tag{20}$$

Similarly, by designing the control law $k_2 = -a_2 x_4 - K_{s3}\mathrm{sgn}(s_2) - K_{s4}s_2$, the derivative of s_2 can be derived as,

$$\dot{s}_2 = a_2 d_3 + d_4 - K_{s3}\mathrm{sgn}(s_2) - K_{s4}s_2 \tag{21}$$

Defining a candidate Lyapunov function as,

$$V_s(s_1, s_2) = \frac{1}{2}s_1^2 + \frac{1}{2}s_2^2 \tag{22}$$

then, using (20) and (21), the time derivation of V_s can be obtained as (23) which is given at the bottom of next page.

Hence, with the conditions of $(K_{s1} + K_{s2}|s_1|) > (a_1 d_{1\max} + d_{2\max})$ and $(K_{s3} + K_{s4}|s_2|) > (a_2 d_{3\max} + d_{4\max})$, it can be obtained that the system state errors $e_{xi} (i \in \{1,2,3,4\})$ will asymptotically converge to the sliding surface $s_1 = 0$ and $s_2 = 0$, respectively.

According to (17) and (18), $s_1 = 0$ and $s_2 = 0$ yields,

$$e_{x2} = -a_1 e_{x1} \tag{24}$$

$$e_{x4} = -a_2 e_{x3} \tag{25}$$

Considering (11), (24), (25) and definitions of $e_{xi} (i \in \{1,2,3,4\})$, the resulting ideal sliding-mode dynamics can be expressed as,

$$\dot{e}_{x1} = -a_1 e_{x1} + d_1 + x_{2ref} \tag{26}$$

$$\dot{e}_{x3} = -a_2 e_{x3} + d_3 + x_{4ref} \tag{27}$$

Eqs. (26) and (27) indicate that the state errors e_{x1} and e_{x3} can converge to their desired equilibrium point if and only if $d_1 + x_{2ref} = 0$ and $d_3 + x_{4ref} = 0$, respectively. However, the mismatched disturbance d_1 and d_3 are varying and hard to be detected, and, as mentioned previously, both the references x_{2ref} and x_{4ref} are constants, which are calculated using the nominal value the circuit parameters. Therefore, it is impossible to ensure $d_1 + x_{2ref} = 0$ and $d_3 + x_{4ref} = 0$ all the time. As such, the steady-state error in the DC bus voltage is inevitable.

Remark I: Based on (26) and (27), although extremely large of a_1 and a_2 can make the DC steady state error in bus voltage negligibly small, those may also dissatisfy the conditions of $(K_{s1} + K_{s2}|s_1|) > (a_1 d_{1\max} + d_{2\max})$ and $(K_{s3} + K_{s4}|s_2|) > (a_2 d_{3\max} + d_{4\max})$, and further destabilize the whole system.

Due to the lack of knowledge of the disturbances and circuit parameter uncertainties, the traditional SMC cannot ensure the state errors converge to their desired equilibrium point although all the state errors reach the designed sliding surface. To fill this gap, a controller combined with the sliding-mode technique and the disturbance observe technique is designed in next subsection.

C. NDO based SMC design

Based on (12), the instantaneous value of load current i_{out} can be obtained using the disturbances d_1 and d_3. Hence, the actual value of the references x_{iref} for $(i \in \{1,2,3,4\})$ can be calculated as long as the disturbance d_1 and d_3 can be accurately estimated. In addition, according to (11), the disturbances d_i $(i \in \{1,2,3,4\})$ also affects the system dynamics of the IFDBC system. To overcome the drawback of the pure SMC and achieve desired system dynamics and tight system output tracking, the NDO technique is adopted.

According to [30], [32], the NDOs to estimate each disturbance can be described as,

$$\begin{cases} \hat{d}_1 = K_{d1}x_1 + \beta_1 \\ \dot{\beta}_1 = -K_{d1}\left(x_2 + \hat{d}_1\right) \end{cases} \tag{28}$$

$$\begin{cases} \hat{d}_2 = K_{d2}x_2 + \beta_2 \\ \dot{\beta}_2 = -K_{d2}\left(k_1 + \hat{d}_2\right) \end{cases} \tag{29}$$

$$\begin{cases} \hat{d}_3 = K_{d3}x_3 + \beta_3 \\ \dot{\beta}_3 = -K_{d3}\left(x_4 + \hat{d}_3\right) \end{cases} \tag{30}$$

$$\begin{cases} \hat{d}_4 = K_{d4}x_4 + \beta_4 \\ \dot{\beta}_4 = -K_{d4}\left(k_2 + \hat{d}_4\right) \end{cases} \tag{31}$$

where $\hat{d}_i$ represents the disturbance estimator of d_i, K_{di} denotes the user defined positive observer gain and β_i are the observer internal variable state $(i \in \{1,2,3,4\})$.

Using (28) - (31), the NDOs' error dynamics are derived as,

$$\begin{aligned} \dot{e}_{d1} &= -K_{d1}e_{d1} + \dot{d}_1 \\ \dot{e}_{d2} &= -K_{d2}e_{d2} + \dot{d}_2 \\ \dot{e}_{d3} &= -K_{d3}e_{d3} + \dot{d}_3 \\ \dot{e}_{d4} &= -K_{d4}e_{d4} + \dot{d}_4 \end{aligned} \tag{32}$$

where $e_{di} = d_i - \hat{d}_i$ $(i \in \{1,2,3,4\})$ are the estimation errors.

Considering an energy function as,

$$V_{es}(e_{d1}, e_{d2}, e_{d3}, e_{d4}) = \frac{1}{2}\sum_{i=1}^{4} e_{di}^2 \tag{33}$$

Using Assumption 1 and (32), the derivative of V_{es} can be given by,

$$\begin{aligned} \dot{V}_{es}(e_{di}) &= \sum_{i=1}^{4}\left(-K_{di}e_{di}^2 + e_{di}\dot{d}_i\right) \\ &\le \sum_{i=1}^{4}\left(-K_{di}|e_{di}|^2 + |e_{di}|\,\bar{d}_{i\max}\right) \\ &= -\sum_{i=1}^{4}|e_{di}|\left(K_{di}|e_{di}| - \bar{d}_{i\max}\right) \end{aligned} \tag{34}$$

Thus, after a finite time, the estimation errors are bounded by,

$$|e_{di}| \le \kappa_d \tag{35}$$

where $\kappa_d = \max\left(\bar{d}_{i\max}/K_{di}\right)$ for $i \in \{1,2,3,4\}$.

Since the exact value of the total output current I_{out} is not available in most practical cases, to implement the controller, based on (12), (15) and (16), the estimated state variables'

references are given as,

$$\begin{aligned}\hat{x}_{1ref} &= \tfrac{1}{2}L_{eq}\tfrac{\hat{d}_1^2}{{V_{in}}^2} + \tfrac{1}{2}C_1V_{cref}^2\\ \hat{x}_{2ref} &= -\hat{d}_1\\ \hat{x}_{3ref} &= \tfrac{1}{2}L_{eq}\tfrac{\hat{d}_3^2}{{V_{in}}^2} + \tfrac{1}{2}C_2V_{cref}^2\\ \hat{x}_{4ref} &= -\hat{d}_3\end{aligned} \tag{36}$$

where $\hat{x}_{iref}$ is the estimation of x_{iref} $((i \in \{1,2,3,4\}))$.

Using the estimated references given in (36), the sliding surfaces given in (17) - (18) are re-designed as,

$$s_1 = a_1e_{x1} + e_{x2} - \dot{\hat{x}}_{1ref} \tag{37}$$

$$s_2 = a_2e_{x3} + e_{x4} - \dot{\hat{x}}_{3ref} \tag{38}$$

where $e_{xi} = x_i - \hat{x}_{iref}$ for $(i \in \{1,2,3,4\})$ are defined as the state errors and $\dot{\hat{x}}_{jref}$ denotes the derivative of $\hat{x}_{jref}$ for $(j \in \{1,3\})$.

To ensure the sliding surfaces s_1 and s_2 converge to zero, following control laws are designed,

$$\begin{aligned}k_1 = -a_1\left(e_{x2} - \dot{\hat{x}}_{1ref}\right) + \ddot{\hat{x}}_{1ref} - \dot{\hat{d}}_1 - \hat{d}_2\\ - K_{s1}\mathrm{sgn}\left(s_1\right) - K_{s2}s_1\end{aligned} \tag{39}$$

$$\begin{aligned}k_2 = -a_2\left(e_{x4} - \dot{\hat{x}}_{3ref}\right) + \ddot{\hat{x}}_{3ref} - \dot{\hat{d}}_3 - \hat{d}_4\\ - K_{s3}\mathrm{sgn}\left(s_2\right) - K_{s4}s_2\end{aligned} \tag{40}$$

where K_{si} $(i \in \{1,2,3,4\})$ are user designed positive sliding-mode control gains.

D. System stability analysis

Considering the NDO based SMC design in last section, the main proposition of this paper is carried out.

Proposition 1: With Assumption 1, the N-phase IFDBC system, described by (4) and (11), regulated by the proposed control laws (13) and (14), is asymptotically stable, and the MG DC bus voltage tracks its reference V_{ref} asymptotically, if the sliding-mode control gains K_{s1}, K_{s2}, K_{s3} and K_{s4} are designed to satisfy $(K_{s1} + K_{s2}\left|s_1\right|) > (1+a_1)\kappa_d$ and $(K_{s3}+K_{s4}\left|s_2\right|) > (1+a_2)\kappa_d$, respectively, and large enough K_{min} is selected.

Proof: Using (11), (32) and (36), the derivative of the sliding surface s_1 is yielded as,

$$\begin{aligned}\dot{s}_1 = k_1 - \ddot{\hat{x}}_{1ref} + \dot{\hat{d}}_1 + d_2\\ + a_1\left(e_{x2} + \hat{x}_{2ref} - \dot{\hat{x}}_{1ref} + d_1\right)\end{aligned} \tag{41}$$

Substituting control law k_1 given in (39) into (41) yields,

$$\dot{s}_1 = a_1e_{d1} + e_{d2} - K_{s1}\mathrm{sgn}\left(s_1\right) - K_{s2}s_1 \tag{42}$$

Similarly, by using (40), the derivative of s_2 can be rewritten as,

$$\dot{s}_2 = a_2e_{d3} + e_{d4} - K_{s3}\mathrm{sgn}\left(s_2\right) - K_{s4}s_2 \tag{43}$$

Defining a candidate Lyapunov function as,

$$V_s(s_1,s_2) = \frac{1}{2}{s_1}^2 + \frac{1}{2}{s_2}^2 \tag{44}$$

The derivative of $V_s\left(s_1,s_2\right)$ is given at the bottom of next page (see (45)). Since there exist the conditions of $(K_{s1} + K_{s2}\left|s_1\right|) > (1+a_1)\kappa_d$ and $(K_{s3} + K_{s4}\left|s_2\right|) > (1+a_2)\kappa_d$, according to [34] and (35), system state errors will asymptotically converge to the defined sliding surface $s_1 = 0$ and $s_2 = 0$.

Remark II: Since the value of κ_d can be arbitrarily small with sufficiently large K_{di}, relatively small values of K_{si} $(i = 1,2,3,4)$ can be adopted, which alleviates the sliding-mode chattering problem.

Based on (37) and (38), $s_1 = 0$ and $s_2 = 0$ result in,

$$e_{x2} = -a_1e_{x1} + \dot{\hat{x}}_{1ref} \tag{46}$$

$$e_{x4} = -a_2e_{x3} + \dot{\hat{x}}_{3ref} \tag{47}$$

Considering the definitions of $e_{xi}(i = 1,2,3,4)$, e_{d1}, e_{d3}, $\hat{x}_{2ref}$ and $\hat{x}_{4ref}$, the dynamics of e_{x1} and e_{x3} can be derived from (11) as,

$$\dot{e}_{x1} = e_{x2} + e_{d1} - \dot{\hat{x}}_{1ref} \tag{48}$$

$$\dot{e}_{x3} = e_{x4} + e_{d3} - \dot{\hat{x}}_{3ref} \tag{49}$$

Substituting (46) and (47) into (48) and (49), respectively, and combining the observer error dynamics given in (32) yields the NDO based sliding dynamics of the regulated system as,

$$\dot{e} = \mathbf{A}e + \mathbf{B}\dot{d} \tag{50}$$

where $\dot{e}=[\dot{e}_{x1},\dot{e}_{d1},\dot{e}_{d2},\dot{e}_{x3},\dot{e}_{d3},\dot{e}_{d4}]^T$ and $\dot{d} = [\dot{d}_1,\dot{d}_2,\dot{d}_3,\dot{d}_4]^T$; $\mathbf{A}$ and $\mathbf{B}$ are coefficient matrix given by,

$$\mathbf{A} = \begin{bmatrix} -a_1 & 1 & 0 & 0 & 0 & 0\\ 0 & -K_{d1} & 0 & 0 & 0 & 0\\ 0 & 0 & -K_{d2} & 0 & 0 & 0\\ 0 & 0 & 0 & -a_2 & 1 & 0\\ 0 & 0 & 0 & 0 & -K_{d3} & 0\\ 0 & 0 & 0 & 0 & 0 & -K_{d4}\end{bmatrix}$$

$$\begin{aligned}\dot{V}_s &= s_1\dot{s}_1 + s_2\dot{s}_2\\ &= -K_{s1}\left|s_1\right| - K_{s2}s_1^2 + \left(a_1d_1 + d_2\right)s_1 - K_{s3}\left|s_2\right| - K_{s4}s_2^2 + \left(a_2d_3 + d_4\right)s_2\\ &\le -\left[K_{s1} + K_{s2}\left|s_1\right| - \left(a_1d_{1\max} + d_{2\max}\right)\right]\left|s_1\right| - \left[K_{s3} + K_{s4}\left|s_2\right| - \left(a_2d_{3\max} + d_{4\max}\right)\right]\left|s_2\right|\end{aligned} \tag{23}$$

$$\mathbf{B} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix}$$

Defining a Lyapunov function as,

$$V_e(e) = V_{es} + \frac{1}{2}e_{x1}^2 + \frac{1}{2}e_{x3}^2 \tag{51}$$

Using (50) and (34), the derivative of V_e with respect to time can be calculated as,

$$\begin{aligned} \dot{V}_e &= \dot{V}_{es} + e_{x1}\dot{e}_{x1} + e_{x3}\dot{e}_{x3} \\ &= \dot{V}_{es} + \left(-a_1 e_{x1}^2 + e_{x1}e_{d1}\right) + \left(-a_2 e_{x3}^2 + e_{x3}e_{d3}\right) \\ &= \sum_{i=1}^{4}\left(-K_{di}e_{di}^2 + e_{di}\dot{d}_i\right) + \left(-a_1 e_{x1}^2 + e_{x1}e_{d1}\right) + \\ &\left(-a_2 e_{x3}^2 + e_{x3}e_{d3}\right) \end{aligned} \tag{52}$$

Using Young's Inequality [35] and (52) yields an inequality as,

$$\begin{aligned} \dot{V}_e \le &-\left(K_{d1}-1\right)e_{d1}^2 - K_{d2}e_{d2}^2 - \left(K_{d3}-1\right)e_{d3}^2 - K_{d4}e_{d4}^2 \\ &-\left(a_1-0.5\right)e_{x1}^2 - \left(a_2-0.5\right)e_{x3}^2 + 0.5\sum_{i=1}^{4}\dot{d}_i \end{aligned} \tag{53}$$

Considering Assumption 1 and (51), Eq. (53) can be re-scaled as,

$$\dot{V}_e \le -K_{\min}V_e + 2\bar{d}_{\max} \tag{54}$$

where $K_{\min} = \min[2\left(K_{d1}-1\right), 2K_{d2}, 2\left(K_{d3}-1\right), 2K_{d4}, 2\left(a_1-0.5\right), 2\left(a_2-0.5\right)] > 0$ and $\bar{d}_{\max} = \max[\bar{d}_{1\max}, \bar{d}_{2\max}, \bar{d}_{3\max}, \bar{d}_{4\max}]$.

According to (54), it is understandable that within a finite time such that the value of V_e is bounded by,

$$V_e \le \varepsilon \tag{55}$$

where $\varepsilon = 2\bar{d}_{\max}/K_{\min}$.

Through selecting a sufficiently large $K_{\min}$, ε can be arbitrarily small and nearly zero. Consequently, the error vector e given in (50) can asymptotically converge to the arbitrarily small neighbourhood of the origin. This indicates that, in practice, both the output capacitor voltages v_{c1} and v_{c2} can be regulated to their reference value V_{cref} with nearly zero steady-state errors and, therefore, the DC bus voltage v_{out} tracks its desired value V_{ref} asymptotically [36].

Remark III: The process of generating the converter output reference V_{ref} is not a part of the proof of the system large-signal stability. Hence, once the reference V_{ref} is given, the proposed controller is able to regulate the DC bus voltage to V_{ref}. As such, the droop control technique can be adopted to the IFDBC system with the proposed controller to achieve proper converter output voltage according to the grid side power variations. Moreover, the power sharing between the IFDBC and other source converters also can be implemented using the droop control technique [37], [38]. As mentioned previously, the proposed NDO based SMC will respond the reference V_{ref} obtained from the droop controller rapidly without compromising the large signal stability of the IFDBC system and the DC bus voltage.

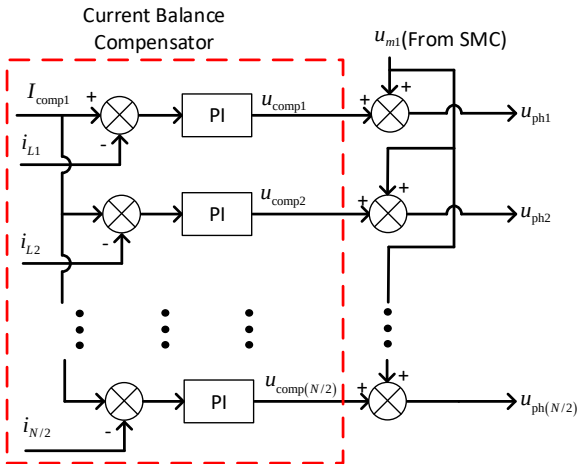

Fig. 3. Schematic of phase current balance compensator for Module 1

E. Phase current balance compensator

Thanks to the symmetrical system structure, the generalized reduced-order model (4) is developed to simplify the controller design for the IFDBC as shown in the last section. However, by using (4), the total input current of a module, instead of the current of each phase, becomes the state variable to be regulated. As a result, in practical implementations, interphase current imbalance will be caused by the unavoidable circuit parameters'deviations and the minor differences among the duty ratios of different phases. To fully explore the merits of the IFDBC, such as low current and voltage ripples as well as equal current sharing among multiple phases, the current balance compensators (CBCs) using PI control technique are applied to both modules. The CBC for Module 1 (see Fig. 2) is presented for the purpose of illustration. Its corresponding schematic is shown in Fig. 3. To make the phase current of each phase in Module 1 equal to each other, the current reference of the CBC is selected as $I_{comp1} = 2i_{in1}/N$. Then,

$$\begin{aligned} \dot{V}_s(s_1, s_2) &= s_1\dot{s}_1 + s_2\dot{s}_2 \\ &= -K_{s1}|s_1| - K_{s2}{s_1}^2 - K_{s3}|s_2| - K_{s4}{s_2}^2 + \left(a_1e_{d1} + e_{d2}\right)s_1 + \left(a_2e_{d3} + e_{d4}\right)s_2 \\ &\le -K_{s1}|s_1| - K_{s2}{s_1}^2 - K_{s3}|s_2| - K_{s4}{s_2}^2 + \left(1+a_1\right)\kappa_d s_1 + \left(1+a_2\right)\kappa_d s_2 \\ &= -\left[K_{s1} + K_{s2}|s_1| - (1+a_1)\kappa_d\right]|s_1| - \left[K_{s3} + K_{s4}|s_2| - \left(1+a_2\right)\kappa_d\right]|s_2| \end{aligned} \tag{45}$$

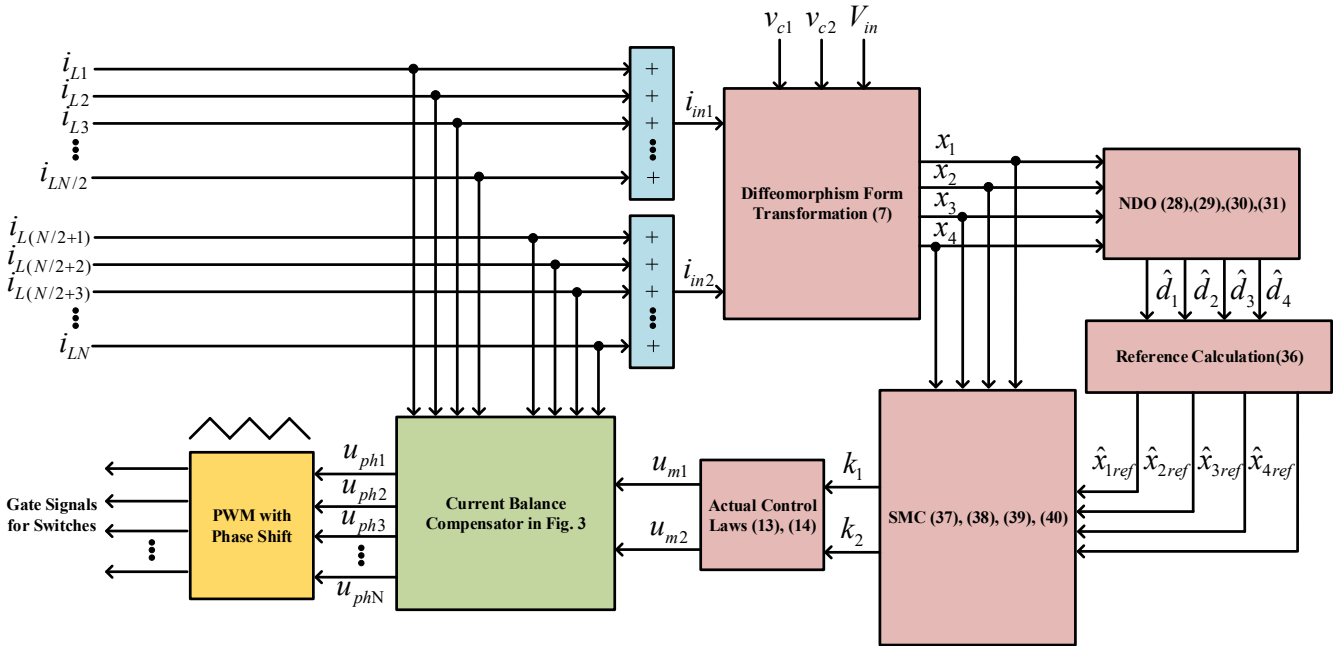

Fig. 4. Block diagram of the proposed controller for the N-phase IFDBC

the CBC for each phase in Module 1 can be designed as,

$$u_{\text{comp}i} = K_P e_{\text{comp}i} + K_I \int e_{\text{comp}i} dt \tag{56}$$

where $e_{\text{comp}i} = I_{\text{comp1}} - i_{Li}$ for $i \in \{1, 2, \ldots, N/2\}$; $K_P > 0$ and $K_I > 0$ are user defined compensator gains. It is noteworthy that selections of K_P and K_I are supposed to ensure the bandwidth of the CBC to be much smaller than that of the SMC proposed previously.

Adding the CBC's output to the control signal obtained from the proposed SMC yields the final phase control signal as,

$$u_{\text{ph}i} = u_{m1} + u_{\text{comp}i} \tag{57}$$

Due to the symmetric structure of IFDBO, the CBC design of Module 2 is the same as that of Module 1. For conciseness, the design process is not repeated here.

To make the paper more readable, the block diagram of the proposed controller is shown in Fig. 4.

IV. Simulation Results

To verify the effectiveness of the proposed controller for the IFDBC, some simulations using high power loads have been carried out in Matlab/Simulink. Among the simulations, the model of a 6-phase (N = 6) IFDBC is adopted. The simulation circuit parameters are given in Table I. Besides, to examine the performance of the proposed controller in worst stability conditions, pure CPL is considered in the simulations.

A. Tuning Guidelines

In Section III, it is indicated that if the observer gains and SMC gains are properly selected, the large-signal stability of the IFDBC powered DC mircogrid can be achieved. However, due to the lack of the tuning guidelines for the gains, the desired dynamic responses are difficult to obtained. To address this problem, the dynamic responses of the DC bus voltage and the estimator $\hat{d}_1$ with various observer gains and SMC gains are given in figs. 5 to 7, respectively. For simplicity, the observer gains K_{d1}, K_{d2}, K_{d3} and K_{d4} are set as the same, i.e. $K_{d1} = K_{d2} = K_{d3} = K_{d4}$, and the SMC gains $K_{s1} = K_{s3}$, $K_{s2} = K_{s4}$ and $a_1 = a_2$ are used.

In Fig. 5(a), the dynamic DC bus voltage responses with varying K_{s1} and K_{s3} in the presence of CPL power step change ($P_{CPL} = 30\text{kW}$ to $P_{CPL} = 45\text{kW}$ at $t = 0.1s$) are illustrated. It is worth mentioning that observer gains K_{di} $(i \in \{1, 2, 3, 4\})$ are initially selected as 2000, and the SMC gains $K_{s2} = K_{s4} = 1250$ and $a_1 = a_2 = 4000$ are selected. It can be seen that the values of the K_{s1} and K_{s3} do not have obvious effects on the DC bus voltage dynamic. Considering the K_{s1} and K_{s3} are switching gains, which causes the SMC chattering problem, small K_{s1} and K_{s3} are desired. Hence, $K_{s1} = K_{s3} = 0.1$ are selected.

In Fig. 5(b), the dynamic DC bus voltage responses with varying K_{s2} and K_{s4} in the presence of CPL power step change ($P_{CPL} = 30\text{kW}$ to $P_{CPL} = 45\text{kW}$ at $t = 0.1s$) are shown. Similarly, $K_{di} = 2000$ $(i \in \{1, 2, 3, 4\})$ is used, and $K_{s1} = K_{s3} = 0.1$ and $a_1 = a_2 = 4000$. It can be seen that the rise of K_{s2} and K_{s4} results in smaller voltage dip during the load power change. In addition, the settling time also reduces a bit (min. 10ms) with the increasing of K_{s2} and K_{s4}.

The DC bus voltage dynamic response with varying a_1 and a_2 in the presence of CPL power step change ($P_{CPL} = 30\text{kW}$ to $P_{CPL} = 45\text{kW}$ at $t = 0.1s$) are given in Fig. 5(c) In the simulations, $K_{s1} = K_{s3} = 0.1$ and $K_{s2} = K_{s4} = 20000$ are selected. It is viewed that the increased a_1 and a_2 further reduce the value of the voltage drop during the load power change. However, due to the condition of (45), extremely large

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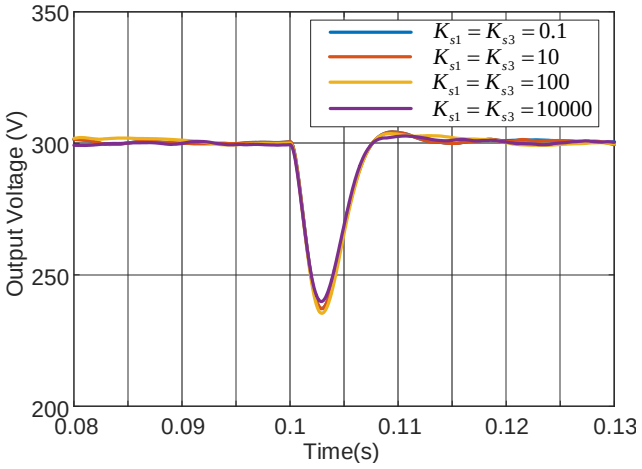
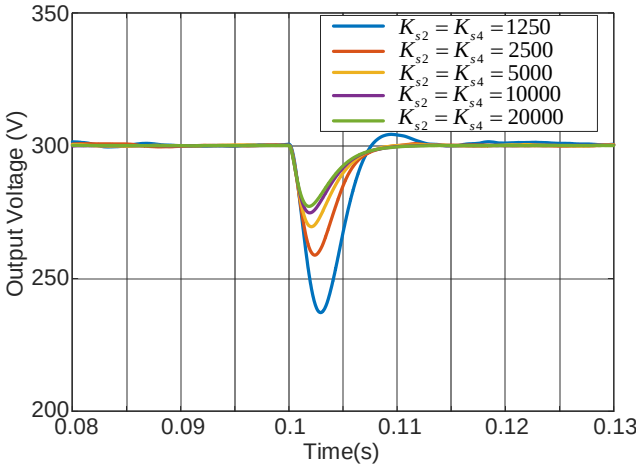
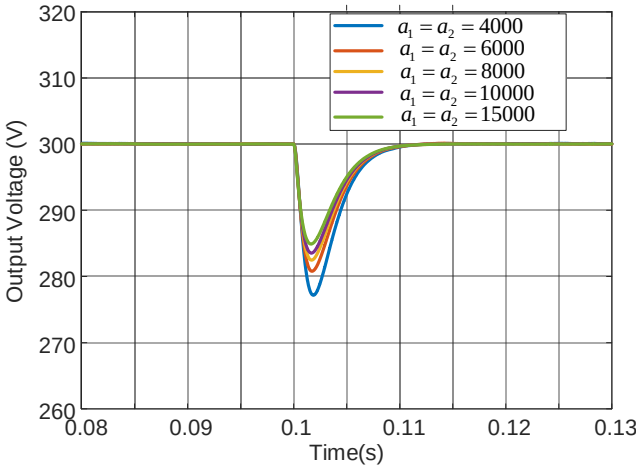


(a)



(b)



(c)

Fig. 5. Dynamic responses of the DC bus voltage: (a) with various K_{s1} and K_{s3}; (b) with various K_{s2} and K_{s4}; (c) with various a_1 and a_2.

a_1 and a_2 may destabilize the regulated converter system. Hence, based on Fig. 5(c), $a_1 = a_2 = 10000$ are selected.

With using $K_{s1} = K_{s3} = 0.1$, $K_{s2} = K_{s4} = 20000$ and $a_1 = a_2 = 10000$, the start-up response of the DC bus voltage with various K_{di} $(i \in \{1, 2, 3, 4\})$ is shown in Fig. 6. It can be easily obtained that the rises of the observer gains provide

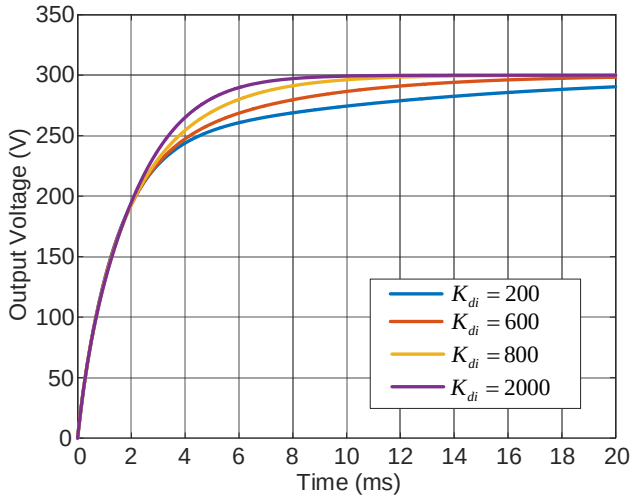


Fig. 6. Start-up responses of the DC bus voltage with various $K_{di}(i \in \{1, 2, 3, 4\})$.

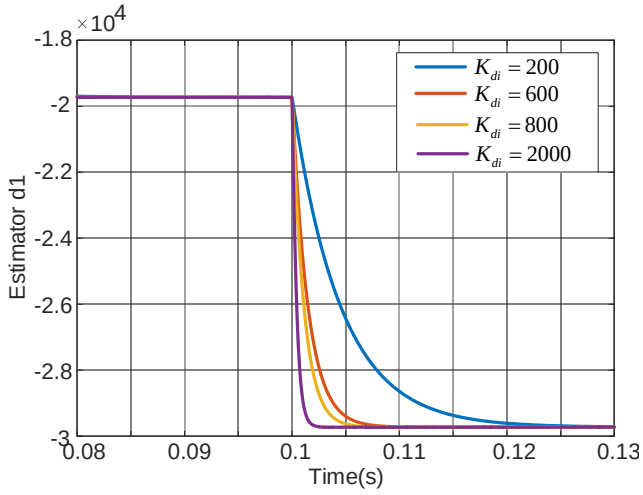


Fig. 7. Dynamics responses of the estimator $\hat{d}_1$ with various $K_{di}(i \in \{1, 2, 3, 4\})$

the DC bus voltage a faster start-up response. Specifically, at $K_{di} = 2000$, the DC bus voltage tracks its reference 300V within 10ms.

Using the same K_{si} $(i \in \{1, 2, 3, 4\})$, a_1 and a_2, the dynamic response of the estimator $\hat{d}_1$ with varying K_{di} $(i \in \{1, 2, 3, 4\})$ is illustrated in Fig. 7. It can be seen that the greater K_{di} provides the estimator $\hat{d}_1$ a faster convergence rate. Since the estimators obtained from the NDO are given to the SMC, it is desired that the dynamic response of the NDO is much faster than that of the SMC. From figs. 5(c), 6 and 7, it can be obtained that the settling time of the DC bus voltage in both the start-up response and transient response (around 10ms) is approximate 10 times of that of the observer (around 1ms) when $K_{di} = 2000$. Hence, the observer gain $K_{di} = 2000$ is selected.

B. The effectiveness of the NDO

To show the effectiveness of the NDO, a comparison study involves the traditional SMC (designed in Section III) and the

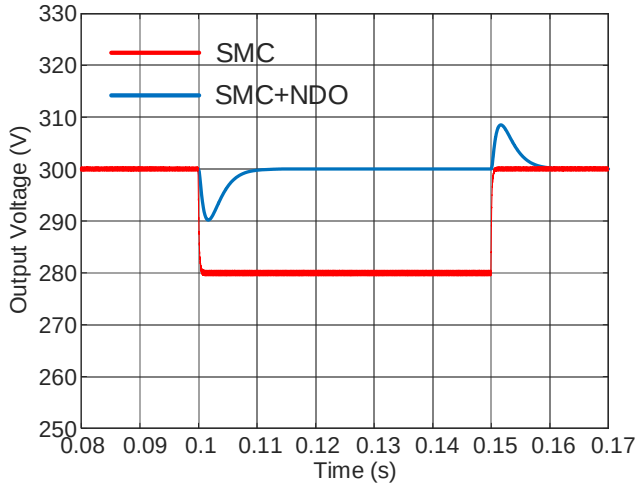


Fig. 8. DC bus voltage responses obtained using the proposed NDO based SMC (blue) and the traditional SMC (red).

TABLE I
SYSTEM PARAMETERS IN HIGH POWER SIMULATION

Circuit Parameters	Values
IFDBC input side voltage	$V_{in} = 100$V
DC bus reference voltage	$V_{ref} = 300$V
Module capacitor reference voltage	$V_{cref} = 200$V
Inductance of each inductor	$L_i = 330\mu$H
Output capacitance	$C_1 = C_2 = 1410\mu$F
Nominal Constant Power Load	$P_{CPL} = 30$kW
Switching frequency	$f_{sw} = 20$kHz

NDO based SMC has been carried out. Fig. 8 shows the DC bus voltage responses obtained using the IFDBC regulated by the proposed NDO based SMC (in blue) and the traditional SMC (in red) with the controller gains of $a_1 = a_2 = 10000$. In detail, the CPL changes from $P_{CPL} = 30kW$ to $P_{CPL} = 40kW$ at $t = 0.1s$, and restores to $P_{CPL} = 30kW$ at $t = 0.15s$. Although, in the traditional SMC design, the value of x_{2ref} and x_{4ref} are carefully selected to meet the conditions of $d_1 + x_{2ref} = 0$ and $d_3 + x_{4ref} = 0$ (see (26) and (27)) at $P_{CPL} = 30kW$, the step change of the P_{CPL} to $40kW$ drives the error states away from their desired equilibrium point. As a result, the DC bus voltage drops to 280V (93% of its reference 300V). This simulation result is highly in consist with the theoretical analysis given previously.

C. Tests with High Power CPL

Fig. 9 shows the system responses in presence of C-PL variations. The converter output voltage v_{out}, capacitor voltages of each module v_{c1}, v_{c2} and phase currents i_{Li} ($i \in \{1, 2, 3, 4, 5, 6\}$) are illustrated in the top sub-figure, the middle sub-figure and the bottom sub-figure, respectively. At $t = 0.1s$, the power of the load has a step change from $P_{CPL} = 30$kW to $P_{CPL} = 45$kW and then, P_{CPL} jumps to 60kW at $t = 0.15s$. It can be seen that the output voltage v_{out} restores to its reference value within 10ms with acceptable voltage dip (maximum 7% of the nominal output

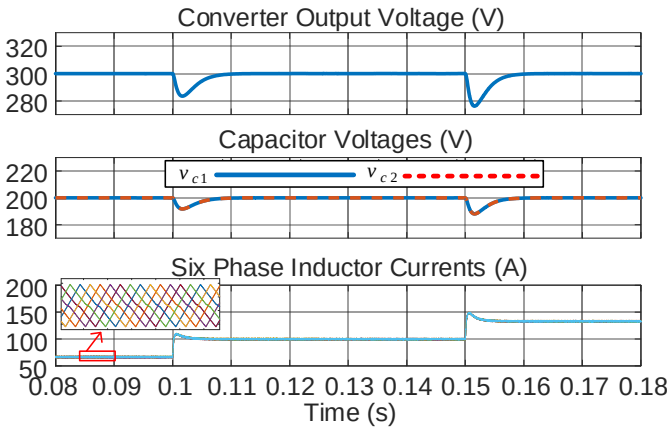


Fig. 9. Simulation system transient responses in the presence of CPL changes (Top: output voltage; Middle: module capacitor voltage; Bottom: current of six phases)

voltage 300V) and the capacitor voltage of each module also tightly tracks its reference with similar dynamics. Besides, the zoomed in current waveforms shown in the bottom sub-figure indicates that the six phase-currents, which are shifted by 60 degree, are in good balance. The 60 degree of phase-shifts significantly suppresses the input current ripple of both modules [10].

In Fig. 10, dynamic responses of the regulated system during input voltage variation has been illustrated. In detail, the input voltage changes from $V_{in} = 100$V to $V_{in} = 110$V at $t = 0.1s$, and then drops to 90V at $t = 0.15s$. At $t = 0.2s$, V_{in} restore to its nominal value $V_{in} = 100$V. From the figure, it can be seen that the output voltage is regulated to its reference 300V with reasonable overshoot (maximum 7% of 300V) and short settling time (maximum 5ms) during all the input voltage variations. Therefore, the proposed controller show good control robustness during the input voltage variations.

In Fig. 11, dynamic responses of the 6-phase IFDBC system in the presences of voltage reference change has been shown. Specifically, at $t = 0.1s$, the reference of the DC bus voltage V_{ref} jumps from 300V to 400V, and further steps up to 500V at $t = 0.15s$. It can be found that the DC bud voltage is regulated to its new reference with short settling time (around 5ms) and negligible voltage overshoot.

D. Circuit Parameter Uncertainties

Since the reduced-order model is derived based on the assumption of the equal phase inductance and equal output capacitor in each module, some simulations have been carried out to show the robustness of the proposed control strategy on handling the circuit parameter uncertainties. In the simulations, the $\pm 20\%$ deviations in inductance and $\pm 10\%$ deviations in capacitance are assumed. The percentage of the deviations are selected based on the practical engineering experience.

The DC bus voltage dynamic responses with 5 different sets of inductance and capacitance are shown in Fig. 12. At $t = 0.15s$, the CPL changes from 30kW to 45kW. It can be seen that the proposed controller provides almost the same voltage dynamic responses regardless the circuit parameter deviations.

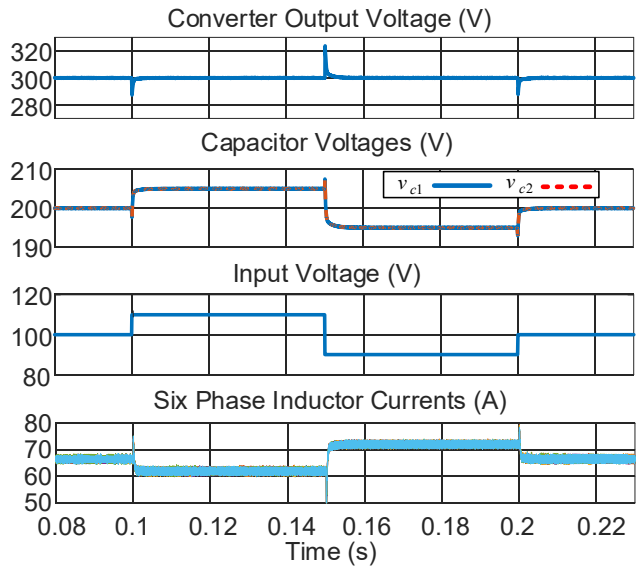


Fig. 10. Simulation system transient responses in the presences of input voltage changes (Top: output voltage; Second: module capacitor voltage; Third: input voltage; Bottom: current of six phases)

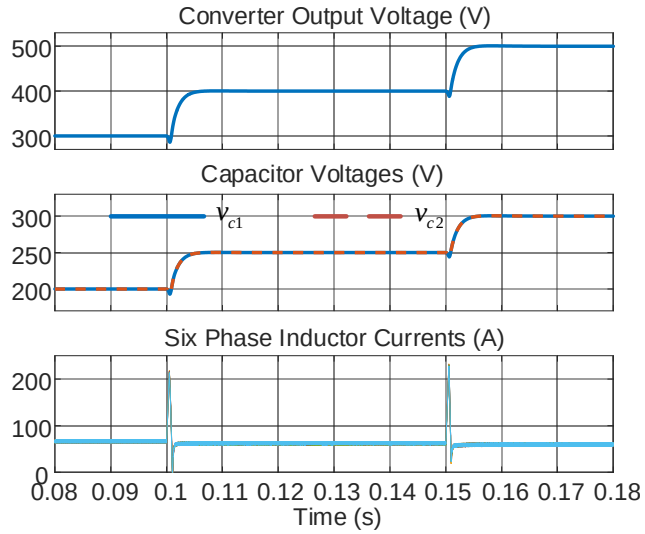


Fig. 11. Simulation system transient responses in the presences of voltage reference changes (Top: output voltage; Second: module capacitor voltage; Third: input voltage; Bottom: current of six phases)

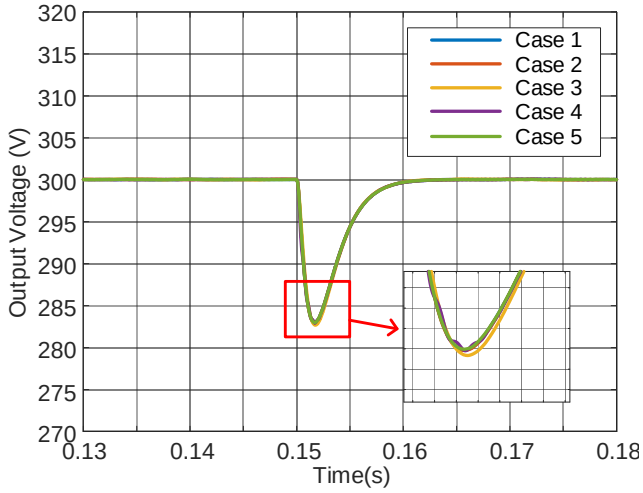


Fig. 12. DC bus voltage dynamic response with the circuit parameter uncertainties (case 1: $L_1 = L_3 = L_5 = 1.2L = 396\mu$H, $L_1 = L_3 = L_5 = 1.2L = 396\mu$H and $C_1 = C_2 = C = 1410\mu$F; case 2: $L_1 = L_3 = L_5 = 1.2L = 396\mu$H, $L_1 = L_3 = L_5 = 0.8L = 264\mu$H, $C_1 = 1.1C = 1551\mu$F and $C_2 = 0.9C = 1269\mu$F; case 3:$L_1 = L_2 = L_6 = 0.8L = 264\mu$H, $L_3 = L_4 = L_5 = 1.2L = 396\mu$H and $C_1 = C_2 = 1.1C = 1151\mu$F; case 4: $L_1 = L_2 = L_3 = 1.2L = 396\mu$H, $L_4 = L_5 = L_6 = 0.8L = 264\mu$F, $C_1 = 0.9C = 1269\mu$F and $C_2 = 1.1C = 1551\mu$F; case 5: $L_1 = L_2 = L_3 = L_4 = L_5 = L_6 = L = 330\mu$H and $C_1 = C_2 = C = 1410\mu$F)

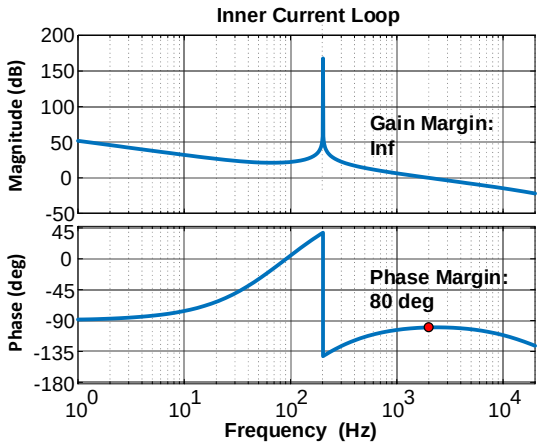


Fig. 13. Bode plot of the inner current loop gain using PI controller given in (48)

E. Comparison with PI Controller

The PI controller has been widely applied to regulate power electronic devices due to its simplicity. However, this controller is designed using the small-signal method, which only guarantees local stability for the non-linear system. However, the existence of large-signal disturbances may drive the system operation point out of its local stability range and destabilize the regulated non-linear system. Next, to show the global stability feature of the proposed controller, a comparative study of the proposed SMC and the conventional PI controller is carried out.

Based on the PI controller design guidelines reported in [10], a dual-loop PI controller for the IFDBC system using the circuit parameters given in Table I is design as follows,

$$G_{ic}(s) = \frac{18.8562}{s}\left(\frac{s+918.06}{918.06}\right)\left(\frac{172010}{s+172010}\right) \quad (58)$$

$$G_{vc}(s) = \frac{134.1263}{s}\left(\frac{s+113.31}{113.31}\right)\left(\frac{13937}{s+13937}\right) \quad (59)$$

where $G_{ic}(s)$ and $G_{vc}(s)$ represent the inner current loop controller and outer voltage loop controller, respectively. The Bode plot of the inner current loop gain is shown in Fig. 13. The cross-over frequency of the inner current loop is 2kHz, which is 1/10 of the switching frequency f_{sw}, and the corresponding phase margin is 80^{o}. To avoid the dynamic of the inner current loop affecting the design of the outer voltage loop controller, the cross-over frequency of the later is selected as

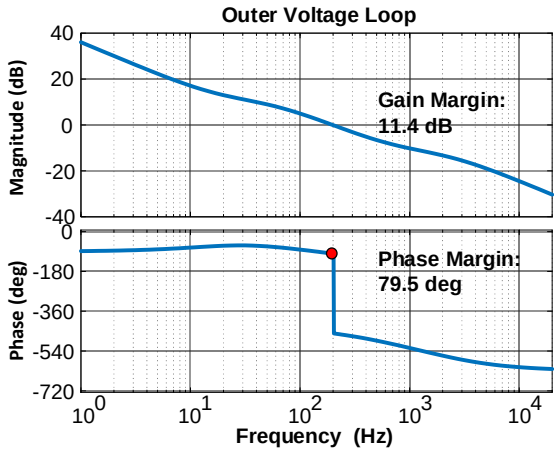


Fig. 14. Bode plot of the inner current loop gain using PI controller given in (49)

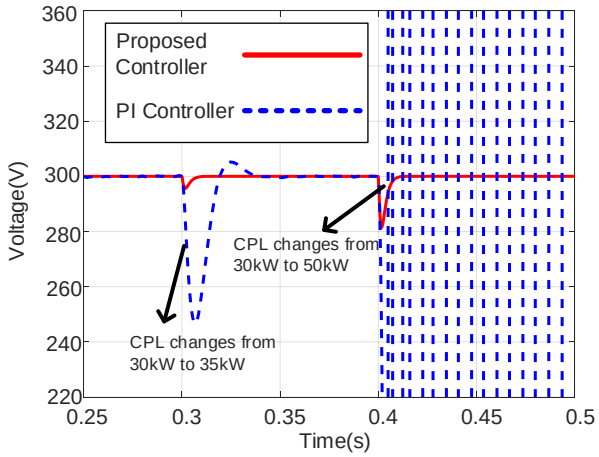


Fig. 15. Transient responses in the presence of CPL changes of the system regulated by proposed controller (red) and PI controller (dotted blue)

1/10 of that of the inner current loop, i.e. 200Hz. the Bode plot of the outer voltage loop gain is illustrated as Fig. 14. As the figure shown, the magnitude plot crosses zero at 202Hz, which meets the design requirement. Besides, 79.5° phase margin and 11.4 gain margin are achieved to ensure the stability robustness of the regulated system [10].

Fig. 15 shows the output transient responses of the IFDBC systems controlled by the proposed SMC and PI controller, respectively. The load power P_{CPL} changes from 30kW to 35kW at $t = 0.3s$ and then, further increases to 50kW at $t = 0.4s$. It can be seen that the proposed controller shows expected performance in handling with both small scale and large scale load power changes. On the contrary, although the PI controller stabilize the IFDBC system for the first load power change, it fails to ensure the system stability with the large signal CPL power change from 1kW to 5kW.

V. Experimental Results

To verify the feasibility of the proposed SMC for the system of IFDBC with CPL in practical applications, an experimental prototype of a 6-phase IFDBC is built, and a Chroma DC

TABLE II
System Parameters in Experiments

Circuit Parameters	Values
IFDBC input side voltage	$V_{in} = 100\text{V}$
DC bus reference voltage	$V_{ref} = 300\text{V}$
Module capacitor reference voltage	$V_{cref} = 200\text{V}$
Inductance of each inductor	$L_i = 2.5\text{mH}$
Output capacitance	$C_1 = C_2 = 470\mu\text{F}$
Switching frequency	$f_{sw} = 20\text{kHz}$

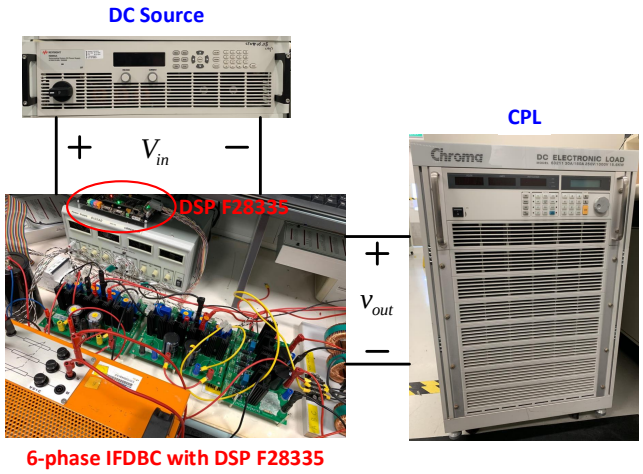


Fig. 16. Experimental prototype of a 6-phase IFBDC fed DC microgrid

electronic load is used to emulate the CPL. In addition, the proposed control strategy is implemented using TI DSP F28335. The corresponding experimental devices are shown in Fig. 16. In the experiments, the adopted circuit parameters are the same as those given in Table II, and, following the tuning guideline given in Section IV, the controller gains are selected as $K_{di} = 2000$ for $i \in \{1, 2, 3, 4\}$, $K_{s1} = K_{s3} = 0.1$, $K_{s2} = K_{s4} = 20000$ and $a_1 = a_2 = 10000$. In addition, it is worth noting that the verification experiments are carried out by using pure CPL, which creates the worst system stability condition.

To show the advantages of the proposed controller as compared to the traditional SMC (designed in Section III) in the practical application, first, an experiment using the traditional SMC without NDO has been carried out, and corresponding experimental results are given in Fig. 17. As the figure shown, the load power P_{CPL} jumps from 2kW to 5kW, and then back to $2kW$. Again, the IFDBC's output voltage v_o and both the module capacitor voltages v_{c1} and v_{c2} do not accurately track their references $V_{ref} = 300V$ and $V_{cref} = 200V$, respectively.

Next, experimental results obtained using the proposed controller, under various operation conditions, are given out. Fig. 18 shows the IFDBC's responses in presence of CPL changes. The load power has a step rise from 2kW to 5kW, and then it restores to 2kW. It can be seen that the capacitor voltages v_{c1} and v_{c2} closely track their reference. Consequently, the total output voltage v_{out} is regulated to its reference with negligible steady-state error. According to the zoom-in

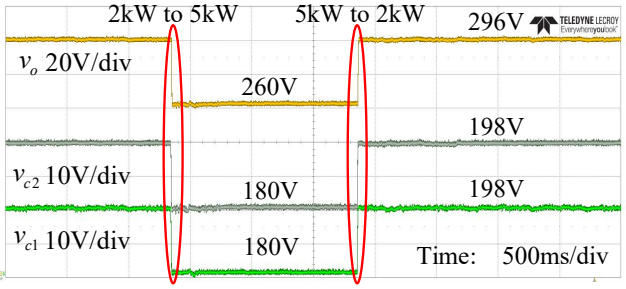


Fig. 17. Six-phase IFDBC system voltage responses obtained using the traditional SMC without NDO

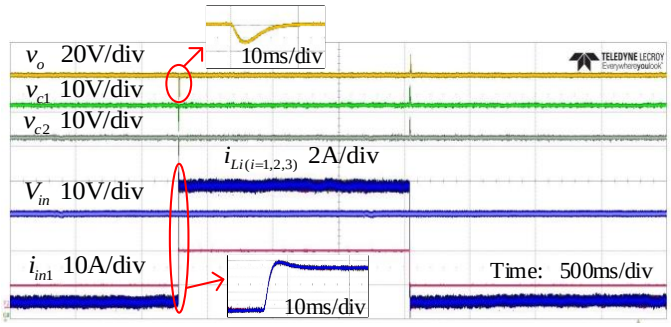


Fig. 18. Six-phase IFDBC system dynamic responses with pure CPL for load power changes from $P_{CPL} = 2kW$ to $P_{CPL} = 5kW$, and restores to $P_{CPL} = 2kW$

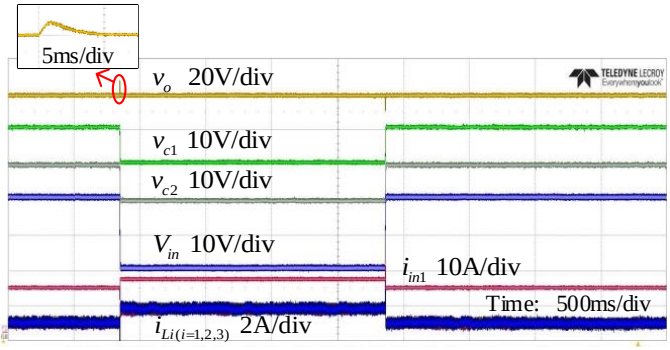


Fig. 19. Six-phase IFDBC system dynamic responses with pure CPL for input voltage changes from $V_{in} = 100V$ to $V_{in} = 80V$, and restores to $V_{in} = 100V$

part of v_{out}, the transient time is around 8ms. In addition, the magnified plot of phase currents of Module 1 indicate that good inter-phase current balance is achieved in both steady-state and transient-state.

The converter system responses in presence of input voltage variations are shown in Fig. 19, where the input voltage changes from $V_{in} = 100V$ to $V_{in} = 80V$, and then back to $V_{in} = 100V$. As shown in the figure, the total output voltage v_{out} rapidly restores to its reference within 5ms, and the capacitor voltages drop to 190V when $V_{in} = 80V$, which is consistent with the previous analysis (see (6)). Besides, thanks to the CBCs, the interphase current equals to each other.

Fig. 20 illustrates the system responses for the step changes in the IFDBC's output voltage reference V_{ref}. Specifically, V_{ref} changes from 300V to 400V, and ,then, restores to 300V.

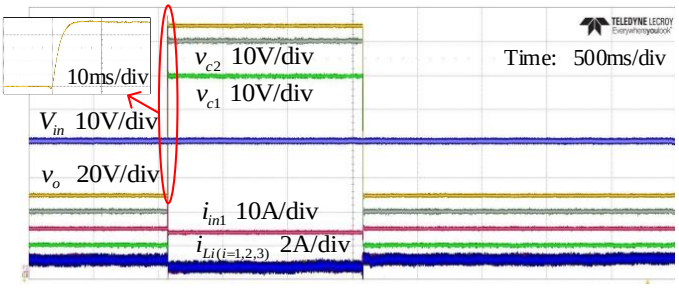


Fig. 20. Six-phase IFDBC system dynamic responses with pure CPL for output voltage reference changes from $V_{ref} = 300V$ to $V_{ref} = 400V$, and restores to $V_{ref} = 300V$

As shown in the figure, with expected interphase current balancing, fast (the settling time is around 6ms) and accurate voltage tracks are achieved for both the converter output voltage and capacitor voltages.

Based on the results presented above, it can be concluded that, the large-signal stability of the IFDBC system with pure CPL is guaranteed by the proposed sliding-mode controller. Fast dynamic response and nearly zero steady-state error are simultaneously achieved. In addition, interphase current balance is maintained even in presence of large-signal disturbances.

VI. Conclusion

This paper proposes a new nonlinear disturbance observer (NDO) based sliding-mode controller for the interleave floating dual boost converter (IFDBC) fed the DC microgrid with constant power loads. A generalized reduced-order model for the IFDBC is developed to simplify the controller design and system analysis.The proposed method guarantees the large signal stability of DC microgrid bus voltage without using extra sensors. Fast and accurate estimations are provided by the proposed NDO, which contributes to effectively alleviate the chattering problem in sliding-mode control. In addition, the interphase current balance is achieved by adopting the current balance compensators, which fully explores the advantages of IFDBC, such as low current/voltage ripple. Noticeably, the proposed control scheme is also available to other converter topologies.

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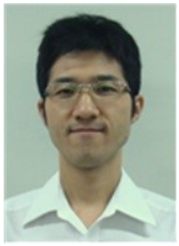

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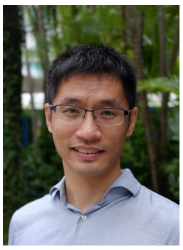

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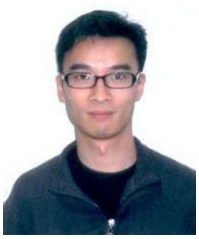

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