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ORIGINAL ARTICLE

Mitigation of voltage sag, swell and power factor correction using solid-state transformer based matrix converter in output stage

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KEYWORDS

Solid-state transformer (SST);
Medium frequency transformer;
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Matrix converter

Abstract This paper presents a novel topology of solid-state transformer (SST). In the design process, the AC/DC, DC/AC and AC/AC converters have been integrated to achieve higher efficiency. To obtain higher efficiency from other SST with DC-link topologies, the AC/DC and DC/AC converters have been integrated in one matrix converter. The proposed SST performs typical functions and has advantages such as power factor correction, voltage sag and swell elimination, voltage flicker reduction and protection capability in fault situations. In addition, it has other benefits such as light weight, low volume and elimination of hazardous liquid dielectrics because it uses medium frequency transformer. The operation and some performances of the proposed SST have been verified by the simulation results.

1. Introduction

Transformers are widely used in electric power system to perform the primary functions, such as voltage transformation and isolation. Transformers are one of the heaviest and most expensive devices in an electrical system because of the large iron cores and heavy copper windings in the composition [1]. A new type of transformers based on power electronic converters has been introduced, which realizes voltage transformation, galvanic isolation, and power quality improvements in a single device. The SST provides a fundamentally different and more complete approach in transformer design by using power electronics on the primary and secondary sides of the transformer. Several features such as instantaneous voltage regulation, voltage sag compensation and power factor correction can be combined into SST.

Different topologies have been presented for realizing the SST, in the recent years [2–13]. These topologies are called as PET or EPT. In [2] the AC/AC buck converter has been proposed to transform the voltage level directly and without any isolation transformer. This method would cause the semiconductor devices to carry very high stress.

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Nomenclature

DC	direct current
AC	alternative current
SST	solid-state transformer
PET	power electronic transformer
EPT	electronic power transformer
MF	medium frequency
VSC	voltage source converter
PWM	pulse width modulation
SPWM	sinusoidal pulse width modulation
V_{in}	input voltage
I_{in}	input current
V_{dc}	DC link voltage
V_i	primary voltage in MF transformer
V_S	secondary voltage in MF transformer
N_i	primary turn winding in MF transformer
N_S	secondary turn winding in MF transformer
IGBT	insulated gate bipolar transistor
f	frequency
m	modulation index
f_S	frequency of the main supply in AC/AC converter
f_T	frequency of the triangular carrier
Vo	output voltage
Io	output current

In second type, the line side AC waveform is modulated into a MF square wave, coupled to the secondary of MF transformer, and again is demodulated to AC form by a converter in second side of MF transformer. This method however does not provide any benefits such as instantaneous voltage regulation and voltage sag compensation due to lack of energy storage system [3–6].

Another type is a three-part design that utilizes an input stage, an isolation stage, and an output stage [7–13]. These types enhance the flexibility and functionality of the electronic transformers owing to the available DC links.

In the recent years, increasing attention has been drawn to the matrix converters as a variable voltage variable frequency AC/AC power processing system with applications to the fields that require smaller size, higher power density and easier maintenance [14–16].

This paper investigates the SST that includes three parts input stage, isolation stage, and output stage. Proposed SST includes AC/AC converter. The proposed AC/AC converter can generate desired output voltage from square input voltage. The main purpose of this paper is reduction in the stage and components of the three-part SSTs.

The proposed SST includes only one DC-link capacitor and in output stage, rectifier and inverter have been integrated to reduce the power losses and increase the efficiency. The proposed topology performs input power factor correction, eliminates voltage sag and swells, reduces the voltage flicker and does not utilize mineral oil or other liquid dielectrics.

Many different algorithms are presented to switching in power electronic converters. A very popular method is classic carrier based SPWM that is used in this paper.

To verify the performance of the proposed SST, computer-aided simulations are carried out using MATLAB/SIMULINK.

2. Conventional SST

In the SST using MF AC-link without DC-link capacitor, the line side AC waveform is modulated with a converter to a medium-frequency square-wave and passed through a MF transformer and again with a converter; it is demodulated to AC form power-frequency. Since the transformer size is inversely proportional to the frequency, the MF transformer will be much smaller than the power-frequency transformer. So, the transformer size, weight and stress factor are reduced considerably [3]. This converter does not provide any benefits in terms of control or power-factor improvement, and may not protect the critical loads from the instantaneous power interruptions due to lack of energy storage system. In addition, another drawback is the inability to prevent primary voltage harmonics from propagating into the load side.

The SST with DC-link capacitor includes three stages. First stage is an AC/DC converter which is utilized to shape the input current, to correct the input power factor, and to regulate the voltage of primary DC bus. Second stage is an isolation stage which provides the galvanic isolation between the primary and secondary side. In the isolation stage, the DC voltage is converted to a medium-frequency square wave voltage, coupled to the secondary of the MF transformer and is rectified to form the DC link voltage. The output stage is a voltage source inverter which produces the desired AC waveforms [4–8]. In comparison with first SST, the voltage or current of SST can be flexibly controlled in either side of MF transformer. It is possible to add energy storage to enhance the ride-through capability of the SST or to prepare integrated interface for distributed resources due to the available DC links. It prevents the voltage or current harmonics to propagate in either side of the transformer, even if the input voltage has low order harmonic content or the load is not linear but they need too many AC/DC links, large bulky magnetic components or DC-link electrolytic capacitors. Thus they are resulted in a rather cumbersome solution and multiple power conversion stages can lower the transformer efficiency.

3. Proposed SST

The block diagram of the proposed SST is shown in Fig. 1. As can be seen from the Fig. 1, this is a three-stage design that

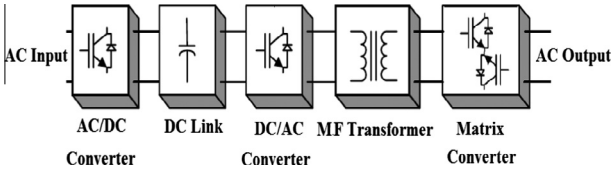

Figure 1 Block diagram of proposed SST with DC link.

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includes input stage, isolation stage and output stage. In the input stage, there is a converter, which converts the input AC voltage to DC voltage. The second part of the converter is formed by a DC/AC converter. This part of the converter contains the MF transformer with the high insulation capability. In the output part, the medium frequency voltage is revealed as a power-frequency voltage. In this paper, a three-part design is introduced. It is a new configuration based on the matrix converter with new function shown in Fig. 1. It can provide desired output voltage. In addition, it performs power quality functions, such as sag correction, reactive power compensation and is capable of providing three-phase power from a single phase system. The SST has three stages and each stage can be controlled independently from the other one. Many advantages of the SST such as output power quality and power factor correction depend on appropriate close-loop control, and correlative research is necessary. The reliability of a system is indirectly proportional to the number of its components. The main purpose of proposed SST is reduction in the power delivery stage (AC/DC and DC/AC links) in SST with DC-link.

3.1. Input stage

The input stage is a three or single phase PWM rectifier, which is used to convert the primary low frequency voltage into the DC voltage. The main functions associated with the rectifier control are shaping the input current, controlling the input power factor, and keeping the DC-link voltage at the desired reference value. Many control methods are presented for control of input stage in conventional SST, which could be used in proposed SST. Fig. 2 shows three phase rectifier with input inductances. A three phase PWM rectifier is used in this paper, which operates same as input stage of conventional SST [6–8]. Fig. 3 shows input stage control diagram. To realize constant DC voltage and keep input current sinusoidal, the double control loops, a DC voltage outer loop and an AC current inner loop, are adopted. For most description refer to [6–8]. As can be seen from Fig. 3, the reference for the active current is derived from the DC voltage outer loop. The reference for the reactive current is set to zero to get unity power factor. The current error signals are input the current regulators and then form the modulation signals. If the d axis of the reference frame is aligned to the grid voltage, we obtain $V_{inq} = 0$.

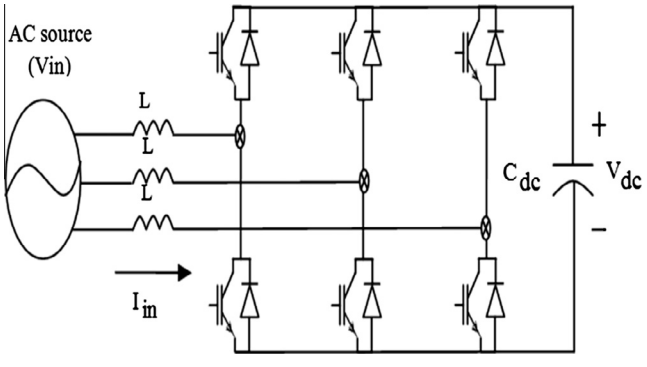

Figure 2 Structure of the proposed input stage.

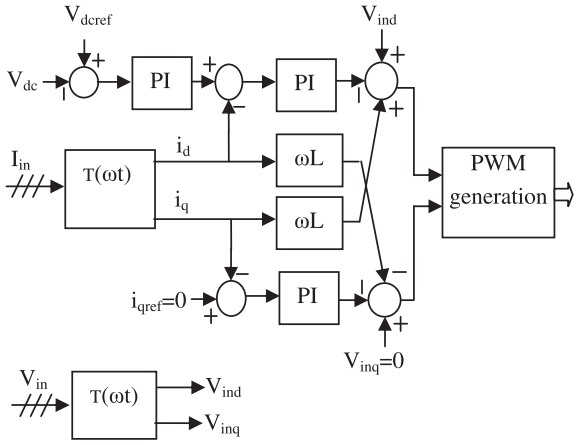

Figure 3 Input stage control diagram.

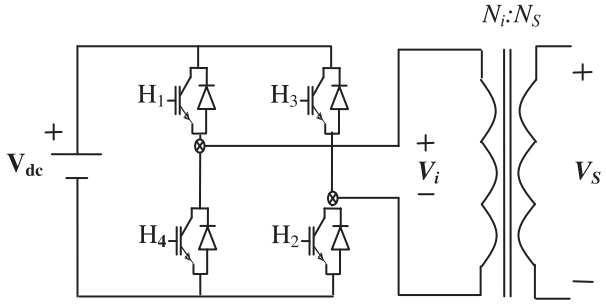

Figure 4 Structure of the proposed isolation stage.

3.2. Isolation stage

Isolation stage is contained a single-phase medium frequency VSC, which converts the input DC voltage to AC square voltage with medium frequency and MF transformer. The main functions of the MF transformer are such as voltage transformation and isolation between source and load [8,9]. Structure of the proposed isolation stage is shown in Fig. 4. Circuit diagram of VSC is the same as H-bridge cell. To simplify the design of the control system, open loop control is applied for the VSC. The principle of modulation is based on a comparison of a sinusoidal reference waveform with zero carrier waveform.

The principle of switching H-bridge is described with conditions bellow:

Condition 1 if sin wave $\geqslant 0$, then H_1 and H_2 are turned on.
Condition 2 if sin wave < 0, then H_3 and H_4 are turned on.

If sine reference wave has a frequency f_r and an amplitude A_r then output voltage of VSC has a frequency f_r.

By neglecting the losses of MF transformer, the MF transformer can be treated as a proportional amplifier. The simplified model of the MF transformer is presented as:

$$V_s = \frac{N_s}{N_i} V_i \tag{1}$$

V_i, V_s are the primary and secondary voltage in MF transformer, respectively and N points to turn ratio. A square voltage source can be generated by isolation stage.

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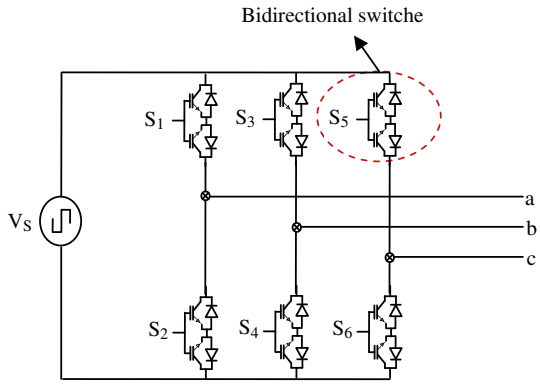

Figure 5 Proposed matrix converter.

3.3. Output stage

Fig. 5 shows a matrix converter with novel function for conversion square wave with medium frequency to sinusoidal with power frequency voltage. Matrix converter topology employs six bidirectional switches to convert medium frequency single-phase input directly to a power frequency (50/60 Hz) three-phase output.

The common emitter anti-parallel IGBT with diode pair arrangement has been used in this topology. This bidirectional switch arrangement consists of two diodes and two IGBTs and has capability of blocking voltage and conducting current in both directions. The proposed converter generates desired output voltage with suitable shape and frequency.

Operation of proposed converter is the same as three levels voltage source inverter but here voltage source has two polarities. Several modulation strategies have been proposed for traditional inverters. Among these methods, the most common used is the SPWM.

The principle of the SPWM is based on a comparison of a sinusoidal reference waveform, with triangular carrier waveform. At each instant, the result of the comparison is decoded in order to generate the correct switching function corresponding to a given output voltage level.

In proposed SST, SPWM modulation technique applied to a matrix converter is employed. The switching algorithm of the matrix converter is composed with SPWM and one control signal. The produced signals by SPWM generator are combined with one control signal (NPD) which shows negative polarity of matrix input voltage. NPD points to negative polarity detector. Fig. 6 shows the circuit that produces NPD signal. The switching pattern is expressed as follows:

$$\text{Gate signals} = (\text{SPWM signals})\text{XOR}(\text{NPD signal}) \quad (2)$$

Fig. 7 shows input voltage and NPD signal. Frequency of input voltage is 1000 Hz in this example.

Table 1 shows logic table of switching. In this switching method with changing of polarity in input voltage source on switches are turned off and off switches in arms are turned on.

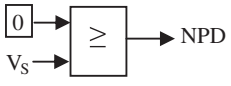

Figure 6 NPD generator.

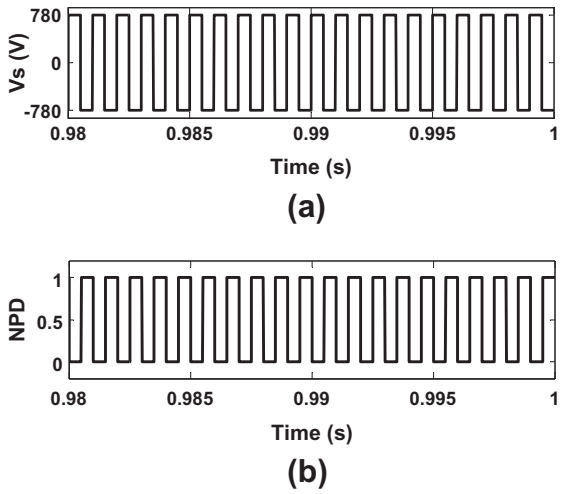

Figure 7 (a) Input voltage of matrix converter and (b) NPD signal.

Table 1 Logic table of switching.

SPWM signals	NPD	Gate signals
0	0	0
0	1	1
1	0	1
1	1	0

In the switching algorithm, there are two important parameters to define the amplitude modulation ratio, or modulation index m, and the frequency modulation ratio p. Definitions are given by

$$m = \frac{V_{ref\max}}{V_{carrier\max}} \quad (3)$$

$$p = \frac{f_T}{f_S} \quad (4)$$

where $V_{ref\ max}$ and $V_{carrier\ max}$ are the amplitudes of reference voltage and carrier voltage, respectively. On the other hand, f_S is the frequency of the main supply and f_T the frequency of the triangular carrier.

As it can be seen in Fig. 8, the matrix converter is controlled by PWM method. In this case, the direct axis, quadratic axis, and zero sequence quantities for three-phase sinusoidal signal are computed by Park transformation. Then the dq voltage terms are compared by reference signals V_{dref} and V_{qref} and error signals enter to PI controllers. Next the PI controller outputs are transformed to three-phase sinusoidal abc voltage terms and used to generate appropriate matrix gate pulses.

In Fig. 9, $m = 0.8$ and $p = 21$. Modulation waveforms to switching are shown in Fig. 9(a). PWM switching pulses are produced from comparison among sin waves and carrier. These pulses are shown in Fig. 9(b). NPD signal has been shown in Fig. 9(c). Fig. 9(d) shows switching pulses in matrix converter. In the modulation method described in Fig. 9 magnitude and harmonic contents of output voltage change with p and m similar to traditional inverters. Fig. 10 shows switching and operation of NPD signal in small time for single phase.

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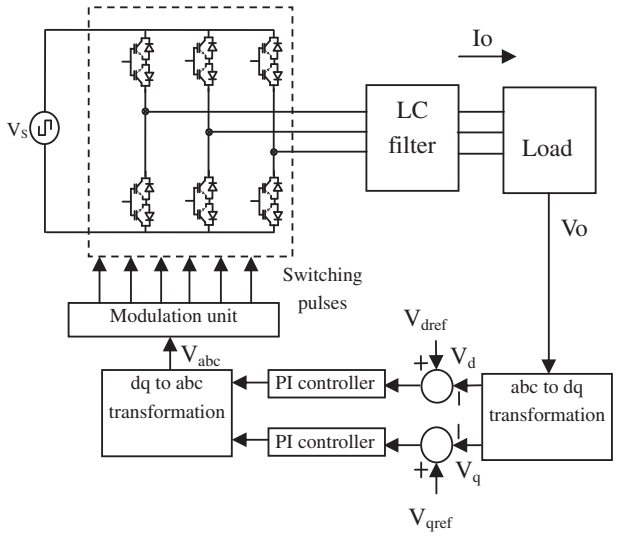

Figure 8 Circuit control of output stage.

When NPD signal is zero, G1 and G2 (or PWM signals) do not change and when NPD signal is one, G1 and G2 are changed to opposite state. This method is used to synthesize each of the three voltage waveforms, which are separated by 120° in this three-phase system.

4. Comparison study

In comparison with conventional SST with DC-link, in proposed converter power delivery stages and power electronic converters have been reduced and AC/AC matrix converter is replaced by two converters (rectifier and inverter). Multiple power conversion stages can lower the transformer efficiency. This idea leads to the loss reduction, by processing the power in one stage instead of two stages. Switching algorithm is easy but not complex. Each switch requires one gate driver. Reduction in gate driver is obtained with reduction in number of switches. This point reduces the installation area and the number of the gate driver circuits. Therefore, the cost of the suggested topology is less than the conventional topology. One DC-link capacitors are required in proposed SST. This plan increases dynamic velocity of transformer. For example, Ref. [8] uses 24 switches and one DC-link capacitor or Ref. [9] uses 10 switches and one DC-link capacitor while proposed structure uses only six switches and does not use DC-link capacitor. Another important problem in converters is the ratings of switches. In other words, voltage and current ratings of the switches in a converter play important roles on the cost and realization of the converter. In the proposed topology, the currents of all switches are equal with the rated current of the load and the rating of switches depends on output voltage of MF transformer. The rating of switches is the same as other topologies [9].

5. Simulation results

To evaluate the expected performance of the SST, the design was simulated to predict steady state performance. A prototype based on the proposed topology is simulated using MATLAB/SIMULINK.

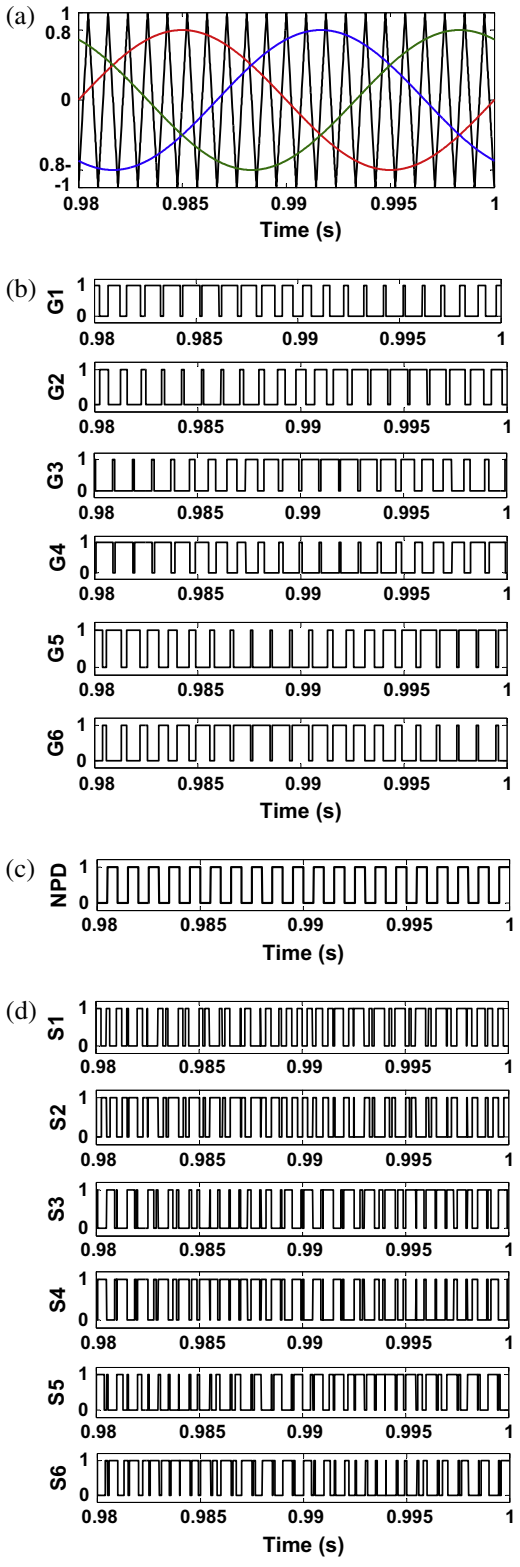

Figure 9 Switching (a) modulation signal (b) PWM signals (c) NPD signal and (d) switching pulses.

In these simulations the line voltage is 3.8 kV and the SST power is 30 kVA. Also the parameter value used for simulations has been shown in Table 2.

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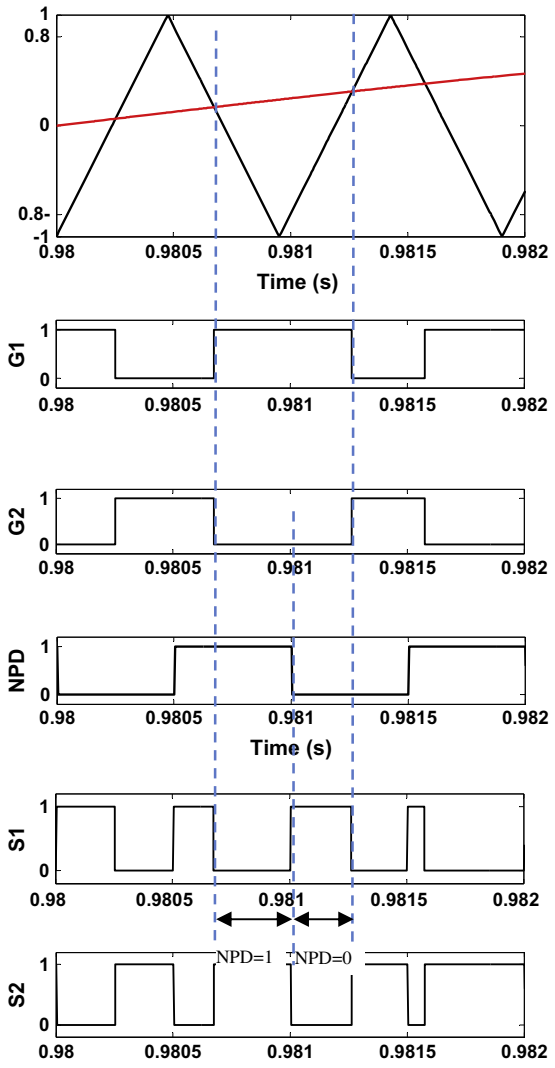

Figure 10 Operations of NPD signal.

Table 2 Parameters of simulation.

Parameters	Value
Input line voltage	3.8 kV
DC link capacitor	2000 μF
Power frequency	50 Hz
MF transformer	1:1, 1000 Hz, 30 kVA
Output line voltage	380 V
Matrix converter switching frequency	2050 Hz
LC filter	2 mH, 220 μF
SST load	20 kW + j10 kVAR

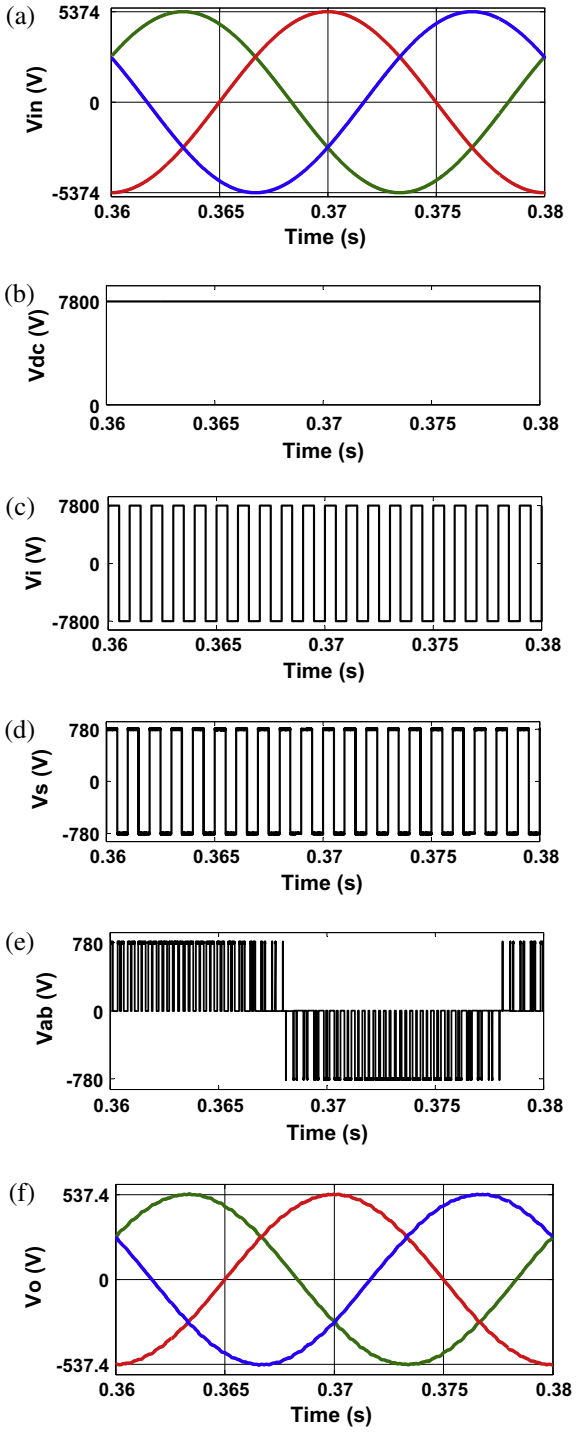

Figure 11 (a) Input line voltages (b) DC-link voltage (c) the MF transformer primary voltage (d) the MF transformer secondary voltage (e) output line voltage before filter and (f) output line voltage.

5.1. Operation of proposed SST

Operation of proposed SST is described in Fig. 11. Fig. 11(a) shows line input voltage of SST. As it can be seen in Fig. 11(b), the DC-link voltage of input stage is 7800 V. The voltage controller in Fig. 3 acts so that the DC-link voltage is regulated in reference value. Fig. 11(c) depicts the output voltage of VSC in isolation stage that transforms DC voltage to medium frequency AC voltage as the transformer primary voltage. The level of medium frequency AC voltage in secondary side is changed by MF transformer in Fig. 11(d). In the output stage, the medium frequency voltage is revealed as a 50 Hz waveform by AC/AC matrix converter. Fig. 11(e) shows

line voltage between phase (a) and phase (b) before LC filter and load voltage is shown in Fig. 11(f).

5.2. Power factor correction

Fig. 12 shows the SST input power factor correction ability. In these simulations the active load is assumed to be 20 kW and the reactive power is assumed to be 10 kVAR inductive. Fig. 12(a) and (b) shows phase voltages and currents of the load. Voltage and current for one phase together are shown in Fig. 12(c). It is considered that the power factor is 0.5 lag. Fig. 12(d) shows input phase voltage and current. As it can be seen, the controller makes the q component of input current in Fig. 3 to be regulated in zero, as a result power factor is 1 in the input when the load is lag.

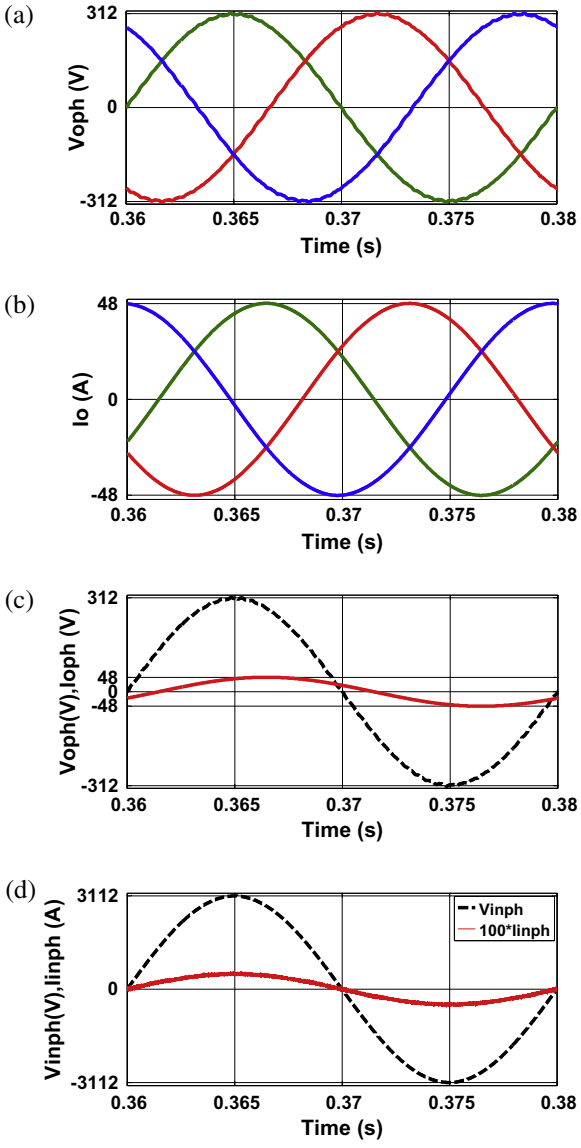

Figure 12 SST current and voltage waveforms in inductive load (a) load voltages (b) load currents (c) one phase output voltage and current and (d) single phase intput voltage and current.

5.3. Responses to sag voltage

To illustrate a typical response of SST, consider three phase balanced voltage sag with 30% depth created at 0.4 s by simulating a remote three phase fault. Input line voltage V_{in}, the DC-link voltage V_{dc}, output line voltage before filter V_{ab} and

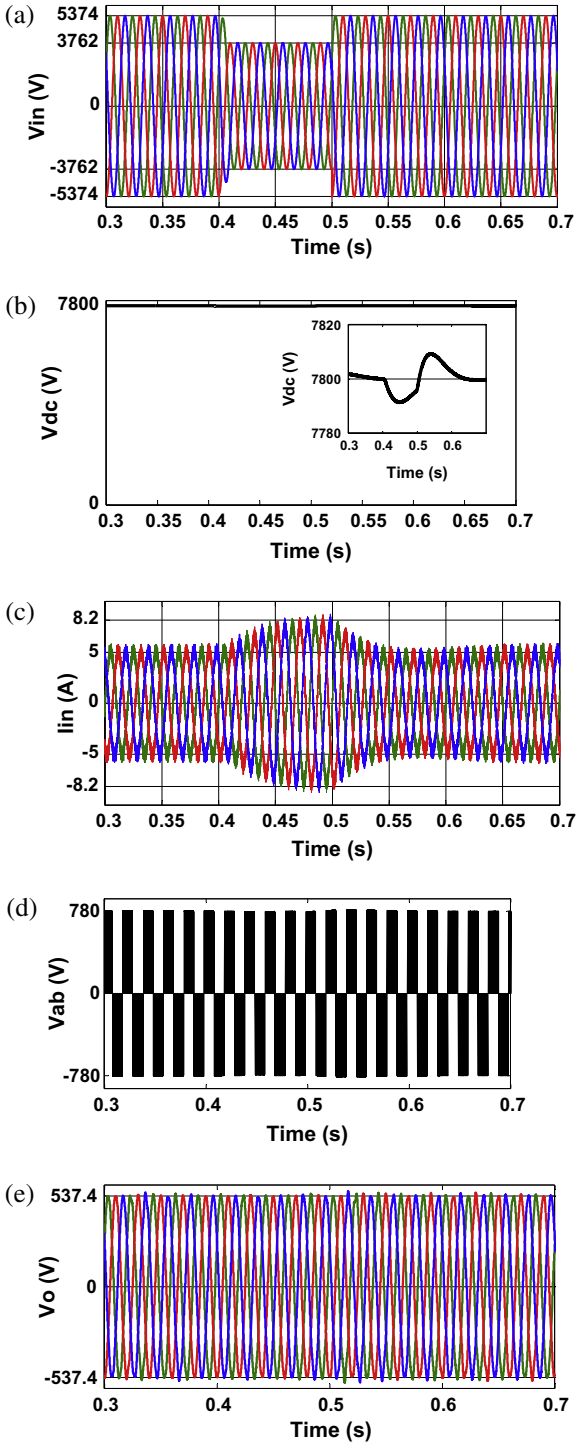

Figure 13 (a) Input line voltage (b) DC-link voltage (c) input current (d) output line voltage before filter and (e) load voltage.

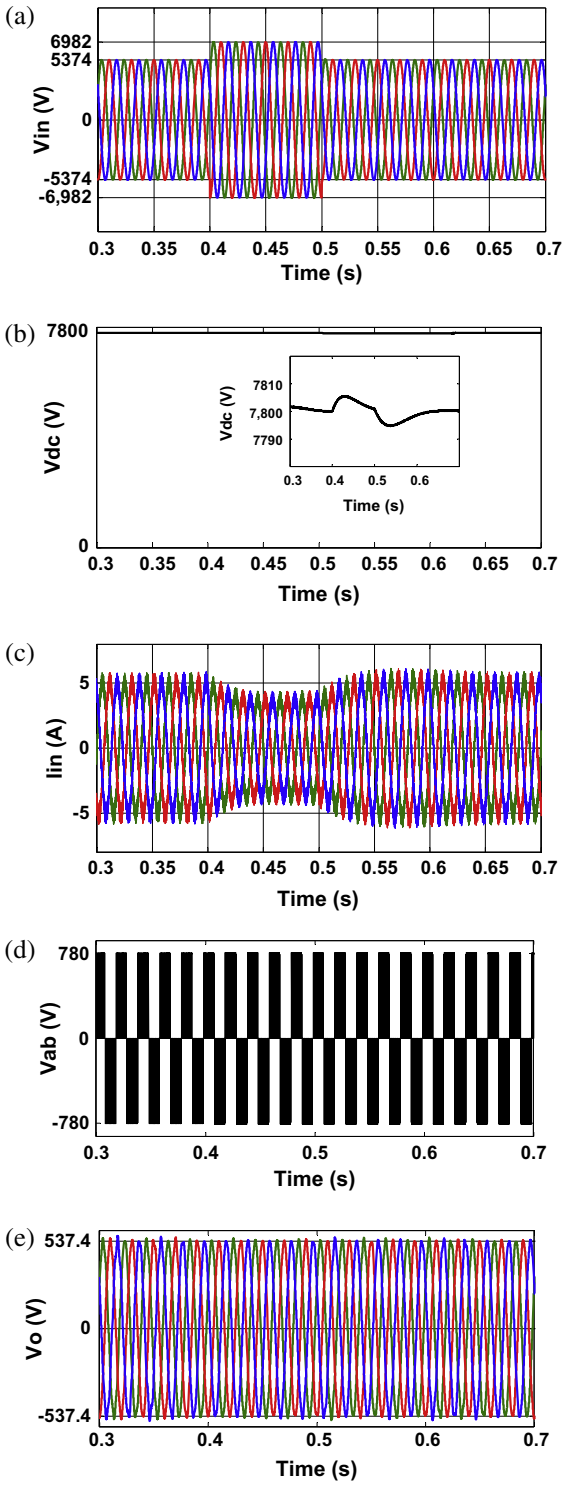

Figure 14 (a) Input line voltage (b) DC-link voltage (c) input current (d) output line voltage before filter and (e) load voltage.

the load voltage V_O of the system with the proposed SST are shown in Fig. 13.

It is considered when voltage sag occurs and clears, DC link voltage deviates in Fig. 13(b) and after transient state tracks the reference value i.e. 7800. The grid currents during sag and swell are not instants, during sag the current will increase

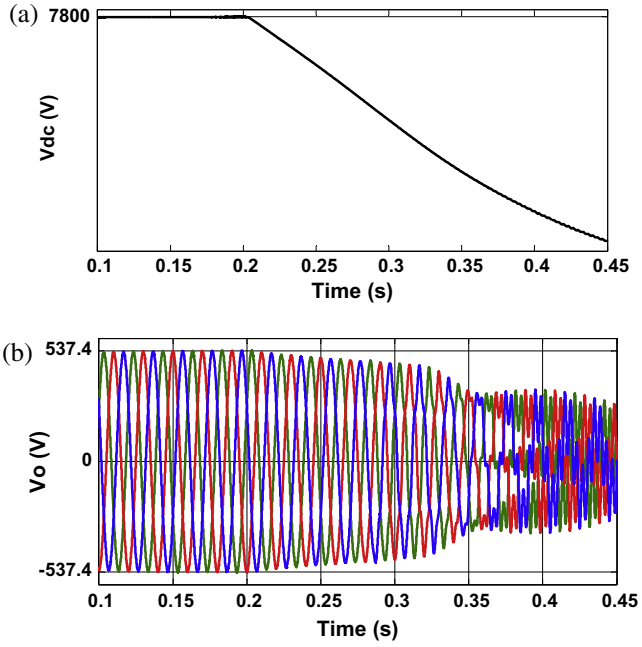

Figure 15 (a) the voltage of DC-link (b) the load voltage.

to maintain constant V_{dc}. Fig. 13(c) shows the input current. The allowable percentage increase for current depends on compensation percentage. Also, the output stage controller in Fig. 8 makes the matrix converter to generate a voltage so that the load voltage maintains as pre-sag.

5.4. Responses to swell voltage

Fig. 14 shows the three-phase balanced voltage swell at input voltage, DC-link voltage, line voltage before filter and the SST output voltages. The swell period starts at $t = 0.4$ s and ends at $t = 0.5$ s. During the swell, the phase voltages increase to 1.3 from its nominal value. Fig. 14(b) shows DC-link voltage. During the voltage swell, the input voltage increases but DC-link voltage almost is constant. The ripple of DC-link voltage is small and controller adjusts DC-link voltage in references value. In this state, input currents decrease. Fig. 14(c) shows input current. Fig. 14(d) shows the load voltage before LC filters. The output converter controller keeps the load voltage at rated value as in normal operation conditions. The load voltage is shown in Fig. 14(e).

As it can be seen, the load voltage has been effectively compensated. Also, the traditional SST is able to correct the voltage within fraction of a cycle. It is considered the suggested topology produces desired load voltage and improves power quality problems. The simulation results demonstrate the excellent performance of the proposed structure for the SST.

5.5. State of undesired DC-link value

If the DC-link voltage is not adjusted in desired value then the voltage of load drops and load is not supplied well. Fig. 15(a) shows the voltage of DC-link. In this case, in 0.2 s the voltage of dc-link decreases. The load voltage is shown in Fig. 15(b). In this state converter cannot regulate output voltage at desired value.

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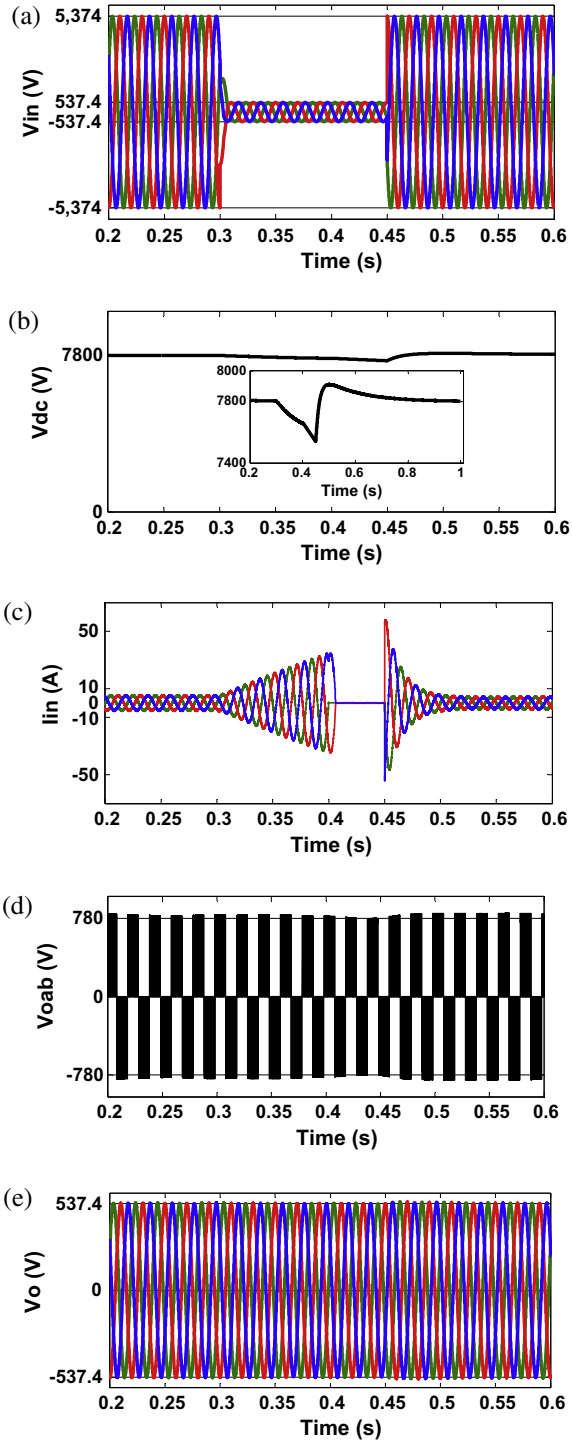

Figure 16 (a) Input line voltage (b) DC-link voltage (c) input current (d) output line voltage before filter and (e) load voltage.

5.6. Responses to severe sag voltage and current limiter operation

To illustrate response of SST to severe sag and current limiter operation, consider three phase balanced voltage sag with 90% depth created at 0.3 s. Imagine current limiter cut line supply if input currents exceed from 10A for two cycles. Input line voltage V_{in}, the DC-link voltage V_{dc}, output line voltage before filter V_{ab} and the load voltage V_O of the system with the proposed SST are shown in Fig. 16. It is considered when voltage sag occurs and clears, DC link voltage deviates in Fig. 16(b). The grid currents during sag will increase to maintain constant V_{dc}. Fig. 16(c) shows the input current. Current limiter cut line supply at 0.4 s. The allowable percentage increase for current depends on compensation percentage. The voltage sag is removed from system in 0.45 s.

6. Conclusions

In this paper a new configuration of SST with DC-Link capacitor has been proposed. To obtain higher efficiency, the AC/DC and DC/AC converters have been integrated in one converter and only one DC-link is used in proposed SST. In proposed SST one AC/AC matrix converter has been replaced by two converters and switching of matrix converter is easy and not complex. These plans decrease the installation area and increase dynamic velocity of transformer. The topology described in this paper has many advantages such as power factor correction, voltage regulation, voltage sag and swell elimination, voltage flicker reduction. Simulation results showed some of advantages in proposed SST.

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