Available online at www.sciencedirect.com
ScienceDirect
Solid-State Electronics 52 (2008) 957–961
SOLID-STATE ELECTRONICS
www.elsevier.com/locate/sse

Low-voltage constant-g_m rail-to-rail CMOS operational amplifier input stage

Yan Lu, Ruo He Yao *

Institute of Microelectronics, South China University of Technology, Guangzhou 510640, China

Received 27 August 2007; received in revised form 20 December 2007; accepted 12 February 2008
Available online 24 March 2008

The review of this paper was arranged by Prof. Y. Arakawa

Abstract

This paper presents a rail-to-rail constant-g_m operational amplifier input stage. The proposed circuit changes the tail current of the input differential pairs dynamically for a constant-g_m by using dummy input differential pairs. The problem which causes total g_m variation is input pairs and dummy input pairs can not take effect at the same time with the common-mode input voltage changes, because the tail current transistor of the input pairs are in triode region when the input pairs are turned off, the dummy input pairs will enter subthreshold region from cut-off region before the input pairs when common-mode voltage changes. The effect of this problem is more obviously in low supply voltage design. To solve this problem, compensate current sources is added to the tail current transistors of each dummy input differential pairs for lower g_m variation. The g_m of this Op Amp's input stage varies around $\pm 2\%$.

Keywords: Rail-to-rail; Operational amplifier; Compensate current

1. Introduction

With the development of mixed/mode VLSI systems, there has been significant interest in analog integrated circuits operating with low supply voltage. The input common-mode voltage (V_{icm}) of an Op Amp should be kept as wide as possible in many applications, especially in mixed/mode IC area [1–4].

The input stage is the key part of a rail-to-rail Op Amp. In order to obtain a reasonable signal-to-noise ratio in low voltage design, the input stage should be able to deal with common-mode input voltages from rail-to-rail [1–4]. This can be achieved by placing an N-channel and a P-channel differential input pair in parallel [5], as shown in Fig. 1. When the common-mode input voltage is near the ground rail, only P-channel operate; when the common-mode input voltage is near the V_{DD} rail, only N-channel operate; and in the middle range of the common-mode input voltage, all differential pairs operate. However, when both differential pairs are in full operation the transconductance of this input stage is twice of that when only one pair is active. The circuit operates in three regions as following:

Region I: $V_{onn} \geqslant V_{icm} \geqslant Gnd$ (N-channel turn-off, P-channel operation)

$$g_m(\text{eff}) \approx g_{m\text{P}} \tag{1}$$

Region II: $V_{onp} \geqslant V_{icm} \geqslant V_{onn}$ (N-channel operation, P-channel operation)

$$g_m(\text{eff}) = g_{m\text{N}} + g_{m\text{P}} \tag{2}$$

Region III: $V_{DD} > V_{icm} > V_{onp}$ (N-channel operation, P-channel turn-off)

$$g_m(\text{eff}) \approx g_{m\text{N}} \tag{3}$$

* Corresponding author. Tel.: +86 020 87111583; fax: +86 020 87112873.
E-mail address: phrhyao@scut.edu.cn (R.H. Yao).

0038-1101/$ - see front matter © 2008 Elsevier Ltd. All rights reserved.
doi:10.1016/j.sse.2008.02.002

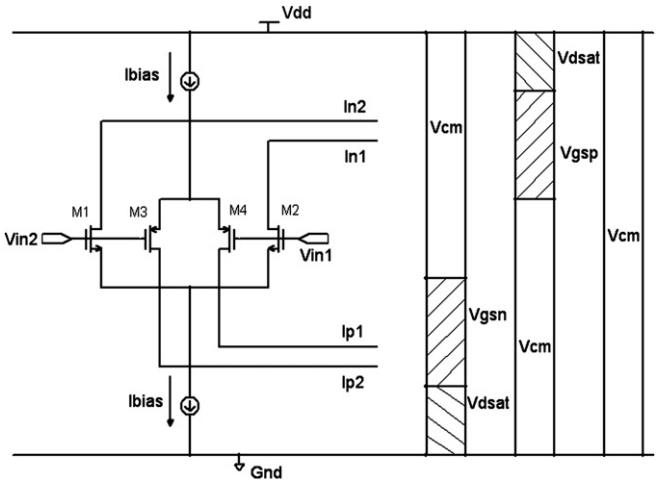

Fig. 1. Common-mode input range of the rail-to-rail input stage.

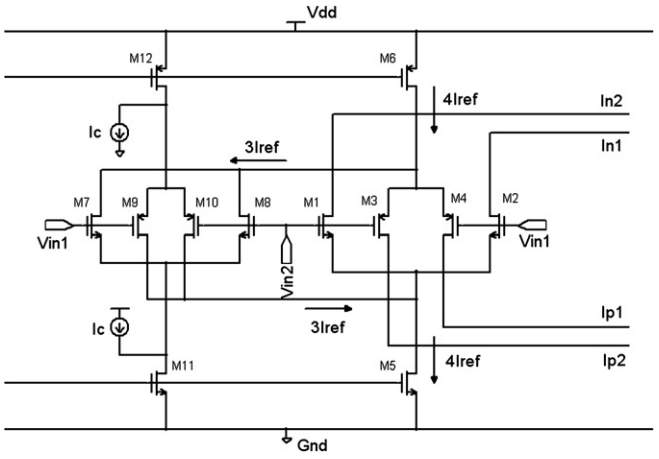

Fig. 2. Rail-to-rail input stage with gm-control dummy input differential pairs.

The large variation of the input stage transconductance prevents optimal frequency compensation, and introduces large variation in unity-gain signal distortion [6,7].

The g_m of input transistors is given by:

$$g_m = K(V_{GS} - V_{TH} = \sqrt{KI_{tail}} \tag{4}$$

$$\text{With} \quad K = \mu_P C_{OX}\left(\frac{W}{L}\right)_P = \mu_N C_{OX}\left(\frac{W}{L}\right)_N \tag{5}$$

where μ_N and μ_P are the mobility of the charge carriers, C_{OX} is the normalized oxide capacitance; W and L are the width and the length of a transistor, respectively. From Eq. (5) we can find out that for a constant-g_m the W over L ratios of the P-channel and the N-channel input pairs have to obey the following relation:

$$\frac{\mu_N}{\mu_P} = \frac{\left(\frac{W}{L}\right)_P}{\left(\frac{W}{L}\right)_N} \tag{6}$$

If the ratio μ_N over μ_P differs from its nominal value because of process variations, especially the temperature variation, the g_m will have an additional variation.

A number of schemes have been proposed to obtain a rail-to-rail constant-*gm*. A general approach is through controlling the DC tail currents of the differential input pairs by 1:3 current mirror circuit [4,8]. Our proposed circuit changes the tail current of the input differential pairs dynamically for a constant-g_m by using dummy input differential pairs, which have compensate current sources at the tail current transistors of each dummy input differential pairs.

2. Constant-g_m input stage

The basic structure of the proposed constant g_m input stage is illustrated in Fig. 2. The N-channel dummy input differential pair connects to the tail current transistor (M6) of P-channel input differential pair, and The P-channel dummy input differential pair connects to the tail current transistor (M5) of N-channel input differential pair. When there is only one active input pair, the dummy input differential pairs do not have any effect. When both differential pairs are in full operation, the dummy input differential pairs take away $3I_{ref}$ of the $4I_{ref}$ tail current. Now, the g_m of the three regions is:

Region I and Region III:

$$g_m(\text{eff}) = g_{mN} = g_{mP} = \sqrt{2K2I_{ref}} = 2\sqrt{KI_{ref}} \tag{7}$$

Region II:

$$g_m(\text{eff}) = g_{mN} + g_{mP} = \sqrt{\frac{2KI_{ref}}{2}} + \sqrt{\frac{2KI_{ref}}{2}} = 2\sqrt{KI_{ref}} \tag{8}$$

Compensate current I_C is implanted to the tail current transistors of each dummy input differential pairs in this structure. I_C is used for keeping M11 and M12 in triode region when dummy input differential pairs are turned off. This optimization can decrease the g_m variation, because M5 and M6 are in triode region when the input differential pairs are turned off. For example: when there is no I_C is implanted, and M7 and M8 are turned off, the drain-source voltage of M11 will be zero. Because no I_C is implanted, M7 and M8 will enter subthreshold region as soon as common-mode voltage is around the threshold voltage of NMOS transistor (V_{THN}); Comparing to input differential pairs (M1 and M2), they will enter subthreshold region as long as the common-mode voltage is higher than $V_{THN} + V_{DS5}$ as a result of drain-source voltage of M5 (V_{DS5}) which is operating in triode region; The dummy differential pairs will take effect before the same type input differential pairs, it is the main cause of g_m variation of this structure.

The value of compensate current is calculated by the following equation:

$$\frac{I_C}{3I_{ref} + I_C} = \frac{3I_{ref}}{4I_{ref}} \tag{9}$$

$$\text{Thus,} \quad I_C = 9I_{ref} \tag{10}$$

I_C is estimate through the proportion of triode region current and saturation current of tail current transistors. The effect of the compensate current is obvious and is shown in the simulation part of this paper.

3. Summing circuit and the entire input stage circuit

As shown in Fig. 3a, the current mirror, M20 and M21, together with the folded cascodes, M22-M25 which is connected with the input differential pairs, form a summing circuit. This summing circuit not only adds the signals coming from the complementary rail-to-rail input stage, but also increases the gain of the stage due to the high voltage gain of the folded cascodes. The summing circuit can be improved by using gain boosting technology as shown in Fig. 3b, when higher gain is needed [9]. A class AB output stage is preferred when driving low resistor. The entire input stage which is shown in Fig. 4 can be seen as a single stage amplifier, and be used to drive capacitors in VLSI system. M28 and M29 form compensate current sources connect to the dummy input pairs.

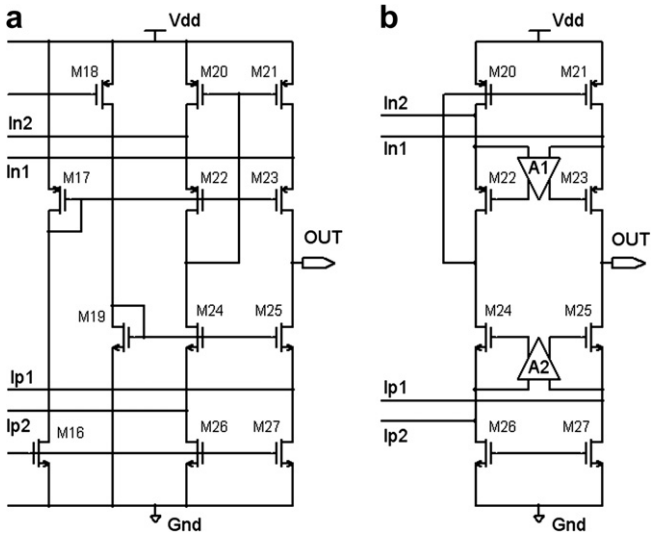

Fig. 3. (a) Folded cascodes summing circuit and (b) gain boosting technology implements in (a) for higher gain.

4. Simulation and analysis

Based on the proposed constant-g_m input stage, a rail-to-rail CMOS Op Amp input stage has been designed in

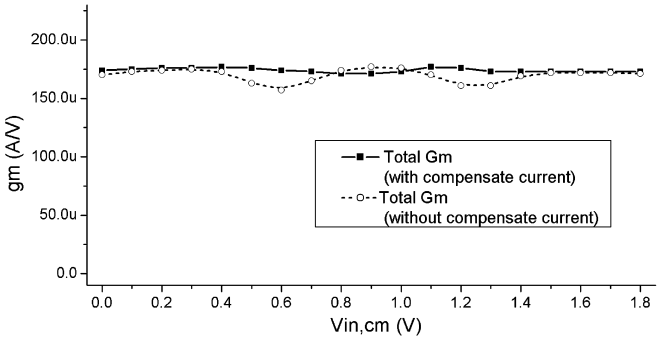

Fig. 5. Compare the g_m variation vs. V_{icm} of the circuit between with and without compensate current.

Table 1
Comparisons of the rail-to-rail amplifiers

	[1]	[2]	[9]	This work
Stages	2	1	2	1
Process	0.35 μm	0.35 μm	0.18 μm	0.18 μm
Supply voltage	1.5 V	3 V	1.8 V	1.8 V
g_m variation	3.4%	0.2%	4%	2%
Power	<319 μW	–	3.55 mW	<498 μW
DC gain	97 dB	>50 dB	100 dB	>61 db
Bandwidth	15.7 MHz	77.7 MHz	100 MHz	25 MHz
Phase margin	>55.5°	80°	47°	78°

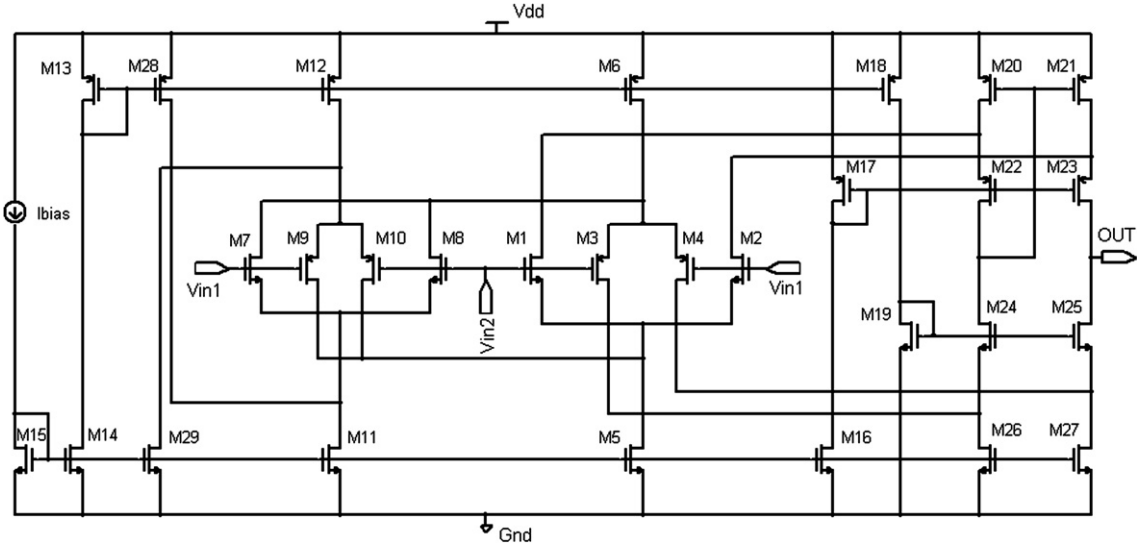

Fig. 4. Overall design of constant-gm rail-to-rail Op Amp input stage.

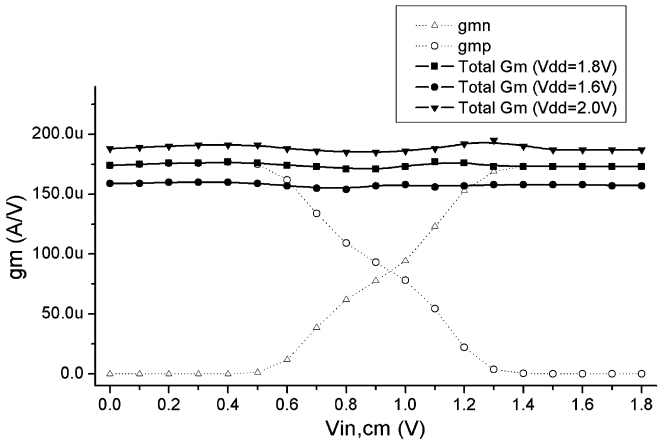

Fig. 6. Simulated g_m vs. V_{icm} of the input stage under different supply voltages.

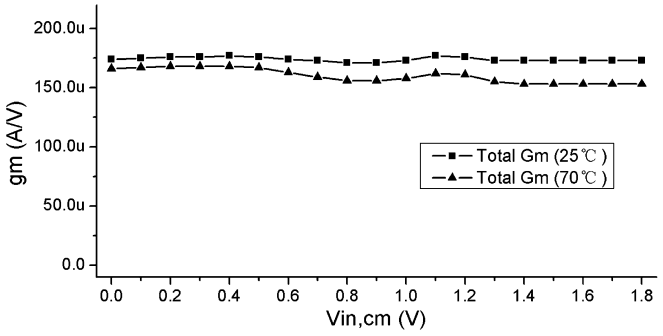

Fig. 7. Simulated g_m vs. V_{icm} of the input stage under different temperatures.

a standard 0.18 μm CMOS technology in which $V_{THN} \approx 0.48$ V, $V_{THP} \approx 0.46$ V. And Fig. 5 shows the simulated results of the total input stage transconductance versus V_{icm} for $I_{tail} = 40$ μA and $V_{DD} = 1.8$ V. The g_m variation is ±2% as simulated, the performance is evidently better than the circuit without compensate current. The largest g_m variation occurs at 0.5–0.6 V and 1.2–1.3 V of the common-mode voltage due to the reason mentioned above. The g_m variation not only caused by electric reasons, but also occurs with process mismatches. Obviously, the mismatch between $(W/L)_N$ and $(W/L)_P$ of the input differential pairs can cause the Δg_m between gm_N and gm_P. The dimension mismatches of M5, 11, 29 and M5, 12, 28 will make the input pairs tail current differ from designed ratio, which also cause g_m variation. According to Eq. (4), the mismatches of transistor dimension which cause ΔK has the same impact to g_m as the mismatch of I_{tail}^2, which means the mismatch of input pairs has more significant effect on total g_m variation than the mismatch of tail current mirrors. Designers should pay more attentions to these transistors' layout. The dummy pairs mismatch will not affect the circuit for its current is decided by the tail current mirrors. Some state-of-the-art techniques are compared as shown in Table 1.

Fig. 6 shows the variation of g_m under different supply voltages. The circuit works well when supply voltage changes within 10%. Fig. 7 shows the variation of g_m under different temperatures. As we can see, temperature has impact on the g_m variation in different V_{icm} values. This is caused by the complementary structure of the input stage, the mobility of electrons and holes response differently to temperature due to their different scatter mechanism [10]. The N-channel MOSFET is more sensitive to temperature, so its g_m drops more quickly when temperature goes up. Fig. 8 shows the AC response of the circuit, DC gain of this single stage amplifier is over 61 dB with 25 MHz bandwidth and 78° phase margin. The power of the circuit is less than 498 μW.

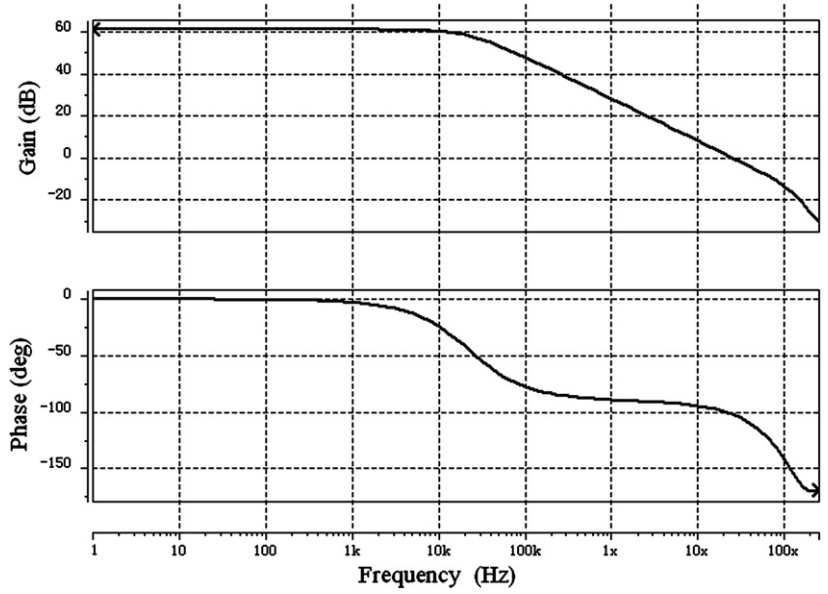

Fig. 8. AC response of the single stage amplifier.

There is one unanticipated phenomenon that the first order g_m calculation expression cannot explain: according to Eq. (4), g_m should increase with the increase of I_{tail}. As it is shown in the figures, g_m does not increase at the two edges of common-mode input range where the I_{tail} is larger than the intermediate range. On the contrary, it decrease slightly. This can be explain by the more specific g_m expression

$$G_m = K(V_{\text{GS}} - V_{\text{TH}})(1 + \lambda V_{\text{DS}}) \tag{11}$$

With λ is the channel length modulation parameter. For N-channel differential pair M1 and M2, their V_{DS} decrease when V_{icm} increases at the higher edge of the common-mode input range; For P-channel differential pair M3 and M4, their $|V_{DS}|$ decrease as soon as V_{icm} decreases at the lower edge of the common-mode input range. This phenomenon will be significant when the channel length decreases.

5. Conclusion

An improved constant-g_m and rail-to-rail operational amplifier input stage with 1.8 V supply in 0.18 μm standard CMOS technology has been presented. The circuit achieves nearly constant-g_m (within ±2%) behavior over the full input common-mode voltage range. The operation of the input stage under different supply voltages and temperature are simulated and analyzed. Mismatch issues on input transistors and current mirrors have been discussed. For better performance, second-order effects have been taken in consideration in this paper.

References

[1] Masoom A, Hadidi Kh. A 1.5-V constant-gm rail-to-rail input stage operational amplifier. In: IEEE Proceedings of the ISCAS'2006, December 10–13; 2006. p. 632–5.
[2] Song TY, Yan SL. A robust rail-to-rail input stage with constant-gm and constant slew rate using a novel level shifter. In: IEEE Proceedings of the ISCAS'2007, May 27–30; 2007. p. 477–80.
[3] Sakurai S, Ismail M. Robust design of rail-to-rail CMOS operational amplifiers for a low power supply voltage. IEEE J Solid-State Circ 1996;31(2):146–56.
[4] Hogervorst R, Wiegerink RJ, Jong PAL, Fonderie J, Wassenaar RF, Huijsing JH. CMOS low-voltage operational amplifiers with constant-gm rail-to-rail input stage. In: IEEE Proceedings of the ISCAS'92, May 3–6 1992, vol. 6. p. 2876–9.
[5] Razavi B. Design of analog CMOS integrated circuits. Boston: McGraw Hill; 2001.
[6] Chang IK, Park JW, Kim SJ, Kae DK. A global operational amplifier with constant-gm input and output stage. In: IEEE Proceedings of the TENCON'1999, vol. 2; 1999. p. 1051–4.
[7] Yan SL, Hu JY, Song TY, Edgar SS. A constant-gm rail-to-rail op amp input stage using dynamic current scaling technique. In: IEEE Proceedings of the ISCAS'2005, May 23–26, vol. 3; 2005. p. 2567–70.
[8] Huijsing JH, Hogervorst R, Langen KJ. Low-power low-voltage VLSI operational amplifier cells. IEEE Trans Circuits–I 1995;42(11):841–52.
[9] Huang HY, Wang BR, Liu JC. High-gain and high-bandwidth rail-to-rail operational amplifier with slew rate boost circuit. In: IEEE Proceedings of the ISCAS'2006, May 21–24; 2006. p. 907–10.
[10] Arora N. MOSFET models for VLSI circuit simulation theory and practice. Wien: Springer-Verlag; 1993.