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DC-bus power quality for aircraft power systems during generator fault conditions

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Abstract: Higher-voltage, 540 V, aircraft DC-bus power quality is examined experimentally and by computer simulation during a short-circuit fault across the phase terminals of a 70 kW, five-phase, permanent magnet fault-tolerant generator. The DC-bus transients caused by the short-circuiting of the generator phases are seen to exceed the limits in MIL-STD-704F and a control algorithm is proposed for a supercapacitor-based energy storage device that mitigates the transients. The controller performance is illustrated by computer simulations for a range of bus switching scenarios.

Nomenclature

C_{bus}	DC-bus capacitor
C_{sc}	supercapacitor
E	magnitude of back emf
I_{bus}	DC-bus current
$I_{ESD/sc}$	ESD/supercapacitor current
I_{gen}	generator total DC current
$I_{gen\text{-}AC}$	generator phase current
$I_{sc\text{-}F}$	fault mitigation control reference
$I_{sc\text{-}L}$	power balance control reference
$I_{sc\text{-}rc}$	supercapacitor recharge reference
k_c	current regulation proportional term
k_v	voltage regulation proportional term
L_{ESD}	ESD DC/DC converter inductor
L_s	stator inductance per phase
R_s	stator resistance per phase
T_c	current regulation integral term
T_e	generator torque
V_{bus}	DC-bus voltage
$V_{ESD/sc}$	ESD/supercapacitor voltage
α	fault angle
ω_c	current regulation bandwidth
ω_e	electrical angular frequency
ω_v	voltage regulation bandwidth

1 Introduction

The increasing use and criticality of electrical systems on-board aircraft is driving the development of new fault-tolerant generator technologies [1–4] and new power distribution systems such as higher-voltage DC networks [5–9]. However, the behaviour of these integrated systems under fault conditions is not well understood, especially the propagation of transients around the system, which, if uncontrolled, may lead to further equipment malfunction or failure. MIL-STD-704F [10] describes allowable DC-bus power quality limits in terms of voltage deviation and current ripple. Exceeding these limits, during load changes, bus switching events or fault conditions, may result in equipment going offline causing further disruption. In this paper, a supercapacitor-based energy storage device (ESD) is used to mitigate the DC-bus transients that result from short-circuit faults across the AC terminals of a five-phase fault-tolerant generator, load changes and voltage steps.

The generator is one of several technologies that are under investigation for embedding in the core of a jet engine, thereby simplifying the current mechanical power off-take arrangements. The generator has a permanent magnet rotor and five stator phases, each of which is electrically, magnetically and thermally isolated from the others [11]. Furthermore each phase has a high impedance which limits the current flowing in a terminal short-circuit to 1 p.u., enabling the machine to continue generating through the healthy phases when one or more windings has a short-circuit fault. However, faulting the generator phases is likely to affect adversely the power quality of the DC-bus, possibly exceeding the voltage deviation limits defined in MIL-STD-704F [10], which is the closest applicable standard.

DC systems are of increasing interest for power distribution on-board aircraft because of the lower system weight that arises from smaller cables and the reduced number of power electronic interfaces [12]. Also, the ability to parallel generators that may be operating asynchronously provides increased power management flexibility. The 270 V DC systems [5, 6] are currently operating on some military

aircraft, and ±270 V DC (540 V) systems are now being suggested [8] for a wider range of higher-power applications. However, a number of technical challenges is limiting the development of DC networks such as managing the interactions within the system, interrupting fault currents [8], protection [7, 13] and safety issues. This paper proposes techniques to limit the propagation of generator faults within a 540 V DC system.

The system under investigation in this paper is first described, followed by experimental results showing short-circuit generator faults. The controller for the ESD is then presented followed by simulation results.

2 System configuration

The outputs of the five-phase generator are connected to a 540 V (±270 V) DC-bus, which supplies a combination of resistive power load and constant power load (CPL) [14] units (Fig. 1). The system also includes an ESD comprising a supercapacitor bank and bi-directional DC/DC converter. Supercapacitor energy storage is used as the key characteristics of this technology; high power density and fast charge/discharge rates [15] are complementary to the generators' electrical characteristics.

The primary function of the ESD is to meet transient load demands, thereby protecting the generator and aircraft engine from rapid and/or repetitive load changes [16]. A similar aircraft system with an ESD is considered by Zhang *et al.* [9]; however, the primary objectives of the energy storage control in [9] are to maintain the main generator online and to share the power between the generator and the ESD.

To preserve the fault-tolerance of the generator system, shown in Fig. 1, each phase winding is passed through a separate H-bridge AC/DC converter. The PWM controllers on each H-bridge ensure that the generator currents are sinusoidal and also regulate the DC-bus voltage [17]. Load sharing between the H-bridge converters is achieved using simple droop controllers. The generator has a rating of 70 kW, a base speed of 1000 rpm and a base electrical frequency of 233 Hz; the nominal DC-bus voltage is set at 540 V and the DC output voltage of the H-bridges is set to droop by 20 V at full load [18]. The total capacitance on the 540 V bus is 800 μF and the bandwidth of the generator controller is 60 rad/s.

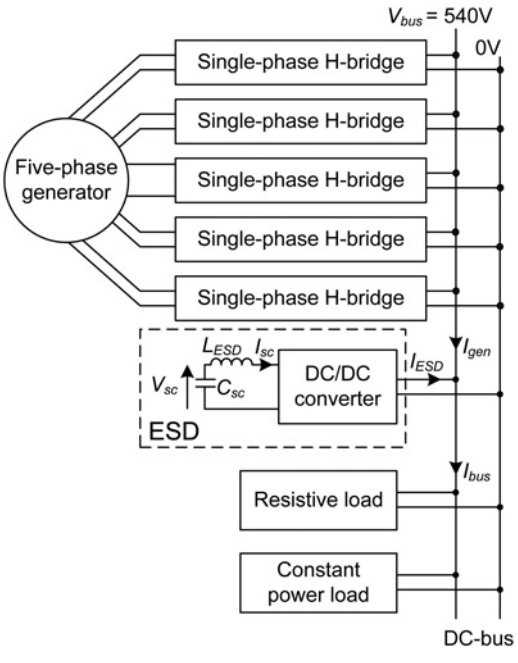

Fig. 1 *System configuration*

In the following sections experimental measurements and simulation results are presented to examine the effect of a short-circuit fault across one of the generator phase terminals. Large voltage deviations in DC-bus voltage are observed, partly at least because of the relatively small value of DC-bus capacitance, and this in turn is due to the requirement to avoid electrolytic capacitor types in aerospace systems. As there are no published standards for the power quality of 540 V DC aerospace systems, the results are compared with the limits in MIL-STD-704F [10], which relates to 270 V DC supplies. Since the observed deviations in DC-bus voltage during a generator terminal short-circuit fault are well outside the limits set by MIL-STD-704F, the control system for the ESD is modified to provide voltage support for the DC-bus. The system performance during multi-phase generator short-circuit winding faults is examined in subsequent sections by means of simulation and is seen to meet the requirements of MIL-STD-704F.

3 Validated single-phase fault response

For convenience the short-circuit fault was applied to the machine winding through the converter by halting the PWM signals so that the top switch in each H-bridge converter leg was permanently closed with the bottom switches open [17]. This condition is representative of the system response to either a machine winding or IGBT fault. In the event of an IGBT short-circuit fault, the system response would be to switch on the corresponding healthy device in the other leg, placing a short-circuit across the phase terminals.

A Simulink-based simulation of the system was developed using lossless averaged-value models of the power electronics. The generator was modelled as five sinusoidal back emfs in series with the corresponding winding inductance and resistance. Friction and windage losses were omitted. In these initial tests the ESD was not connected.

An analytical solution for the short-circuit current in the faulted phase may be derived assuming constant phase inductance and neglecting eddy current effects. The phase equivalent circuit following the short-circuit fault [3, 19] is therefore the back emf, $E\cos(\omega_e t)$, in series with the winding resistance and inductance, R_s and L_s. Assuming that the terminal short-circuit is applied at $t = \alpha/\omega_e$, the post-fault current may be expressed as

$$I_{\text{gen-AC}} = \frac{E}{|Z|}\cos(\omega_e t - \angle Z) + I_e \exp\left\{\frac{-R_s}{L_s}\left[t - \frac{\alpha}{\omega_e}\right]\right\} \quad \text{for } t \geq \frac{\alpha}{\omega_e} \tag{1}$$

where $I_e = -(mV_{bus}/|Z|)\cos(\alpha - \delta - \angle Z)$ and $Z = R_s + j\omega_e L_s$, ω_e is the electrical frequency and δ and m are the angle and the depth of modulation of the H-bridge AC input voltage immediately before the fault is applied.

Fig. 2 shows the response of the generator to a single-phase short-circuit fault on phase 'c' at approximately $t = 1.03$ s. Experimental results [17] are shown in Figs. 2*a* and *b* and results from the averaged-value model in Figs. 2*c* and *d*. The initial operating condition was all five generator phases

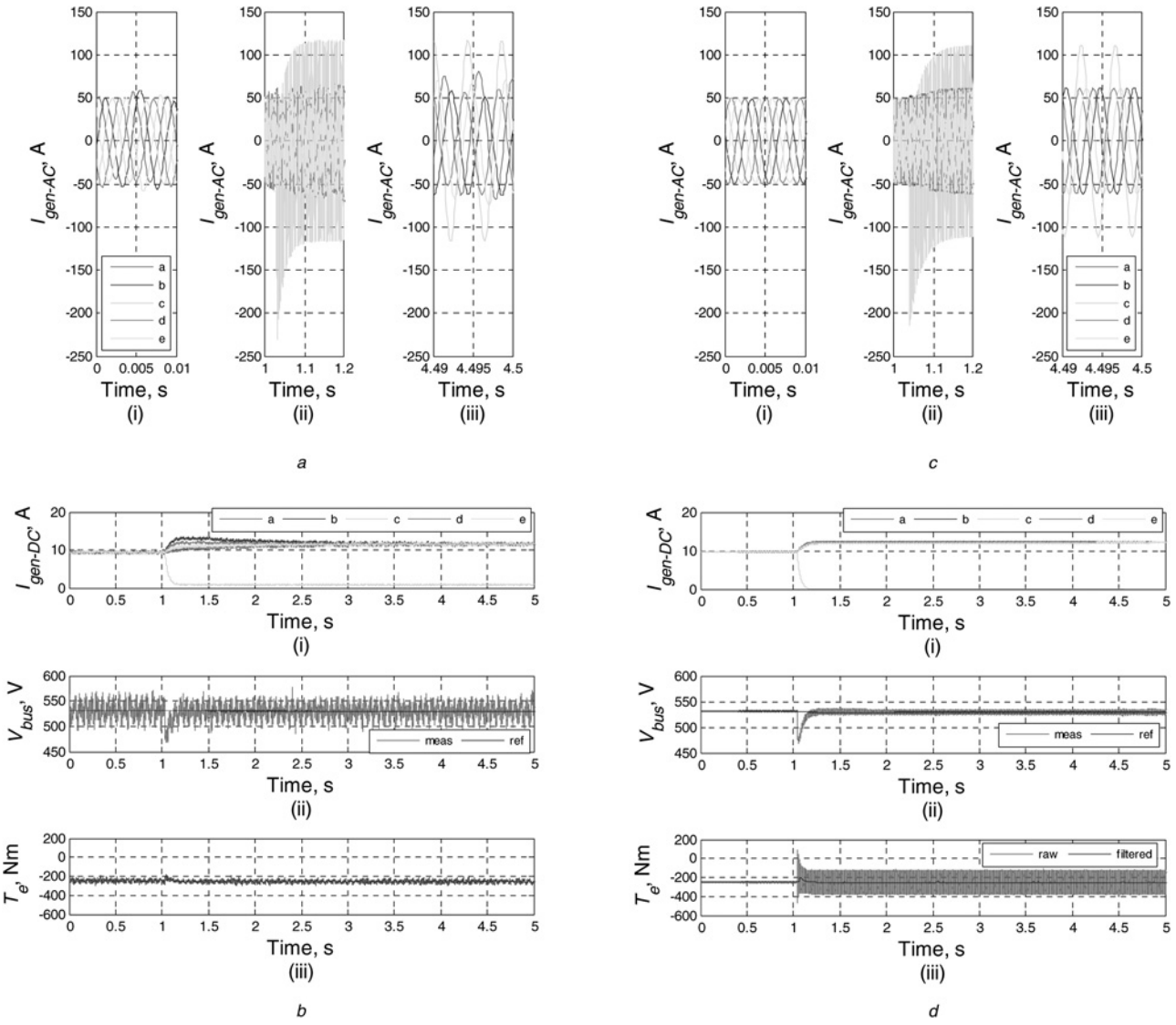

Fig. 2 *Single-phase short-circuit at t = 1.03 s, 1001 rpm, 540 V, with a 26.7 kW resistive load*

a Experimental result [17]
b Experimental result [17]
c Simulation result
d Simulation result

active at 1001 rpm, 540 V nominal DC-bus voltage and a 26.7 kW resistive load. The per-phase AC and DC currents, $I_{\text{gen-AC}}$ and $I_{\text{gen-DC}}$, respectively, DC-bus voltage, V_{bus}, and torque, T_{e}, are shown in the results. $I_{\text{gen-DC}}$ is filtered by a 4.66 Hz low-pass filter to remove the second-harmonic component prior to its use in the generator droop controllers which ensure balanced phases.

Prior to the fault, $t < 1.03$ s, the five machine phases share equally the 26.7 kW load power as shown by the AC current in Figs. 2*a*(i) and *c*(i). In both plots the per phase AC currents are 72° phase displaced and approximately 50 A in magnitude with a phase sequence of 'a', 'b', 'c', 'd' 'e'. Figs. 2*b*(i) and *d*(i) show $I_{\text{gen-DC}}$ per phase, which are identical prior to the fault at 9.4 A.

Phase 'c' is switched to a short-circuit fault at $t = 1.03$ s. Figs. 2*a*(ii) and *c*(ii) show $I_{\text{gen-AC}}$ in the faulted phase, phase 'c', rising to the 1 p.u. value (116 A) because of the high winding inductance. The peak transient current from (1) is −208 A settling to 1 p.u. after approximately 160 ms, which is consistent with $I_{\text{gen-AC}}$ peak in Figs. 2*a*(ii) and *c*(ii). $I_{\text{gen-AC}}$ in the remaining four phases, Figs. 2*a*(iii) and *c*(iii), show a slight increase to approximately 60 A as the controller now regulates these phases to share the total power. $I_{\text{gen-DC}}$ in the faulted phase, phase 'c', falls to zero in Figs. 2*b*(i) and *d*(i) and the outputs of the remaining four phases increase to 11.5 A to maintain the load requirements; this is possible as prior to the fault the phases were operating below the 14 kW maximum.

A negative deviation in the DC-bus voltage, V_{bus}, is apparent when the short-circuit is applied, shown in Figs. 2*b*(ii) and *d*(ii). V_{bus} falls to 467 V in the simulation and 468 V in the test results. This 73 V deviation in bus voltage marginally exceeds the +60/−70 V limit in MIL-STD-704F for a 270 V bus. A significant ripple component is apparent on V_{bus} in the test results, Fig. 2*b*(ii), which was attributed to parasitic effects in the system and measurement noise. The 5 V amplitude second-harmonic V_{bus} ripple during faulted operation, Fig. 2*d*(ii), is within the 6 V amplitude allowed in MIL-STD-704F. The reference value for the bus voltage is determined by the droop control and in Figs. 2*b*(ii) and *d*(ii) is 531.6 V at $t < 1.03$ s and 529.6 V when the system is in a steady-state post-fault.

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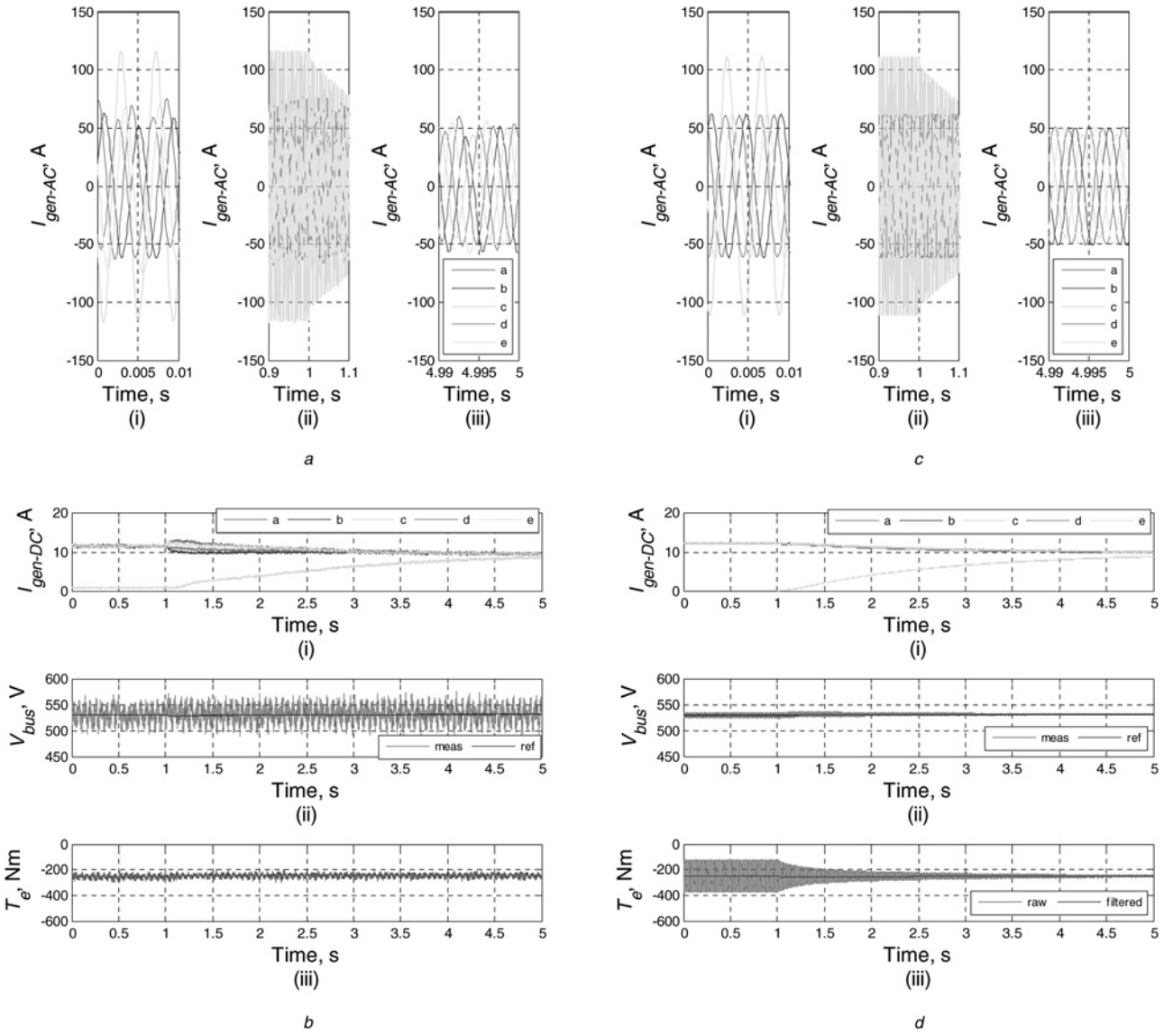

Fig. 3 *Single-phase fault recovery at t = 1 s, 1001 rpm, 540 V, with a 26.7 kW resistive load*

a Experimental result [17]
b Experimental result [17]
c Simulation result
d Simulation result

A slight deviation is noticeable in the generator torque, T_e, Figs. 2*b*(iii) and *d*(iii) after fault occurrence. The simulation results, raw data in Fig. 2*d*(iii) (dark grey trace), show a second-harmonic ripple (466 Hz) in T_e, which is due to the unbalanced conditions when only four phases are active; however, owing to the limited bandwidth of the mechanical couplings and the torque transducer, this is not evident in the experimental results, Fig. 2*b*(iii). For comparison the simulated T_e data are filtered, black trace in Fig. 2*d*(iii), and correlates closely with the measured T_e in Fig. 2*b*(iii).

The recovery of a single faulted phase at $t = 1$ s is shown in Figs. 3*a* and *b* for the test-rig and Figs. 3*c* and *d* for the averaged-value simulation. Figs. 3*a*(i) and *c*(i) show the fault on phase 'c' approximately 1 p.u. magnitude with the remaining phases generating the 26.7 kW load power at 1001 rpm and approximately 66 A. Phase recovery is initiated by restarting the PWM for phase 'c' at $t = 1$ s, shown in Figs. 3*a*(ii) and *c*(ii) Initially, within 500 ms, the controller reduces the phase 'c' current from the fault level, and then, gradually, over a period of 3–4 s the active power drawn from the phase is increased. There is a corresponding increase in the DC output current from phase 'c' and a complementary reduction in the output currents from the other phases as they adjust to share the total load current equally, Figs. 3*b*(i) and *d*(i). When the recovery of phase 'c' is initiated there is only a very slight disturbance in V_{bus} and T_e, Figs. 3*b*(ii), *b*(iii), *d*(ii) and *d*(iii), as the fault current is brought under control. Also the second-harmonic component in T_e, which is particularly evident in the simulation, is virtually eliminated once phase recovery is complete. The experimental results confirm the accuracy of the simulation model.

4 Control of energy storage device

A multi-functional controller for the ESD is described which regulates the supercapacitor current to meet transient load changes on the DC-bus, manages the supercapacitor state of charge and mitigates DC-bus voltage transients such as those caused by generator short-circuit faults.

Supercapacitor-based energy storage is proposed for a variety of applications in published literature, often as a power buffer between the load and the main power source [9, 20–29]. The control schemes are often based on a power balance between the individual hardware elements that form the system [20–22, 25–28]. These control schemes are inappropriate for this application, for example they are based on the vehicle speed [22], committed power generation [20, 26], generator speed-droop characteristic [27], estimated diesel engine output [25], or are designed to enable the main power source to have a constant output [21] or require many system level measurements [28], which if extrapolated to an aircraft system would be unmanageable and may introduce communication difficulties. DC-bus voltage control schemes [23, 24, 29] for the ESD are not appropriate here as the bus voltage in this work is regulated by the two generator controllers.

The ESD shown in Fig. 1 is primarily intended to protect the generator and gas engine from rapid load transients, thereby limiting the rate-of-change of torque applied by the generator on the engine [16]. However, it is shown later in this section, Section 4.3, that under severe DC-bus voltage transients the ESD can enter a runaway mode, owing to the action of the ESD control, and collapse the DC-bus, therefore an additional control function is introduced to mitigate the voltage transients.

4.1 Control structure

The ESD, Fig. 4, comprises a 55F supercapacitor bank with a maximum voltage of 145 V and approximately 0.4 MJ of usable energy capacity and a simple, unisolated, bi-directional DC/DC converter [16].

A closed-loop controller is used to regulate the supercapacitor current, I_{sc}, and the reference value for the current controller is determined by the combination of three signals. The first, $I_{sc\text{-}L}$, is determined by the instantaneous DC-bus power calculation ($V_{bus} \times I_{bus}$ – where V_{bus} and I_{bus} are the bus voltage and current), which is then divided by supercapacitor voltage, V_{sc}. This forces the ESD to respond to instantaneous load changes on the DC-bus. The supercapacitor state-of-charge is managed by the second signal, $I_{sc\text{-}rc}$, which is determined by the error between the supercapacitor reference voltage, V_{sc}^{*}, here 135 V, and the actual voltage. The third component, $\boldsymbol{I}_{sc\text{-}F}$, is determined by the error between the DC-bus voltage and the nominal set-point. This enables the ESD to support the bus voltage during generator faults.

4.2 Current control

The current control loop was designed using the averaged-value differential equations for the DC/DC converter, which assume lossless operation and ideal switches

$$\dot{I}_{sc} = \frac{V_{sc} - V_{bus}(1-D)}{L_{ESD}} \tag{2}$$

$$\dot{V}_{bus} = \frac{I_{sc}(1-D) - I_{bus} + I_{gen}}{C_{bus}} \tag{3}$$

where D is the duty-ratio of $S2$ and $(1-D)$ is the duty ratio of $S1$, I_{gen} is the total generator DC current, L_{ESD} is the DC/DC converter inductor and C_{bus} is the combined filter capacitance on the DC-bus.

A non-linear compensator is used to simplify the design of the current control loop in Fig. 4. The duty-ratio signal D is calculated by the non-linear compensator as shown in (4), where V_{ESD}^{*} is the output signal from the PI controller, Fig. 4. By substituting (4) into the converter differential equation, (2), the overall transfer function between the control signal V_{ESD}^{*} and the supercapacitor current, I_{sc}, is seen to have a simple linear first-order form, (5).

$$D = 1 - \frac{V_{sc} - V_{ESD}^{*}}{V_{bus}} \tag{4}$$

$$\frac{I_{sc}}{V_{ESD}^{*}} = \frac{1}{sL_{ESD}} \tag{5}$$

Assuming that the PI controller has the form $PI(s) = k_c((1 + T_c s)/T_c s)$, where k_c and T_c are the proportional and integral terms, respectively, then a unity gain cross-over frequency of ω_c may be obtained for the control loop by choosing $k_c = \omega_c L_{ESD}$ and $T_c = \sqrt{10}/\omega_c$.

The ESD was assumed to have a switching frequency of 30 kHz, the filter inductor was 100 μH and the current

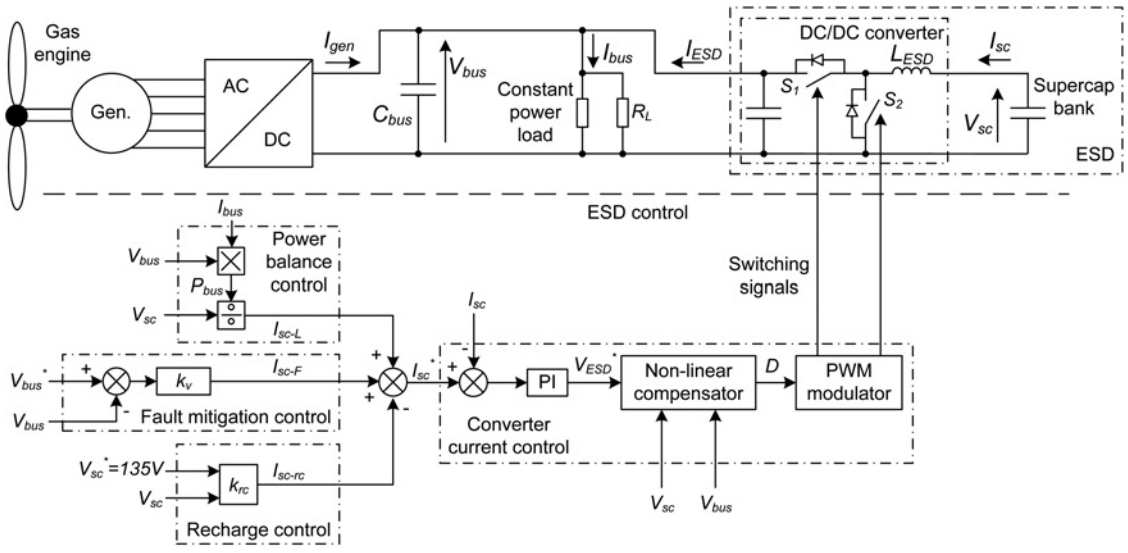

Fig. 4 *Overall system schematic including ESD control*

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controller bandwidth was set at 8 kHz by choosing $k_c = 5.03$ and $T_c = 62.9$ μs. The resultant phase margin was 43°.

4.3 Fault mitigation controller

To illustrate the need for the fault mitigation controller, Fig. 5 shows results from a Simulink simulation of the system when a short-circuit fault is simultaneously applied to three of the generator phases. The fault is applied at approximately $t = 5$ s and the DC-bus has a 14.6 kW resistive load and a 4.75 kW CPL. The parameters of the ESD controller are as given in Section 4.2. Fig. 5 shows the five generator phase currents, the DC-bus voltage and the three components of the DC system current; the generator output current, I_{gen}, the overall load current, I_{bus}, and the ESD current, I_{ESD}.

Pre-fault phase currents are 35 A, displaced by 72°. At approximately $t = 5$ s three phases, 'a', 'b' and 'c', of the five-phase generator are short-circuited and after an initial transient settle at 1 p.u. current. The two remaining active phases, 'd' and 'e', increase to 90 A to supply the load. The imposition of the fault results in a very severe DC-bus voltage transient, Fig. 5(iii), which appears to the ESD power balance controller as a sudden reduction in DC-bus power, therefore the ESD responds with a negative I_{ESD}, light grey trace in Fig. 5(iv), drawing power from the DC-bus which further reduces the DC-bus voltage.

Just after $t = 5.02$ s the ESD exceeds its maximum current of 60 A and trips out, allowing the DC-bus voltage to recover through the action of the generator controller, which increases

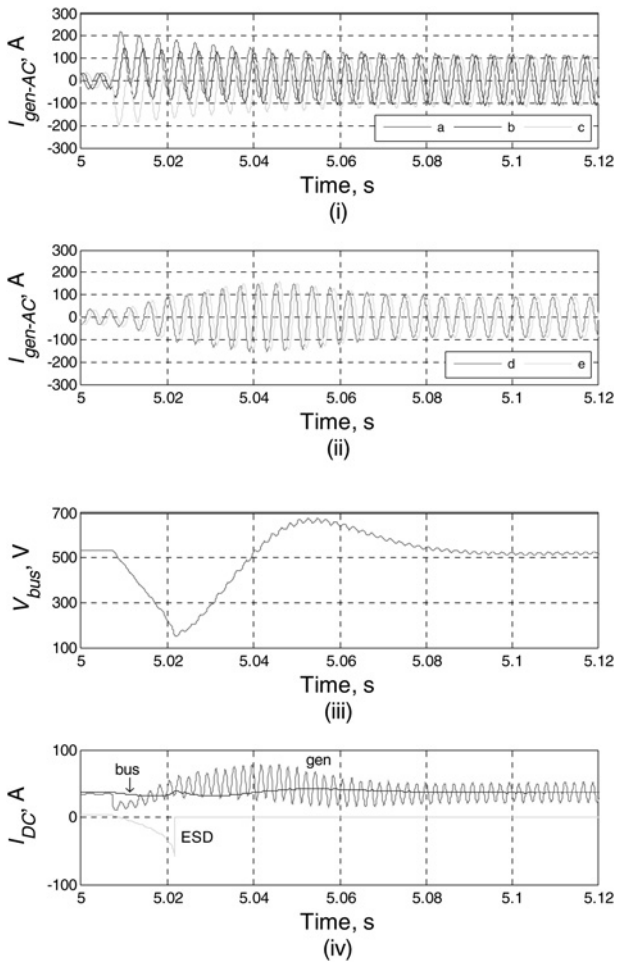

Fig. 5 *System behaviour with a 14.6 kW resistive load and 4.75 kW CPL; $I_{sc\text{-}F} = 0$*

the power drawn from the remaining healthy phases to meet the load demand, Fig. 5(ii). Had the ESD not tripped out, the DC-bus voltage would have collapsed to the supercapacitor voltage level, forward biasing the diode in the DC/DC converter, and probably resulting in equipment failure.

To prevent the ESD from collapsing the DC-bus, the fault mitigation control function is added to the ESD system as shown in Fig. 4. A signal $I_{sc\text{-}F}$ is added to the supercapacitor current demand based on the error between the reference and actual bus voltage multiplied by a proportional gain, k_v. To ensure that the power balance control function does not degrade the DC-bus power quality during bus voltage transients k_v must be chosen such that

$$\left|\frac{\partial I_{sc\text{-}F}}{\partial V_{bus}}\right| \geq \left|\frac{\partial I_{sc\text{-}L}}{\partial V_{bus}}\right| \Rightarrow k_v \geq \left|\frac{I_{bus}}{V_{sc}}\right| \tag{6}$$

For the system under consideration here, the maximum value of I_{bus} is 130 A corresponding to 70 kW, whereas the minimum V_{sc} is assumed to be 100 V, implying a minimum value of k_v of 1.3.

However, using a larger value will result in the ESD tending to mitigate transient deviations in the DC-bus voltage. The maximum value of k_v is limited by stability concerns. From (3) the transfer function between V_{bus} and I_{sc}^* may be approximated by (7) within the current control loop bandwidth.

$$\frac{V_{bus}}{I_{sc}} = \frac{(1-D)}{sC_{bus}} \tag{7}$$

Therefore to limit the bandwidth of the voltage control loop to ω_v, the proportional gain k_v must be equal to $\omega_v C_{bus}/(1-D)$. For the system under consideration, choosing $k_v = 15$ sets the bandwidth of the voltage control loop at 800 Hz, well below the current control loop bandwidth to prevent any interactions between the loops.

4.4 State-of-charge controller

The state-of-charge controller provides a contribution, $I_{sc\text{-}rc}$, to the overall supercapacitor current reference, I_{sc}^*, based on the error between the actual supercapacitor voltage and its fully charged value, which is 135 V in this case. Since under steady-state conditions the supercapacitor current tends to zero, then the $I_{sc\text{-}rc}$ and $I_{sc\text{-}L}$ components of supercapacitor current must be equal, resulting in the supercapacitor voltage falling with increasing DC-bus power. This ensures that the supercapacitor is fully charged under no-load conditions and is therefore able to supply transient load increases. In contrast, the supercapacitor will be heavily discharged when the DC-bus is fully loaded and therefore able to absorb power in the event of transient load decreases.

A non-linear recharge function, $k_{rc} = 0.64(V_{sc}^* - V_{sc})^2$, was used to regulate the supercapacitor voltage recharge. k_{rc} was chosen to give a 33 V drop in V_{sc} at 70 kW load power, as shown in Fig. 6, and results in the ESD output settling in approximately 10 s.

An additional droop in V_{sc} with DC-bus power occurs because of the action of the fault mitigation control function, which produces a non-zero output under steady-state conditions. This is because the DC-bus voltage droops with load owing to the action of the generator control unit,

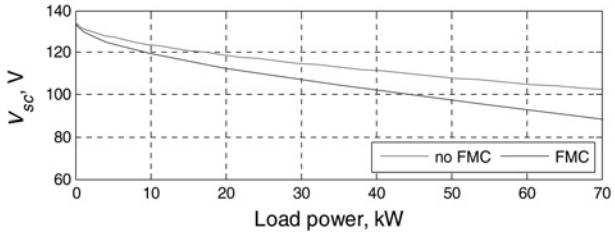

Fig. 6 *Supercapacitor voltage droop characteristic*

whereas the nominal DC-bus voltage is used as the reference signal in the fault mitigation function. The effect on the steady-state supercapacitor voltage is seen in Fig. 6, which shows the voltage with and without the fault mitigation controller active.

5 Multi-phase fault response with energy storage device

The DC-bus voltage and generator torque are examined in this section by means of simulation during multi-phase generator faults with combined resistive and CPLs on the bus, both with and without the ESD. All results relate to three generator phases suffering simultaneous short-circuit faults, with all phases being faulted on the zero crossing of phase 'a' terminal voltage, which results in a higher deviation in DC-bus voltage compared to the staggered faulting of the phases.

5.1 Combined resistive and constant power load

The bus is nominally loaded with 14.6 kW of resistive load and 9.5 kW of CPL which, when combined, is approximately the maximum power output of two active phases. The speed is constant at the minimum operating speed of 1000 rpm as the phase current and torque are highest. The above conditions result in one of the worst-case scenarios for the generator in normal service.

Fig. 7(i) shows the AC-current of the faulted phases and the Fig. 7(ii) shows the AC current of the healthy phases. The phase currents are plotted separately for clarity. Fig. 7(iii) shows bus voltage and Fig. 7(iv) is the generator torque.

In Figs. 7 and 8 the bus is initially loaded with 14.6 kW of resistive load and 9.5 kW of CPL and all five generator phases are active. $I_{\text{gen-AC}}$ per phase are 72° phase displaced with respect to the adjacent phase and all are 46 A. At $t = 5$ s three generator phases, 'a', 'b' and 'c', suffer short-circuit faults. $I_{\text{gen-AC}}$ 'a', 'b' and 'c' increase to a magnitude of 1 p.u. and $I_{\text{gen-AC}}$ 'd' and 'e' increase to 116 A to maintain power to the loads. At $t = 10$ s the 9.5 kW CPL is turned off for 5 s and then turned on again and finally at $t = 25$ s the three generator phases are restarted, $I_{\text{gen-AC}}$ 'd' and 'e' reduce to 70 A when the CPL is off and then increase to 116 A when the CPL is restarted. $I_{\text{gen-AC}}$ 'a', 'b' and 'c' are unaffected by the changes in CPL. When the phases are restarted $I_{\text{gen-AC}}$ are automatically adjusted by the control to be 46 A so that all phases equally share the load.

In Fig. 7, with the ESD inactive, fault occurrence at $t = 5$ s results in V_{bus} deviations of +206/ −282 V, exceeding the MIL-STD-704F limits of +60/ −70 V for a 270 V system. Switching the 9.5 kW CPL off at $t = 10$ s and back on at $t = 15$ s also results in large bus transients. Owing to the controller design, the phase recovery at $t = 25$ s results in a gradual adjustment of the generator currents and virtually no deviation in V_{bus}, Fig. 7(iii). Fault and bus load changes

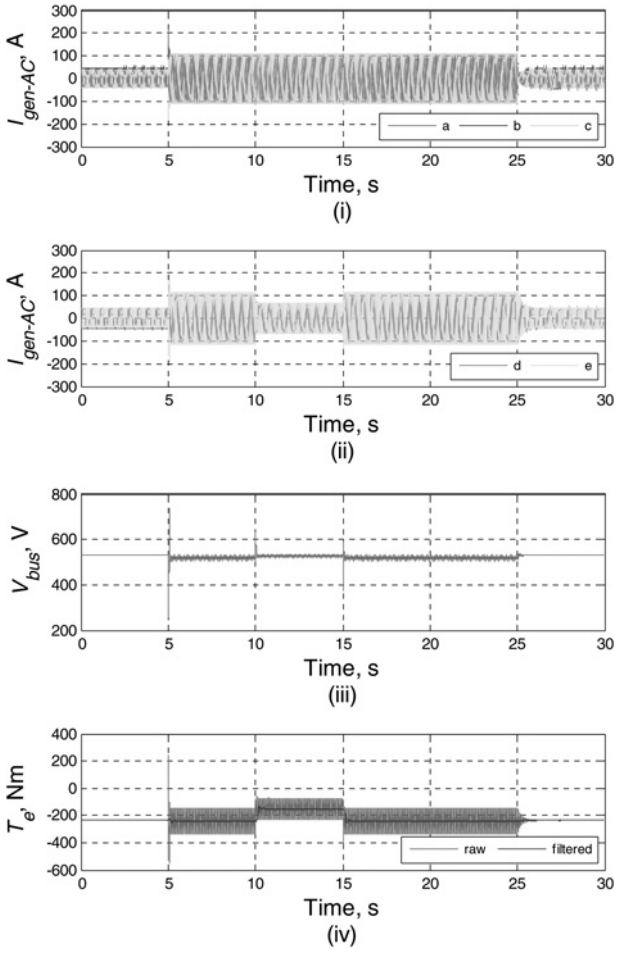

Fig. 7 *System behaviour with 14.6 kW resistive and 9.5 kW CPL; ESD inactive*

at $t = 5$, 10 and 15 s result in large transients in AC-current, $I_{\text{gen-AC}}$, and torque, T_{e}, Figs. 7(i), (ii) and (iv).

During the faulted generator condition when only two phases are active, $5 < t < 25$ s, the second-harmonic component is noticeable on V_{bus} and T_{e}, Figs. 7(iii) and (iv); outside this time range the second-harmonics of the five active phases cancel. A 96 N m second-harmonic ripple is apparent on T_{e} during the high-load conditions $5 < t < 10$ s and $15 < t < 25$ s, which would be attenuated by the mechanical system in practice. The 8.5 V amplitude second-harmonic ripple on V_{bus} during high-load exceeds the MIL-STD-704F limit of 6 V.

Fig. 8 shows the system behaviour for the same events as in Fig. 7 but with the ESD active. Fig. 8(i) shows $I_{\text{gen-AC}}$ of the faulted phases and Fig. 8(ii) shows $I_{\text{gen-AC}}$ of the healthy phases. The deviations in V_{bus}, Fig. 8(iii), are almost eliminated at the instants of fault occurrence and load switching; the minimum and maximum values of V_{bus} being 514 and 530 V, well within the MIL-STD-704F limits. $I_{\text{gen-AC}}$ and T_{e} (Figs. 8(i), (ii) and (iv)) exhibit very mild variations except at fault occurrence because of the ESD, which rapidly responds to V_{bus} deviations in the case of faults or phase recovery by supplying/drawing power to/from the bus. The high current and torque peaks immediately after fault occurrence are unchanged in Figs. 7 and 8 as the ESD has no direct effect on generator currents.

The second-harmonic torque ripple is unchanged in Fig. 8 since there is no change in the generator currents. However, the DC-bus voltage ripple is reduced from 8.5 V, in Fig. 7,

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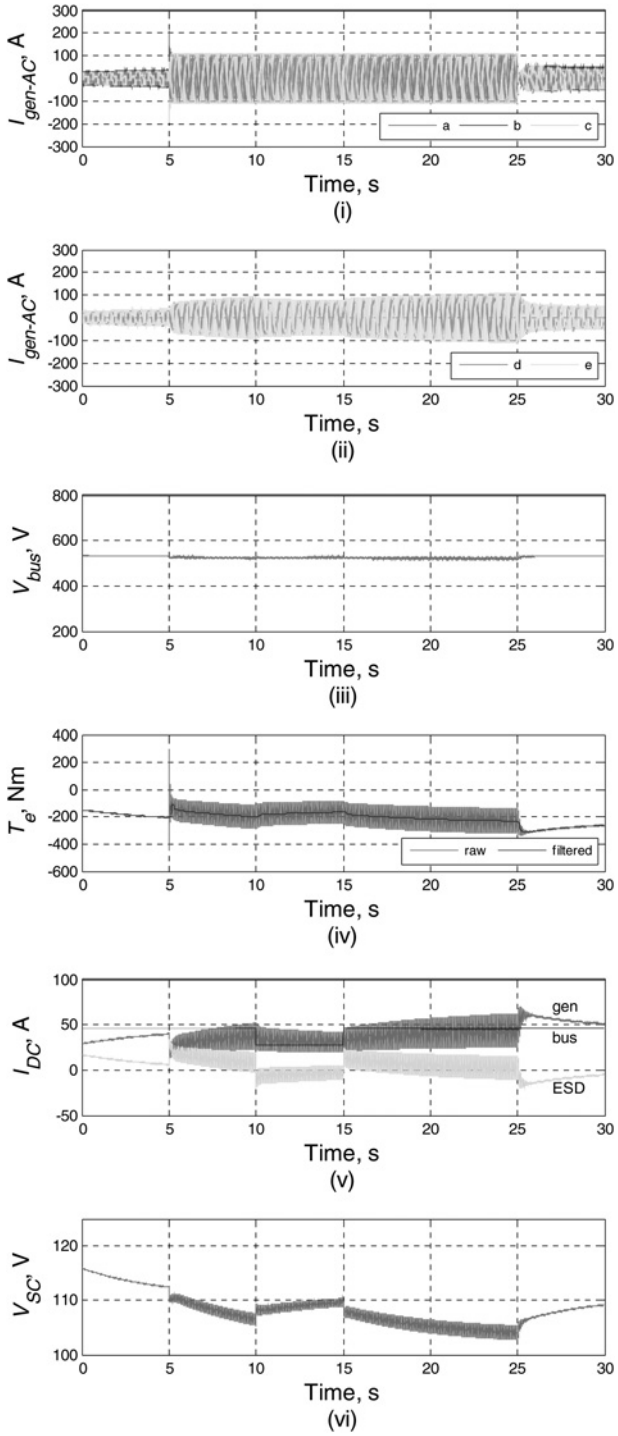

Fig. 8 *System behaviour with 14.6 kW resistive and 9.5 kW CPL; ESD active*

to 6.3 V in Fig. 8 by the action of the fault mitigation function, which produces a component of ESD current, that is, in anti-phase with the generator second-harmonic current. The cancellation of second-harmonic current is far from complete because of the relatively low bandwidth (800 Hz) of the fault mitigation loop in the ESD. Furthermore this effect will be less pronounced at higher generator speeds. Fig. 8(v) shows the contributions of the generator and ESD to bus current, the second-harmonic component in I_{ESD} is clearly visible during faulted operation. Negative ESD current, and an increase in V_{sc}, Fig. 8(vi), indicates power drawn from the bus. The ESD output settles to zero in approximately 10 s.

5.2 Entirely constant power load

Fig. 9 shows the system behaviour when a 24 kW CPL is present on the DC-bus with the generator and ESD active during bus voltage switching, load switching and generator fault events. In Fig. 9 the bus voltage reference value is initially 540 V and at $t = 2$ s the voltage reference is increased to 560 V with a 10 ms rise time, at $t = 5$ s three generator phases, 'a', 'b' and 'c', suffer short-circuit faults and are restarted 9 s later, between $9 < t < 11$ s the CPL is halved to 12 kW and finally at $t = 17$ s the voltage reference is restored to 540 V over 10 ms.

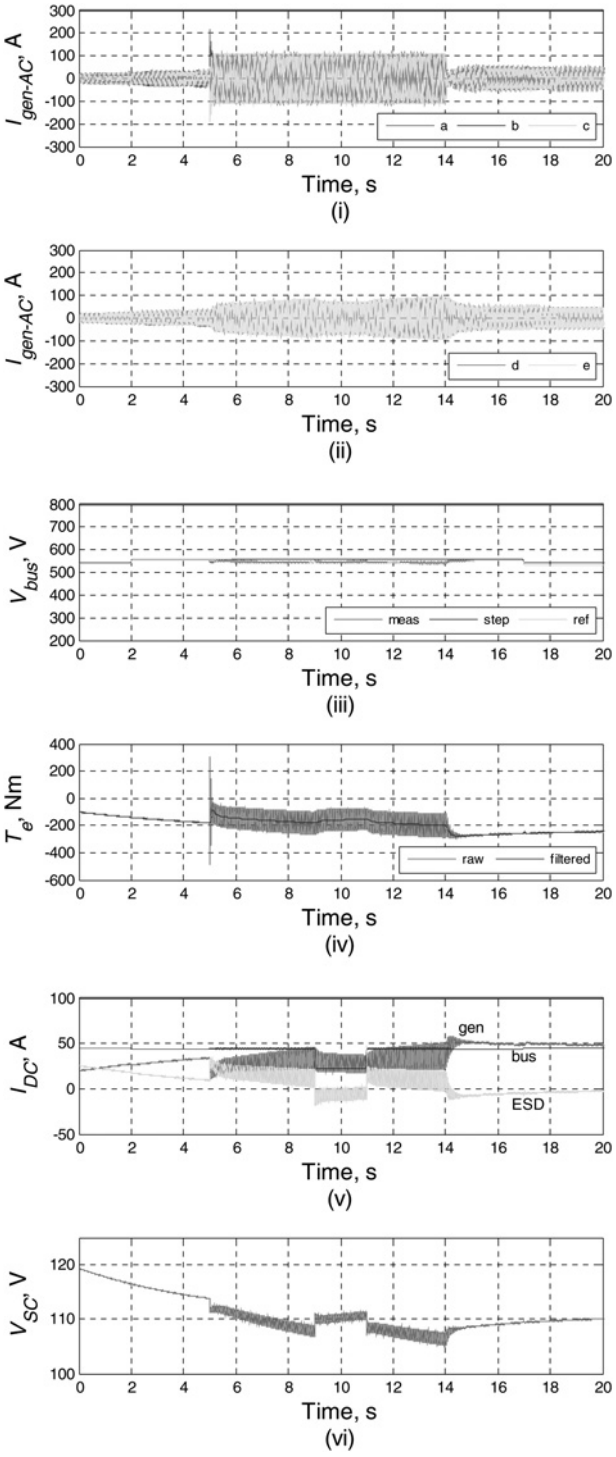

Fig. 9 *System behaviour with 24 kW CPL during V_{bus}^* switching events; ESD active*

In Fig. 9 steps in bus voltage reference, V^*_{bus}, at $t = 2$ s and $t = 17$ s result in a controlled response in V_{bus}, Fig. 9(iii), because of the combined action of the generator control and ESD. The ESD shows a small deviation in output (3 A), Fig. 9(v), because of the V^*_{bus} step change. As in Fig. 8 the ESD minimises deviations in V_{bus} during fault occurrence, $t = 5$ s in Fig. 9, and during load changes at $t = 9$ s and $t = 11$ s. $I_{gen\text{-}AC}$ and T_e, Figs. 9(i), (ii) and (iv), contain a transient following the generator fault condition as the ESD has no direct effect on generator currents. Figs. 9(v) and (vi) confirm the performance of the ESD during both generator fault occurrence and load changes.

Interestingly, with only CPLs in the system, the DC-bus becomes unstable when the ESD is disconnected, illustrating a further benefit of the device.

6 Conclusions

Experimental results on a five-phase, fault-tolerant generator show that a single-phase AC short-circuit fault results in excessive DC-bus voltage deviations. A simulation model based on the test results is then used to show that an ESD with a load-tracking, power balance controller enters a runaway mode during such transients. To overcome this problem a simple fault mitigation function is added to the ESD to control the DC-bus transient during short-circuit faulted operation of the generator. The fault mitigation controller enables the ESD to respond instantaneously to generator faults, virtually eliminating voltage transients from the DC-bus. The simulation model was then extended to impose a three-phase short-circuit fault on the five-phase generator, which represents one of the worst-case fault scenarios. Combined resistive and CPLs were used to demonstrate the system performance under faulted generator conditions both with and without the ESD. The ESD was also seen to provide some attenuation of the second-harmonic bus voltage ripple that occurs during generator fault conditions. A bus switching event represented by a step in DC-bus reference voltage was also examined to demonstrate the robustness of the ESD control.

The ESD, with a multi-input controller, has been demonstrated to be multi-functional in that it mitigates DC-bus voltage transients which occur as a result of normal events on the DC-bus, such as generator short-circuit faults, load changes (combined resistive and constant power) and bus switching events represented by step changes in voltage reference. Combining functionality in a single electrical subsystem, as in the case of this ESD, minimises the increase in system weight, which is a critical factor in aircraft applications. The significant reduction in voltage deviations during normal events on the DC-bus when the ESD is online enables the limits in MIL-STD-704F to be respected.

More generally the work in this paper illustrates the importance of energy storage in on-board power networks for a range of functions including power quality management, system stability and the control of transients on the prime mover. Optimising these multiple objectives and the capacity of the ESD are topics for further research.

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